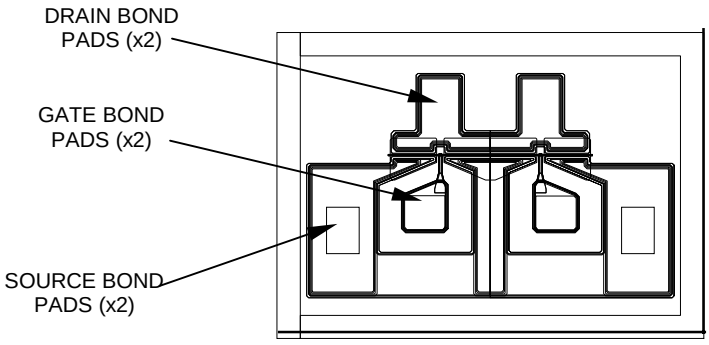
Filtronic LP7512

Solid State

Ultra Low Noise PHEMT

FEATURES

- **0.6 dB Typical Noise Figure at 12 GHz**
- **12.0 dB Typical Associated Gain at 12 GHz**
- **Low DC Power Consumption**
- **Excellent Phase Noise**



DIE SIZE: 18 x 13 mils (460 x 330 µm)
DIE THICKNESS: 3.8 mils (100 µm typ.)
BONDING PADS: 1.9 x 1.9 mils (50 x 50 µm typ.)

DESCRIPTION AND APPLICATIONS

The LP7512 is an Aluminum Gallium Arsenide / Indium Gallium Arsenide (AlGaAs/InGaAs) Pseudomorphic High Electron Mobility Transistor (PHEMT), utilizing an Electron-Beam direct-write 0.25 µm by 200 µm Schottky barrier gate. The recessed "mushroom" gate structure minimizes parasitic gate-source and gate resistances. The epitaxial structure and processing have been optimized for ultra low noise and usable gain to 40 GHz. The LP7512 also features Si_3N_4 passivation and is available in a 70 mil ceramic package (P70) and the SOT-23 low cost plastic package.

Typical applications include low noise receiver preamplifiers for commercial applications including Cellular/PCS systems, broad bandwidth commercial instrumentation and military EW amplifiers, and commercial Space applications.

The LP7512 may be procured in a variety of grades, depending upon specific user requirements. Standard lot screening is patterned after MIL-STD-19500, JANC grade. Space-level screening to FSS JANS grade is also available.

PERFORMANCE SPECIFICATIONS (T_A = 25°C)

SYMBOLS	PARAMETERS		MIN	TYP	MAX	UNITS
I_{DSS}	Saturated Drain-Source Current V_{DS} = 2V V_{GS} = 0V		15		50	mA
NF_{MIN}	Minimum Noise Figure V_{DS} = 2.0V, I_{DS} = 25% I_{DSS}	*f* = 12 GHz *f* = 18 GHz		0.6 1.0	0.9 1.4	dB dB
G_A	Associated Gain at Minimum Noise Figure V_{DS} = 2.0V, I_{DS} = 25% I_{DSS}	*f* = 12 GHz *f* = 18 GHz	11.0 7.5	12.0 8.5		dB dB
G_M	Transconductance	V_{DS} = 2V V_{GS} = 0V	60	90		mS
V_P	Pinch-Off Voltage	V_{DS} = 2V I_{DS} = 1mA	-0.2	-0.4	-1.5	V
I_{GDO}	Gate-Drain Leakage Current	V_{GD} = -3V		1	10	µA
I_{GSO}	Gate-Source Leakage Current	V_{GS} = -3V		1	10	µA
Θ_J	Thermal Resistivity (V_{DS} = 3.0V)			325		°C/W

DSS-034 WF

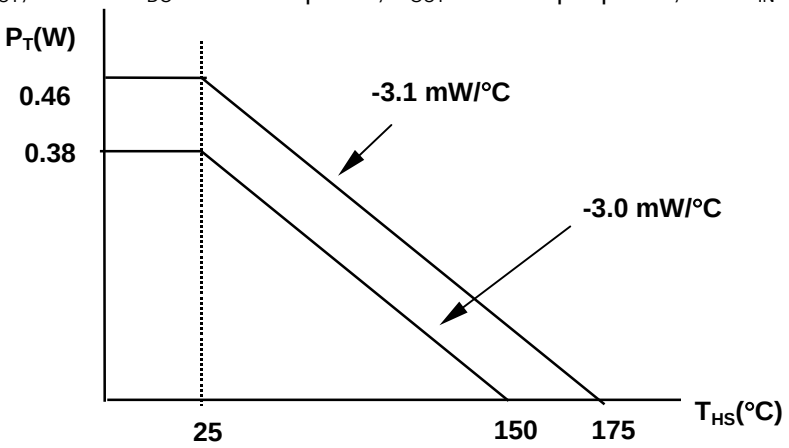
Phone: (408) 988-1845 **Internet:** http://www.filtronicsolidstate.com **Fax:** (408) 970-9950

ABSOLUTE MAXIMUM RATINGS (25°C)		
SYMBOL	**PARAMETER**	**RATING[1]**
V_{DS}	Drain-Source Voltage	4V
V_{GS}	Gate-Source Voltage	-2V
I_{DS}	Drain-Source Current	I_{DSS}
I_G	Gate Current	5 mA
P_{IN}	RF Input Power	50 mW
T_{CH}	Channel Temperature	175°C
T_{STG}	Storage Temperature	-65/175°C
P_T	Power Dissipation	460mW[3,4]

RECOMMENDED CONTINUOUS OPERATING LIMITS		
SYMBOL	**PARAMETER**	**RATING[2]**
V_{DS}	Drain-Source Voltage	3V
V_{GS}	Gate-Source Voltage	-0.6V
I_{DS}	Drain-Source Current	0.50 x I_{DSS}
I_G	Gate Current	2 mA
P_{IN}	RF Input Power	25 mW
T_{CH}	Channel Temperature	150°C
T_{STG}	Storage Temperature	-20/50°C
P_T	Power Dissipation	380 mW[3,4]
G_{XdB}	Gain Compression	4 dB

NOTES:

1. Operating conditions that exceed the Absolute Maximum Ratings could result in permanent damage to the device.
2. Recommended Continuous Operating Limits should be observed for reliable device operation.
3. Power Dissipation defined as: $P_T \equiv (P_{DC} + P_{IN}) - P_{OUT}$, where: P_{DC} = DC bias power, P_{OUT} = RF output power, and P_{IN} = RF input power.
4. Power Dissipation to be de-rated as follows:
5. Specifications subject to change without notice.



Example:
V_{DS} = 3V, I_{DS} = 15 mA
$P_{IN} = P_{OUT}$ = 0 dBm (quiescent condition):
$P_T = P_{DC}$ = 0.045W
Max. continuous T_{HS} = 135°C

HANDLING PRECAUTIONS:

PHEMT chips should be stored in a dry nitrogen environment until assembly. Care should be exercised during handling to avoid damage to the devices. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 1A (0-500V), and further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

ASSEMBLY INSTRUCTIONS:

The recommended die attach is gold/tin eutectic solder under a nitrogen atmosphere. Stage temperature should be 280-290°C; maximum time at temperature is 1 min. Conductive epoxy is also acceptable. The recommended wire bond method is thermo-compression wedge bonding with 0.7 or 1.0 mil (0.018 or 0.025 mm) gold wire. Stage temperature should be 250-260°C.

APPLICATIONS NOTES AND DESIGN DATA:

Applications Notes are available from your local FSS Sales Representative, or directly from the factory. Complete design data, including S-parameters, Noise data, and Large-Signal models, is available on 3.5" diskette, or may be down-loaded from our Web Page.

DSS-034 WF