LCK4972 Low-Voltage PLL Clock Driver

1 Features

- Fully integrated PLL
- Output frequency up to 240 MHz
- 150 ps typical cycle-to-cycle jitter
- Output skews of less than 250 ps
- Single 3.3 V/2.5 V ±5% supply
- 52-pin TQFPT
- Compatible with *PowerPC*® and *Pentium*® microprocessors
- Pin compatible with 972 type devices

2 Description

Agere Systems' LCK4972 is a 3.3 V/2.5 V, PLL-based clock driver designed for high-performance RISC or CISC processor-based systems. The LCK4972 has output frequencies of up to 240 MHz and skews of less than 250 ps, making it ideal for synchronous systems. The LCK4972 contains 12 low-skew outputs and a feedback/sync output for flexibility and simple implementation.

There is a robust level of frequency programmability between the 12 low-skew outputs in addition to the input/output relationships. This allows for very flexible programming of the input reference versus the output frequency. The LCK4972 contains a flexible output enable and disable scheme. This helps execute system debug as well as offer multiple powerdown schemes, which meet green-class machine requirements.

The LCK4972 features a power-on reset function, which automatically resets the device on powerup, providing automatic synchronization between QFB and other outputs.

The LCK4972 is 3.3 V/2.5 V compatible and requires no external loop filters. It has the capability of driving 50 Ω transmission lines. Series terminated lines have the ability of driving two 50 Ω lines in parallel, effectively doubling the fanout.

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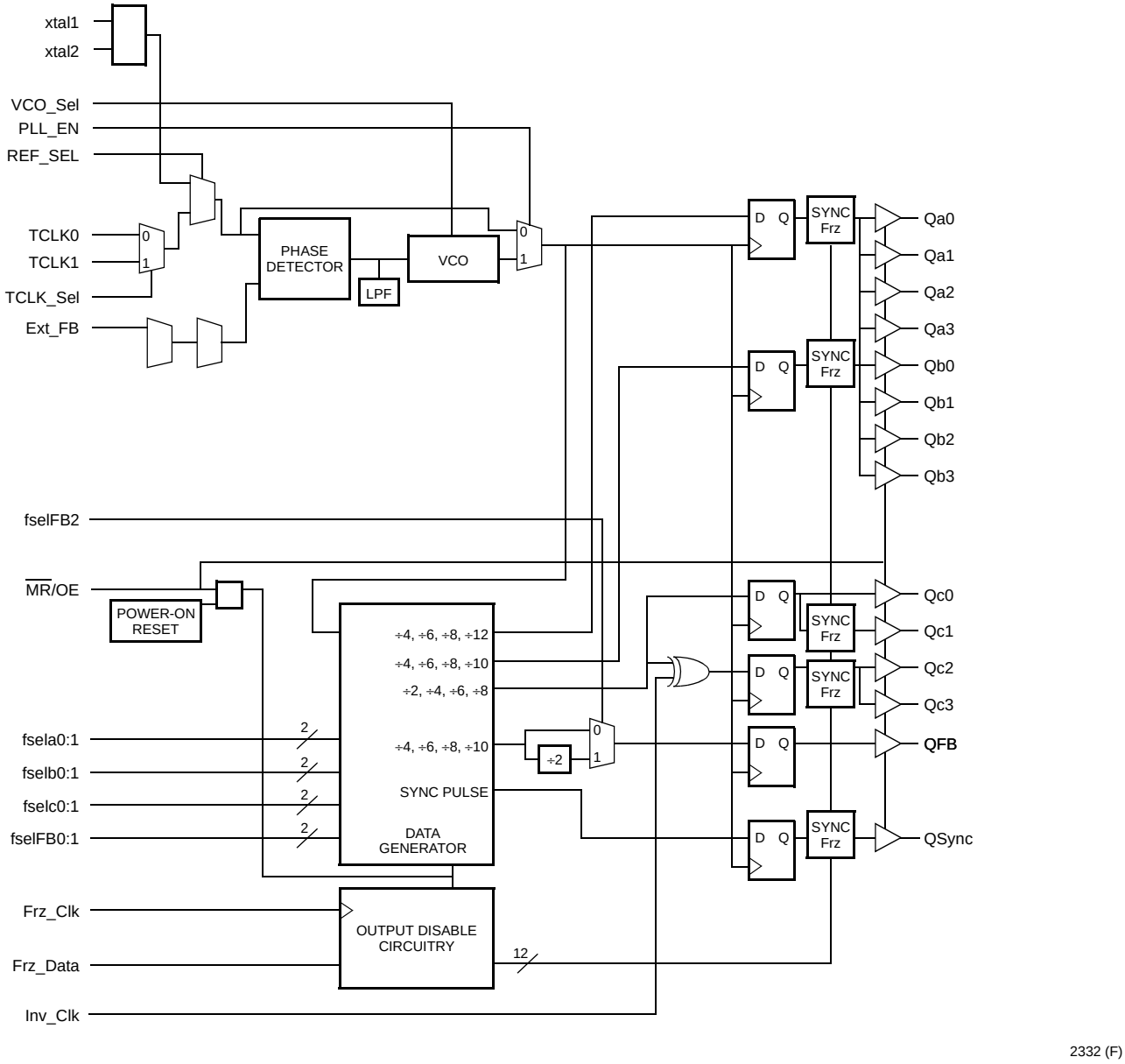

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Figure 2-1. Logic Diagram

3 Pin Information

3.1 Pin Diagram

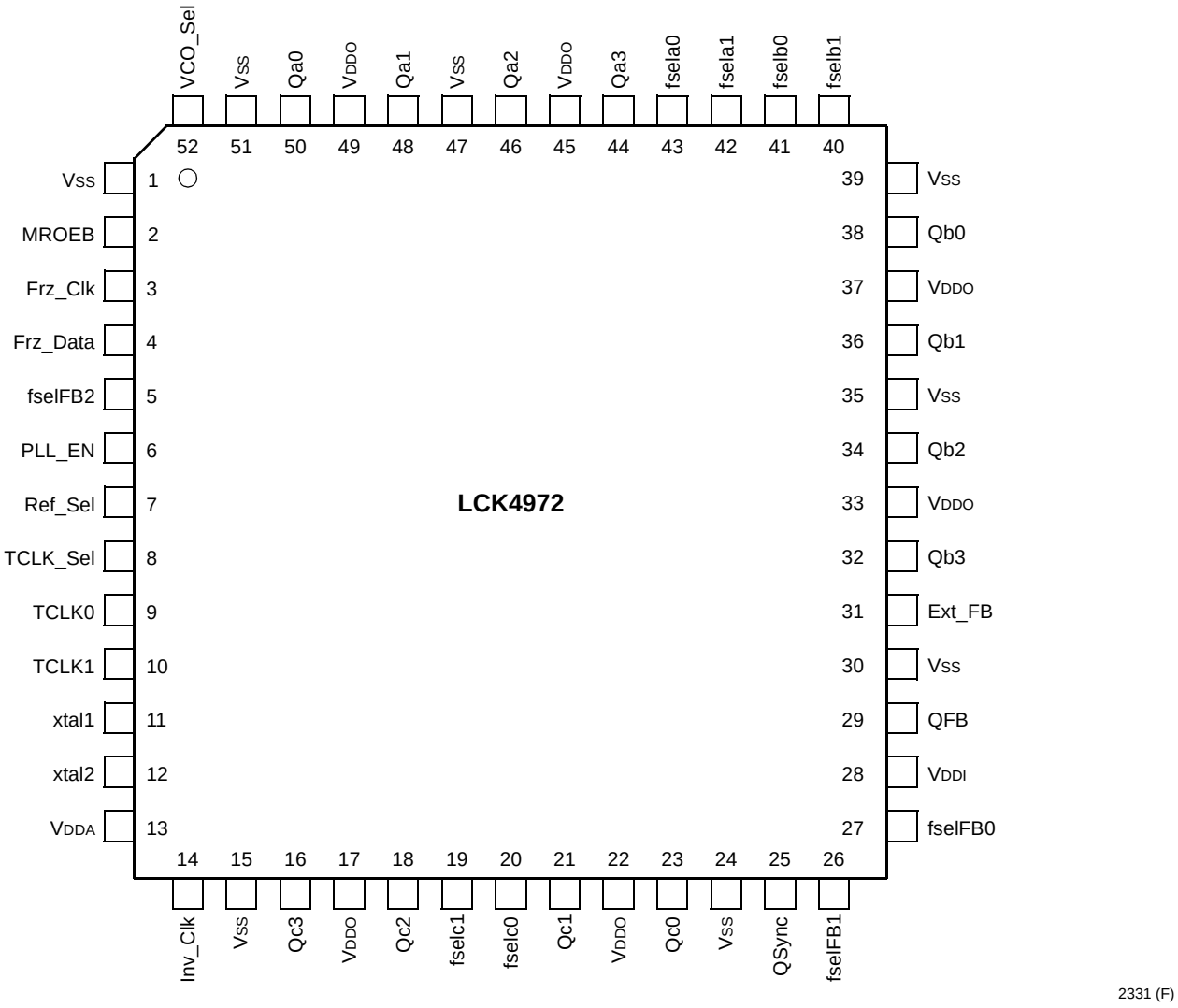


Figure 3-1. 52-Pin TQFPT

Table 3-1. Pin Description

Pin	Symbol	Type	I/O*	Description
1, 15, 24, 30, 35, 39, 47, 51	VSS	Ground	—	**Ground.**
2	MROEB	LVTTL	I^u	**Master Reset and Output Enable Input.** 0 = Outputs disabled (high-impedance state). During this condition the PLL loop is open and the VCO will run at an indeterminate frequency. 1 = Normal operation (outputs active).
3	Frz_Clk	LVTTL	I	**Freeze Mode.**
4	Frz_Data	LVTTL	I	**Freeze Mode.**
5	fselFB2	LVTTL	I^u	**Feedback Output Divider Function Select.** This input, along with pins fselFB0 and fselFB1, controls the divider function of the feedback bank of outputs. See Table 4-2 for more details.
6	PLL_EN	LVTTL	I^u	**PLL Bypass Select.** 0 = The internal PLL is bypassed and the selected reference input provides the clocks to operate the device. 1 = The internal PLL provides the internal clocks to operate the device.
7	Ref_Sel	LVTTL	I^u	**Reference Select Input.** The Ref_Sel input controls the reference input to the PLL. 0 = The input is selected by the TCLK_Sel input. 1 = The XTAL is selected.
8	TCLK_Sel	LVTTL	I^u	**TCLK Select Input.** The TCLK_Sel input controls which TCLK input will be used as the reference input if Ref_Sel is set to 0. 0 = TCLK0 is selected. 1 = TCLK1 is selected.
9, 10	TCLK[0:1]	LVTTL	I	**LVTLL Reference Input.** These inputs provide the reference frequency for the internal PLL when selected by Ref_Sel and TCLK_Sel.
11	xtal1	Analog	I	**Xtal Reference Input.** This input provides the reference frequency for the internal PLL when selected by Ref_Sel.
12	xtal2	Analog	I	**Xtal Reference Input.** This input provides the reference frequency for the internal PLL when selected by Ref_Sel.
13	VDDA	Power	—	**PLL Power.**
14	Inv_Clk	LVTTL	I^u	**Invert Mode.** This input only affects the Qc bank. 0 = All outputs of the Qc bank are in the normal phase alignment. 1 = Qc2 and Qc3 are inverted from the normal phase of Qc0 and Qc1.
16, 18, 21, 23	Qc[3:0]	LVTTL	O	**Clock Output.** These outputs, along with the Qa[0:3], Qb[0:3], and QFB outputs, provide numerous divide functions determined by the fsela[0:3], fselb[0:3], and the fselFB[0:2] See Table 4-1 and Table 4-2 for more details.
17, 22, 33, 37, 45, 49	VDDO	Power	—	**Output Buffer Power.**
19, 20	fselc[1:0]	LVTTL	I^u	**Output Divider Function Select.** Each pair controls the divider function of the respective bank of outputs. See Table 4-1 for more details.

* U = Internal pull-up resistors (50 kΩ).

Table 3-1. Pin Description (continued)

Pin	Symbol	Type	I/O*	Description
25	QSync	LVTTL	O	**Synchronous Pulse Output.** This output is used for system synchronization. See Section 4.4 on page 10.
26	fselFB1	LVTTL	I^u	**Feedback Output Divider Function Select.** This input, along with pins fselFB1 and fselFB2, controls the divider function of the feedback bank of outputs. See Table 4-2 for more details.
27	fselFB0	LVTTL	I^u	**Feedback Output Divider Function Select.** This input, along with pins fselFB0 and fselFB2, controls the divider function of the feedback bank of outputs. See Table 4-2 for more details.
28	V_{DDI}	Power	—	**PLL Power.**
29	QFB	LVTTL	O	**Clock Output.** This output, along with the Qa[0:3] and Qc[0:3] outputs, provides numerous divide functions determined by the fsela[0:3], fselb[0:3], and the fselFB[0:2]. See Table 4-1 and Table 4-2 for more details.
31	Ext_FB	LVTTL	I	**PLL Feedback Input.** This input is used to connect one of the clock outputs (usually QFB) to the feedback input of the PLL.
32, 34, 36, 38	Qb[3:0]	LVTTL	O	**Clock Output.** These outputs, along with the Qa[0:3], Qc[0:3], and QFB outputs, provide numerous divide functions determined by the fsela[0:3], fselb[0:3], and the fselFB[0:2]. See Table 4-1 and Table 4-2 for more details.
40, 41	fselb[1:0]	LVTTL	I	**Output Divider Function Select.** Each pair controls the divider function of the respective bank of outputs. See Table 4-1 for more details.
42, 43	fsela[1:0]	LVTTL	I	**Output Divider Function Select.** Each pair controls the divider function of the respective bank of outputs. See Table 4-1 for more details.
44, 46, 48, 50	Qa[3:0]	LVTTL	O	**Clock Output.** These outputs, along with the Qb[0:3], Qc[0:3], and QFB outputs, provide numerous divide functions determined by the fsela[0:3], fselb[0:3], and the fselFB[0:2]. See Table 4-1 and Table 4-2 for more details.
52	VCO_Sel	LVTTL	I^u	**VCO Frequency Select Input.** This input selects the nominal operating range of the VCO used in the PLL. 0 = The VCO range is 150 MHz—240 MHz. 1 = The VCO range is 200 MHz—480 MHz.

* U = Internal pull-up resistors (50 kΩ).

4 Functional Description

Using the select lines (fsela[1:0], fselb[1:0], fselc[1:0], and fselFB[2:0]), the following output frequency ratios between outputs can be obtained:

1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 5:1, 5:2, 5:3, 6:1, and 6:5

These ratios can be achieved by forcing the control signal low one clock edge before the coincident edges of outputs Qa and Qc. The synchronization output indicates when these rising edges will occur. Selectability of feedback frequency is independent of the output frequencies. Output frequencies can be odd or even multiples of the input reference clock, as well as being less than the input frequency.

The power-on reset function is designed to reset the system after powerup for synchronization between QFB and other outputs.

The LCK4972 has the ability to independently enable/disable each output through a serial input port. When disabled (frozen), the outputs will freeze to the low state while internal state machines remain unaffected. When re-enabled, the outputs initialize synchronously and in phase with those not reactivated. Freezing only happens when the outputs are in the low state, preventing runt pulse generation, see Section 4.5 Output Freeze Circuitry on page 12.

Table 4-1. Function Table for Qa, Qb, and Qc

fsela1	fsela0	Qa	fselb1	fselb0	Qb	fselc1	fselc0	Qc
0	0	÷4	0	0	÷4	0	0	÷2
0	1	÷6	0	1	÷6	0	1	÷4
1	0	÷8	1	0	÷8	1	0	÷6
1	1	÷12	1	1	÷10	1	1	÷8

Table 4-2. Function Table for QFB

fselFB2[1]	fselFB1	fselFB0	QFB
0	0	0	÷4
0	0	1	÷6
0	1	0	÷8
0	1	1	÷10
1	0	0	÷8
1	0	1	÷12
1	1	0	÷16
1	1	1	÷20

1. If fselFB2 is set to 1, it may be necessary to apply a reset pulse after powerup in order to ensure synchronization between the QFB and other inputs.

Table 4-3. Function Table for Logic Selection

Control Pin	Logic 0	Logic 1
VCO_Sel	VCO/2	VCO
Ref_Sel	TCLK	Xtal
TCLK_Sel	TCLK0	TCLK1
PLL_EN	Bypass PLL	Enable PLL
$\overline{MR}$/OE	Master reset/output high-Z	Enable outputs
Inv_Clk	Noninverted Qc2, Qc3	Inverted Qc2, Qc3

4.1 Device Programming

The LCK4972 contains three independent banks of four outputs as well as an independent PLL feedback output. The possible configurations make Agere Systems' LCK4972 one of the most versatile frequency programming devices. Table 4-4 shows various selection possibilities.

Table 4-4. Programmable Output Frequency Relationships for Qa, Qb, and Qc (VCO_Sel = 1)

fsela1	fsela0	Qa	fselb1	fselb0	Qb	fselc1	fselc0	Qc
0	0	VCO/4	0	0	VCO/4	0	0	VCO/2
0	1	VCO/6	0	1	VCO/6	0	1	VCO/4
1	0	VCO/8	1	0	VCO/8	1	0	VCO/6
1	1	VCO/12	1	1	VCO/10	1	1	VCO/8

Table 4-5. Programmable Output Frequency Relationships for QFB (VCO_Sel = 1)

fselFB2	fselFB1	fselFB0	QFB
0	0	0	VCO/4
0	0	1	VCO/6
0	1	0	VCO/8
0	1	1	VCO/10
1	0	0	VCO/8
1	0	1	VCO/12
1	1	0	VCO/16
1	1	1	VCO/20

To determine the relationship between the three banks, compare their divide ratios. For example, if a ratio of 5:3:2 is desired, set Qa to ÷10, Qb to ÷6, and Qc to ÷4. These selections would yield a 5:3:2 ratio.

For low frequency circumstances, the VCO_Sel pin allows the option of an additional ÷2 to be added to the clock path. This pin maintains the output relationships, but provides an extended clock range for the PLL. The feedback output is matched to the input reference frequency after the output frequency relationship is set and VCO is in a stable range.

If, in the previous example, the input reference frequency were equal to the lowest output frequency, the output would be set to ÷10 mode. The fselFB2 input could be asserted to half the frequency if the needed feedback frequency is half of the lowest frequency output. This multiplies the output frequencies by a factor of two, relative to the input reference frequency.

Assume the previously mentioned 5:3:2 ratio with the highest output frequency of 100 MHz. If the only available reference frequency is 50 MHz, the setup of Figure 4-1 can be used. The device provides 100 MHz, 66 MHz, and 40 MHz outputs, all generated from the 50 MHz source. Figure 4-2 and Figure 4-3 also show possible configurations of the LCK4972.

4.2 Application Examples

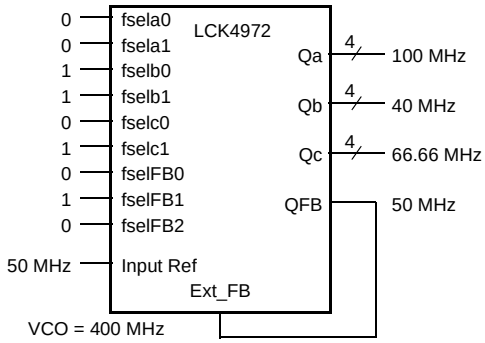


Figure 4-1. 100 MHz from 50 MHz Example

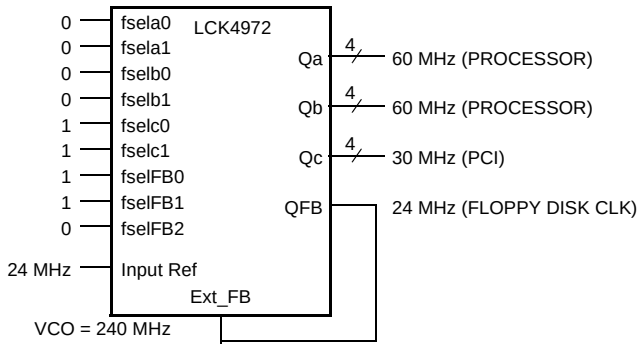


Figure 4-2. *Pentium* Compatible Clocks Example

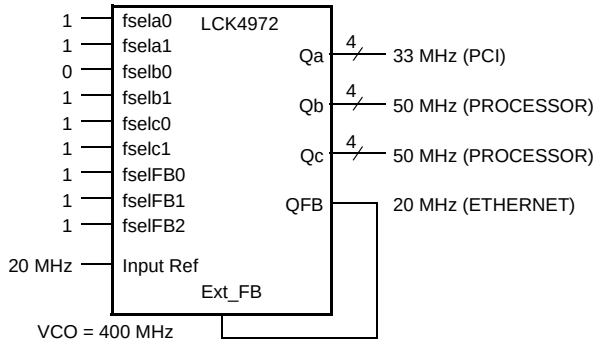


Figure 4-3. 20 MHz Source Example

4.3 Typical Skew Example

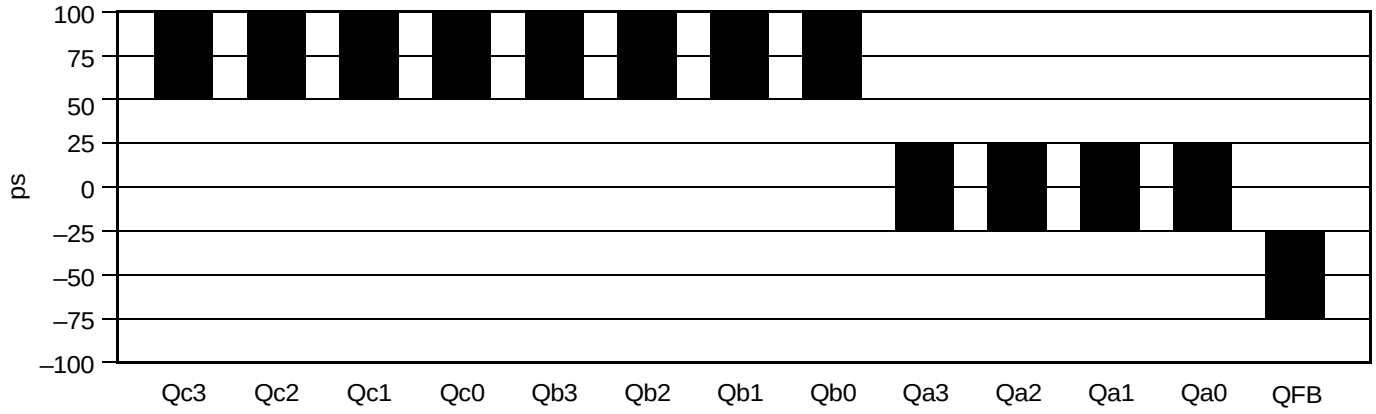


Figure 4-4. Skew Relative to Qa

The Inv_Clk input pin, when asserted, will invert the Qc2 and Qc3 outputs. This inversion does not affect the output-output skew of the device and allows for the development of 180° phase-shifted clocks. This output can also be used as a feedback output or routed to a second PLL to generate early/late clocks. Figure 4-5 shows a 90° phase-shift configuration.

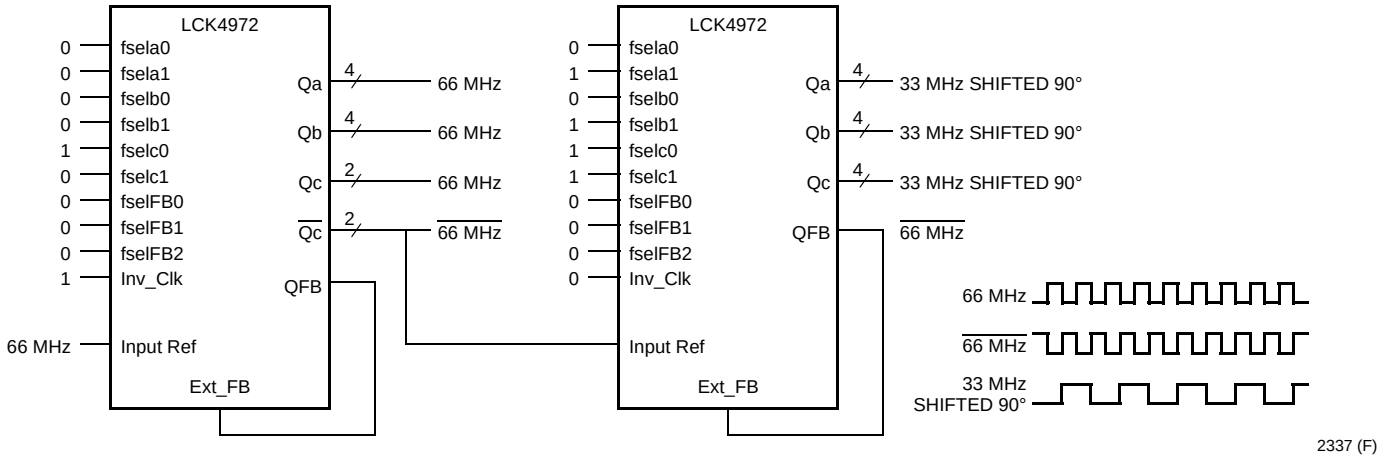


Figure 4-5. Phase Delay Example Using Two LCK4972s

4.4 SYNC Output

When the output frequencies are not integer multiples of each other, there is a need for a signal for synchronization purposes. The SYNC output is designed to address this need. The Qa and Qc banks of outputs are monitored by the device, and a low-going pulse (one period in duration, one period before the coincident rising edges of Qa and Qc) is provided. The duration and placement of the pulse is dependent on the highest of Qa and Qc output frequencies. The timing diagram, (Figure 4-6) shows the various waveforms for SYNC.

Note: SYNC is defined for all possible combinations of Qa and Qc, even though the lower frequency clock should be used as a synchronizing signal in most cases.

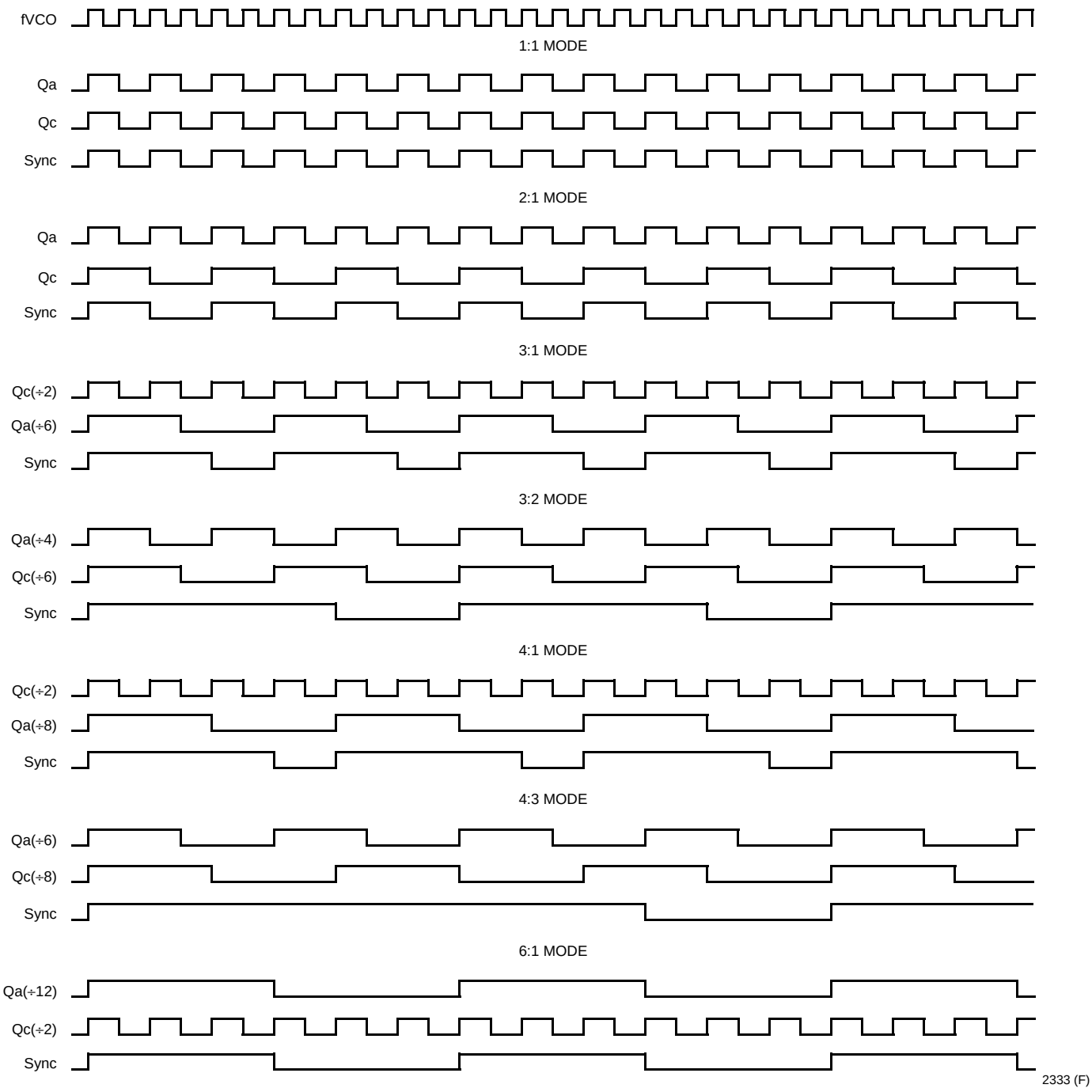


Figure 4-6. LCK4972 Timing

4.5 Output Freeze Circuitry

The new green classification for computers requires unique power management. The LCK4972's individual output enable control allows software to implement unique power management. A serial interface was created to eliminate individual output control at the cost of one pin per output.

The freeze control logic provides a mechanism for the LCK4972's clock outputs to be stopped in the logic 0 state.

The freeze mechanism allows serial loading of the 12-bit serial input register. This register contains one programmable freeze enable bit for 12 of the 14 output clocks. The Qc0 and QFB outputs cannot be frozen with the serial port, which prevents possible lock-up situations if there is an error in the serial input register. The user can also program a freeze by writing 0 to the respective freeze bit. Likewise, it can be programmed unfrozen by writing a 1 to that same bit.

Freeze logic cannot force a recently frozen clock to a logic 0 state before the time which it would normally transition to that state. The logic will only maintain the frozen clock in logic 0. Similarly, the logic will not force a recently frozen clock to logic 1 before the time it would normally transition there. When the clock would normally be in a logic 0 state, the logic re-enables the unfrozen clock, eliminating the possibility of runt clock pulses.

The user may write to the serial input register by supplying a logic 0 start bit followed (serially) by 12 NRZ freeze bits through Frz_Data. The period of the Frz_Clk signal equals the period of each Frz_Data bit. The timing should be such that the LCK4972 is able to sample each Frz_Data bit with the rising edge of the Frz_Clk (free running) signal.

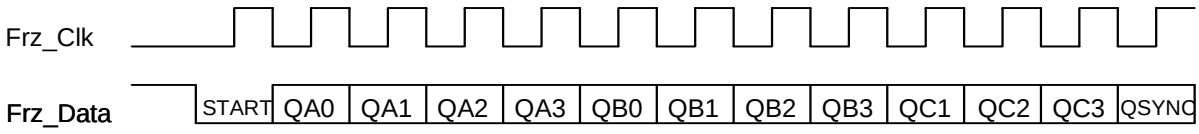


Figure 4-7. Freeze Data Input Protocol

4.6 On-Board Crystal Oscillator

The LCK4972 features an on-board crystal oscillator for seed clock generation. The oscillator is self-contained. The only external component required is the crystal. The circuit is a series resonant circuit, eliminating the need for large on-board capacitors.

This series resonant design calls for a series resonant crystal, but most crystals are characterized in parallel resonant mode. Physically, a parallel resonant crystal is no different from a series resonant crystal. Overall, a parallel crystal can be used with this device with a small frequency error due to the actual series resonant frequency of the parallel resonant crystal. A parallel specified crystal will exhibit an oscillatory frequency ±100 ppm lower than the specified value. This translates to ineffectual kHz inaccuracies, which will not effect the device.

Table 4-6. Crystal Recommendations

Parameter	Value
Crystal Cut	Functional AT cut
Resonance	Series resonance
Frequency Tolerance	±75 ppm at 25 °C
Frequency/Temperature Stability	±150 ppm at 0 °C—70 °C
Operating Range	0 °C—70 °C
Shunt Capacitance	5 pF—7 pF
Equivalent Series Resistance (ESR)	50 Ω—80 Ω max
Correlation Drive Level	100 µW
Aging	5 ppm/year (first 3 years)

4.7 Power Supply Filtering

The LCK4972 is a mixed-signal product which is susceptible to random noise, especially when this noise is on the power supply pins. To isolate the output buffer switching from the internal phase-locked loop, the LCK4972 provides separate power supplies for the internal PLL (V_{DDA}) and for the output buffers (V_{DDO}). In a digital system environment, besides this isolation technique, it is highly recommended that both V_{DDA} and V_{DD} power supplies be filtered to reduce the random noise as much as possible.

Figure 4-8 illustrates a typical power supply filter scheme. Due to its susceptibility to noise with spectral content in this range, a filter for the LCK4972 should be designed to target noise in the 100 kHz to 10 MHz range. The RC filter in Figure 4-8 will provide a broadband filter with approximately 100:1 attenuation for noise with spectral content above 20 kHz. More elaborate power supply schemes may be used to achieve increased power supply noise filtering.

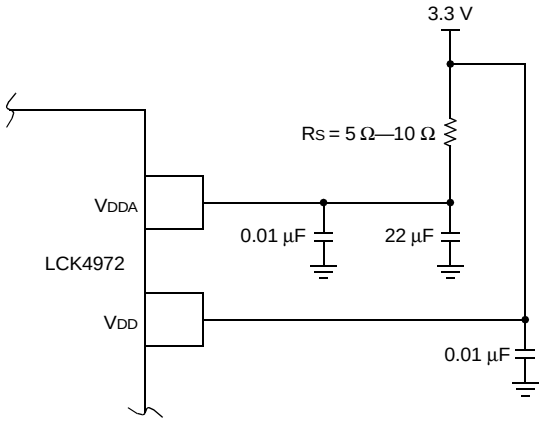


Figure 4-8. Power Supply Filter

4.8 Driving Transmission Lines

The output drivers of the LCK4972 were designed for the lowest impedance possible for maximum flexibility. With the LCK4972's 7 Ω impedance, the drivers can accommodate either parallel or series terminated transmission lines.

Point-to-point distribution of signals is the preferred method in today's high-performance clock networks. Series-terminated or parallel-terminated lines can be used in a point-to-point scheme. The parallel configuration terminates the signal at the end of the line with a 50 Ω resistance to $V_{DD}/2$. Only one terminated line can be driven by each output of the LCK4972 due to the high level of dc current drawn.

In a series-terminated case, there is no dc current draw; the outputs can drive multiple series-terminated lines, see below.

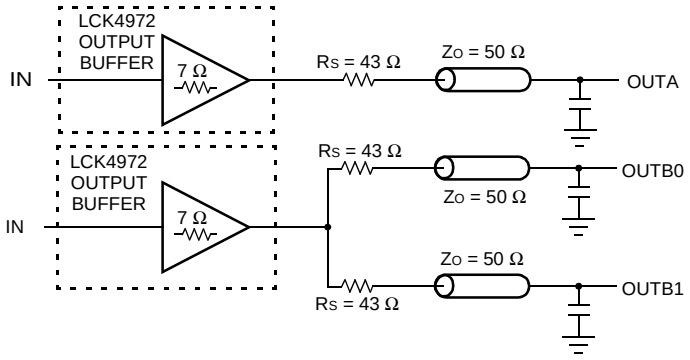


Figure 4-9. Dual Transmission Lines

The waveform plots of Figure 4-10 show the simulated results of a single output versus a two-line output. A 43 ps delta exists between the two differently loaded outputs that can be seen in the figure. This implies that dual-line driving need not be used in order to maintain tight output-to-output skew. The step in the figure shows an impedance mismatch caused when looking into the driver. The parallel combination in Figure 4-9 plus the output resistance do not equal the parallel combination of the line impedances. The voltage wave down the lines will equal the following:

$VL = VS (Z_0/R_S + R_0 + Z_0) = 3.0 (25/53.5) = 1.4$ V

The voltage will double at the load-end to 2.8 V, due to the near-unity reflection coefficient. It then continues to increment towards 3.0 V in one-round trip delay steps (4 ps). This step will not cause any false clock triggering, but some users may not want these reflections on the line. Figure 4-11 shows a possible configuration to eliminate these reflections. In this scenario, the series terminating resistors are reduced so the line impedance is matched when the parallel combination is added to the output buffer.

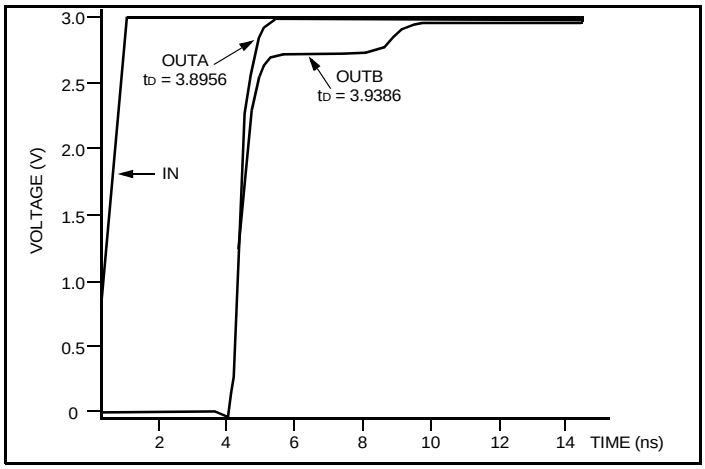


Figure 4-10. Single vs. Dual Waveforms

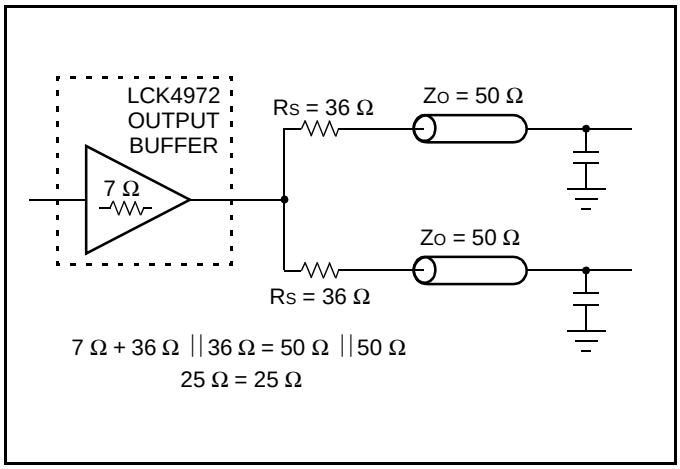


Figure 4-11. Optimized Dual Transmission Lines

5 Absolute Maximum Ratings

Stresses which exceed the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods of time can adversely affect device reliability.

Table 5-1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	–0.3	4.6	V
Input Voltage	V_I	–0.3	V_{DD} + 0.3	V
Input Current	I_{IN}	—	±20	mA
Storage Temperature Range	T_{stg}	–40	125	°C

5.1 Handling Precautions

Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. Agere employs both a human-body model (HBM) and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114 (HBM) and JESD22-C101 (CDM) standards.

Table 5-2. ESD Tolerance

Device	Minimum Threshold	
	HBM	CDM
LCK4972	>2500 V	>1000 V

5.2 Thermal Parameters (Definitions and Values)

System and circuit board level performance depends not only on device electrical characteristics, but also on device thermal characteristics. The thermal characteristics frequently determine the limits of circuit board or system performance, and they can be a major cost adder or cost avoidance factor. When the die temperature is kept below 125 °C, temperature activated failure mechanisms are minimized. The thermal parameters that Agere provides for its packages help the chip and system designer choose the best package for their applications, including allowing the system designer to thermally design and integrate their systems.

It should be noted that all the parameters listed below are affected, to varying degrees, by package design (including paddle size) and choice of materials, the amount of copper in the test board or system board, and system airflow.

Θ_{JA} - Junction to Air Thermal Resistance

Θ_{JA} is a number used to express the thermal performance of a part under JEDEC standard natural convection conditions. Θ_{JA} is calculated using the following formula:

$\Theta_{JA} = (T_J – T_{amb}) / P$; where P = power

Θ_{JMA} - Junction to Moving Air Thermal Resistance

Θ_{JMA} is effectively identical to Θ_{JA} but represents performance of a part mounted on a JEDEC four layer board inside a wind tunnel with forced air convection. Θ_{JMA} is reported at airflows of 200 LFPM and 500 LFPM (linear feet per minute), which roughly correspond to 1 m/s and 2.5 m/s (respectively). Θ_{JMA} is calculated using the following formula:

$\Theta_{JMA} = (T_J – T_{amb}) / P$

Θ_{JC} - Junction to Case Thermal Resistance

Θ_{JC} is the thermal resistance from junction to the top of the case. This number is determined by forcing nearly 100% of the heat generated in the die out the top of the package by lowering the top case temperature. This is done by placing the top of the package in contact with a copper slug kept at room temperature using a liquid refrigeration unit. Θ_{JC} is calculated using the following formula:

$\Theta_{JC} = (T_J - T_C) / P$

Θ_{JB} - Junction to Board Thermal Resistance

Θ_{JB} is the thermal resistance from junction to board. This number is determined by forcing the heat generated in the die out of the package through the leads or balls by lowering the board temperature and insulating the package top. This is done using a special fixture, that keeps the board in contact with a water chilled copper slug around the perimeter of the package while insulating the package top. Θ_{JB} is calculated using the following formula:

$\Theta_{JB} = (T_J - T_B) / P$

Ψ_{JT}

Ψ_{JT} correlates the junction temperature to the case temperature. It is generally used by the customer to infer the junction temperature while the part is operating in their system. It is not considered a true thermal resistance. Ψ_{JT} is calculated using the following formula:

$\Psi_{JT} = (T_J - T_C) / P$

Table 5-3. Thermal Parameter Values

Parameter	Temperature °C/Watt
Θ_{JA}	51.11
Θ_{JMA} (1 m/s)	TBD
Θ_{JMA} (2.5 m/s)	TBD
Θ_{JC}	14.81
Θ_{JB}	40.23
Ψ_{JT}	1

6 Electrical Characteristics

Table 6-1. PLL Input Reference Characteristics (T_A = –40 °C to +85 °C)

Parameter	Symbol	Condition	Min	Max	Unit
TCLK Input Rise/Fall	tr, tf	—	—	3.0	ns
Reference Input Frequency	fref	—	—[1]	—[1]	MHz
Reference Input Duty Cycle	trefDC	—	25	75	%
Crystal Oscillator Frequency	txtal	—[2]	10	25	MHz

1. Maximum input reference frequency is limited by VCO lock range and the feedback driver or 100 MHz. Minimum input reference frequency is limited by the VCO lock range and the feedback divider.
2. See Section On-Board Crystal Oscillator, on page 12 for more crystal information.

6.1 dc Characteristics

Table 6-2. dc Characteristics (T_A = –40 °C to+85 °C, V_{DD} = 3.3 V ± 5%)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input High Voltage	VIH	—	2.0	—	3.6	V
Input Low Voltage	VIL	—	—	—	0.8	V
Output High Voltage	VOH	IOH = –24 mA[1]	2.4	—	—	V
Output Low Voltage	VOL	IOL = 24 mA[1]	—	—	0.5	V
Input Current	IIN	—[2]	—	—	±120	µA
Maximum Supply Current	IDD	All VDD pins	—	130	160	mA
Analog VDD Current	IDDA	VDDA pin only[3]	—	60	85	mA
Input Capacitance	CIN	—	—	—	4	pF
Power Dissipation Capacitance	Cpd	Per output	—	25	—	pF

1. The LCK4972 inputs can drive a series of parallel terminated transmission lines on the incident edge.
2. Inputs have pull-up/pull-down resistors, which affect input current.
3. Qa = Qb = Qc = 50 MHz, unloaded outputs.

Table 6-3. dc Characteristics (T_A = –40 °C to +85 °C, V_{DD} = 2.5 V ± 5%)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
PLL Supply Voltage	VDD_PLL	LVCMOS	2.325	—	VDD	V
Input High Voltage	VIH	LVCMOS	1.7	—	VDD + 0.3	V
Input Low Voltage	VIL	LVCMOS	–0.3	—	0.7	V
Output High Voltage	VOH	IOH = –15 mAS*	1.8	—	—	V
Output Low Voltage	VOL	IOL = 15 mA	—	—	0.6	V
Output Impedance	ZOUT	—	17	—	20	W
Input Current	IIN	VIN = VDD or GND	—	—	±120	µA
Analog VDD Current	IDDA	VDDA pin only†	—	60	85	mA
Maximum Supply Current	IDD	All VDD Pins	—	130	160	mA
Input Capacitance	CIN	—	—	—	4	pF
Power Dissipation Capacitance	Cpd	Per output	—	25	—	pF

* The LCK4972 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of VTT. Alternatively, the device drives up to two 50 Ω series terminated transmission lines per output.
† Qa = Qb = Qc = 50 MHz, unloaded outputs.

6.2 ac Characteristics

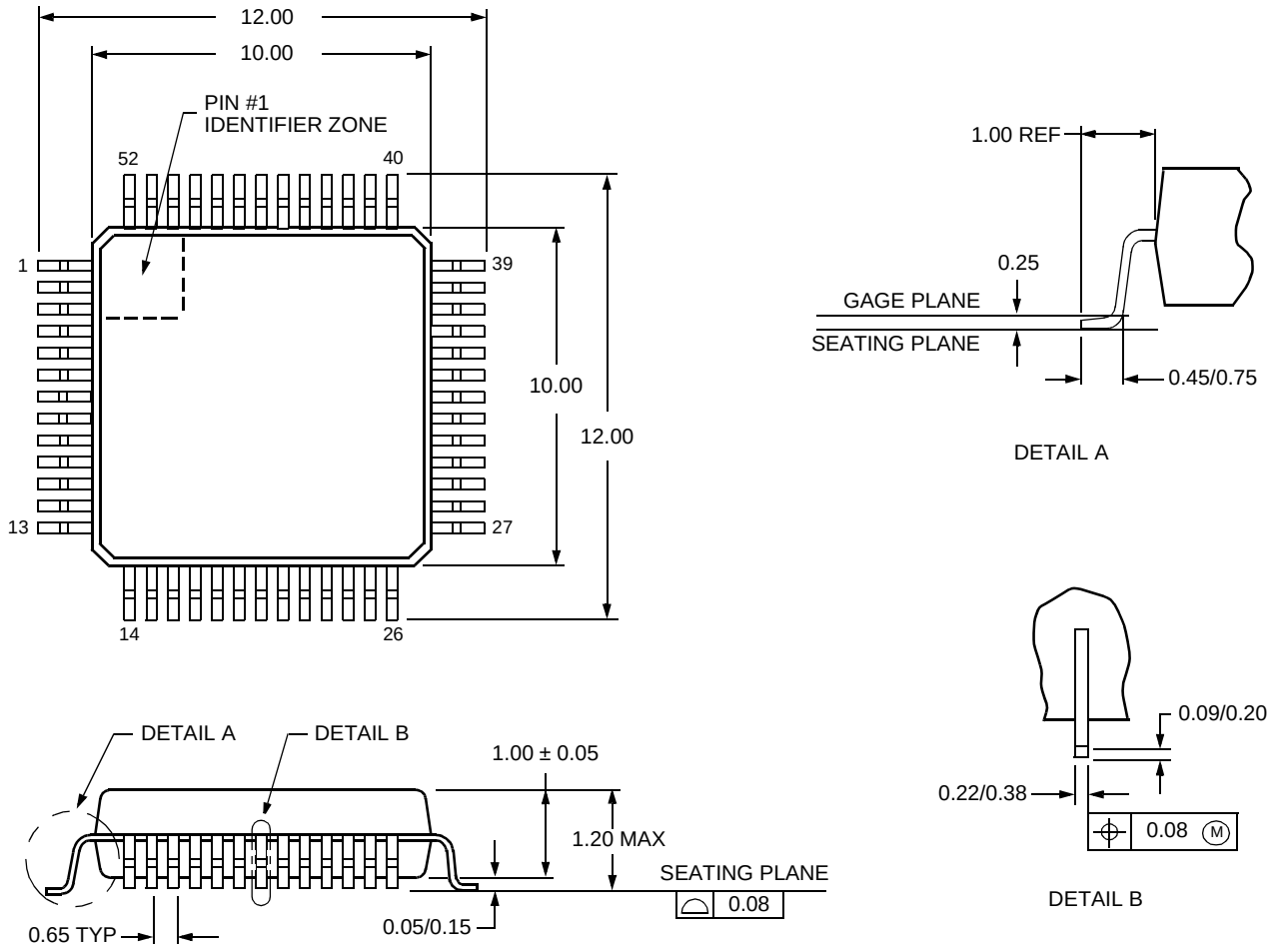
Table 6-4. ac Characteristics (T_A = –40 °C to +85 °C, V_{DD} = 3.3 V/2.5 V ± 5%)[1]

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Reference Frequency:	f_{REF}	PLL locked				MHz
÷4 feedback			37.5	—	120.0	
÷6 feedback			25.0	—	80.0	
÷8 feedback			18.75	—	60.0	
÷10 feedback			15.0	—	48.0	
÷12 feedback			12.5	—	40.0	
÷16 feedback			9.4	—	30.0	
÷20 feedback			7.5	—	24.0	
Input Reference Frequency in PLL Bypass Mode[2]	f_{REF}	PLL bypass	—	—	250	MHz
VCO Frequency Range[3]	f_{VCO}	—	150	—	480	MHz
Crystal Internal Frequency Range[4]	f_{XTAL}	—	10	—	25	MHz
Output Frequency:	f_{MAX}	PLL locked				MHz
÷2 output			75.0	—	240.0	
÷4 output			37.5	—	120.0	
÷6 output			25.0	—	80.0	
÷8 output			18.75	—	60.0	
÷10 output			15.0	—	48.0	
÷12 output			12.5	—	40.0	
Serial Interface Clock Frequency	f_{STOP_CLK}	—	—	—	20	MHz
Reference Input Duty Cycle	f_{REFDC}	—	25	—	75	%
CCLKx Input Rise/Fall Time	t_R, t_F	20% to 80%	—	—	1.0	ns
Propagation Delay (static phase offset) CCLKx or FB_IN	t(∅)	PLL locked	—	—	150	ps
Output-to-Output Skew	$t_{SK(O)}$	—	—	—	250	ps
Output Duty Cycle	DC	—	47	50	53	%
Output Rise/Fall Time	t_R, t_F	20% to 80%	0.1	—	1.0	ns
Output Disable Time	$t_{PLZ, HZ}$	—	—	—	8	ns
Output Enable Time	$t_{PZL, LZ}$	—	—	—	8	ns
Cycle-to-Cycle Jitter[5]	$t_{JIT(CC)}$	—	—	150	200	ps
Period Jitter	$t_{JIT(PER)}$	—	—	—	150	ps
I/O Phase Jitter	$t_{JIT(∅)}$	—	—	—	150	ps
Maximum PLL Lock Time	t_{LOCK}	—	—	10	—	ms

1. ac characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. In bypass mode, the LCK4972 divides the input reference clock.
3. The input reference frequency must match the VCO lock range divided by the total feedback divider ratio: $f_{REF} = f_{VCO} \div (M \times VCO\_SEL)$.
4. The crystal frequency range must meet the interface frequency range and the VCO lock range divided by the feedback divider ratio: f_{XTAL} (min, max) = f_{VCO} (min, max) ÷ (M x VCO_SEL) and 10 MHz ≤ f_{XTAL} ≤ 25 MHz.
5. t_{JIT} (CC) is valid for a VCO frequency of 400 MHz with QFB = to divide by 4.

7 Outline Diagram

52-pin TQFPT package outline. All dimensions are in millimeters.



8 Ordering Information

Table 8-1. LCK4972 Ordering Information

Device	Package Type	Comcode	Delivery
LCK4972	TQFPT	700010364	Tray

For additional information, contact your Agere Systems Account Manager or the following:
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