LCK4801
Low-Voltage HSTL Differential Clock

General

The LCK4801 is a low-voltage, 3.3 V HSTL differential clock synthesizer. The LCK4801 supports two differential HSTL output pairs with frequencies from 336 MHz to 1 GHz. The clock is designed to support single and multiple processor systems that require HSTL differential inputs. The LCK4801 contains a fully integrated PLL (phase-locked loop) which multiplies the HSTL_CLK or PECL_CLK input frequency to match individual processor clock frequencies. The PLL can be bypassed so that the PCLK outputs are fed from the HSTL_CLK or PECL_CLK input for test purposes. All outputs are powered from a 2 V external supply to reduce on-chip power consumption. All outputs are HSTL. The PLL can operate in the internal feedback mode, or in the external feedback mode for board level debugging applications.

Features

- Two fully selectable clock inputs.
- Fully integrated PLL.
- 336 MHz to 1 GHz output frequencies.
- HSTL outputs.
- HSTL and LVPECL reference clocks.
- 32-pin TQFP package.
- Pin compatible with *Motorola*® MPC998.
- Agere Systems Inc. chip has expanded frequency range and improved performance:
  — MPC998 range is 520 MHz—840MHz.
  — LCK4801 range is 336 MHz—1 GHz.

Description

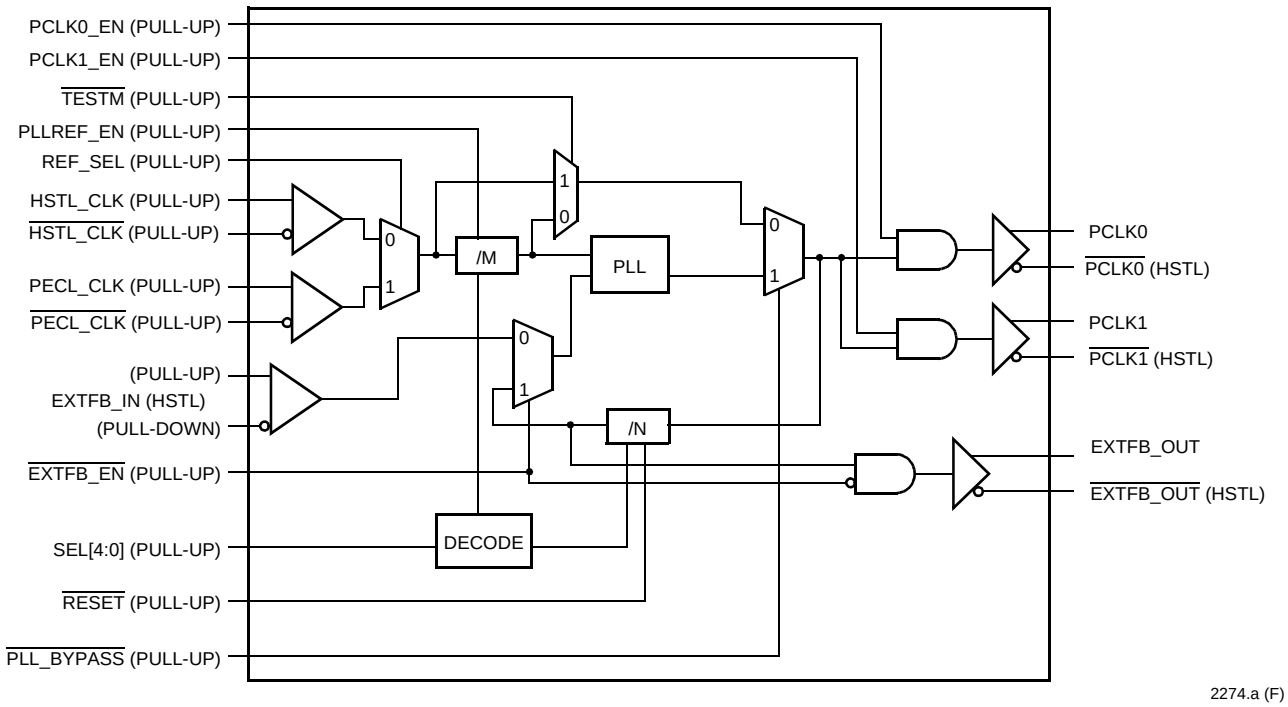

Figure 1. LCK4801 Logic Diagram

Description (continued)

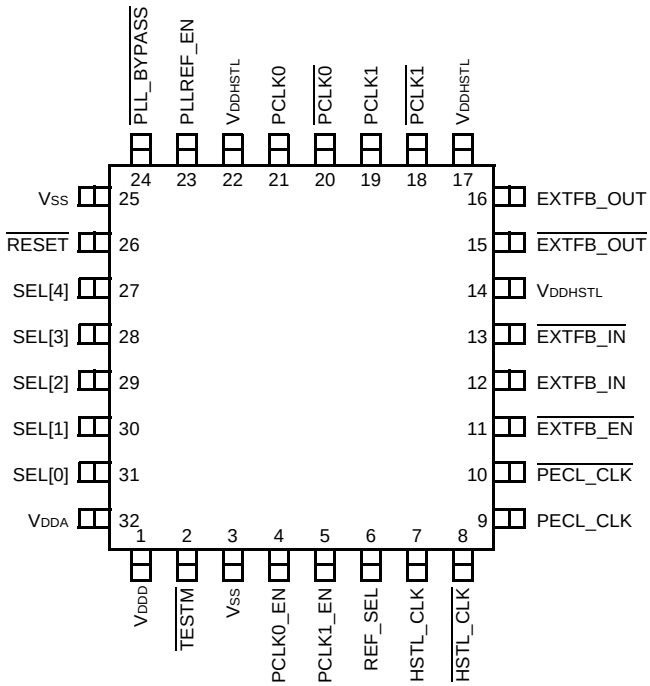

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Figure 2. 32-Pin TQFP

Pin Information

Table 1. Pin Description

Pin Number	Pin Name	I/O[1]	Type	Description
1	V_{DDD}	P	Power Supply	3.3 V power supply.
2	$\overline{\text{TESTM}}$	I	LVCMOS	M divider test pins.
3	V_{SS}	G	Ground	Digital ground.
4	PCLK0_EN	I	LVCMOS	PCLK0 enable.
5	PCLK1_EN	I	LVCMOS	PCLK1 enable.
6	REF_SEL	I	LVCMOS	Selects the PLL input reference clock.
7	HSTL_CLK	I	Differential HSTL	PLL reference clock input.
8	$\overline{\text{HSTL\_CLK}}$	I	Differential HSTL	PLL reference clock input.
9	PECL_CLK	I	Differential LVPECL	PLL reference clock input.
10	$\overline{\text{PECL\_CLK}}$	I	Differential LVPECL	PLL reference clock input.
11	$\overline{\text{EXTFB\_EN}}$	I	LVCMOS	External feedback enable.
12	EXTFB_IN	I	Differential HSTL	External feedback input.
13	$\overline{\text{EXTFB\_IN}}$	I	Differential HSTL	External feedback input.
14	V_{DDHSTL}	P	Power Supply	Output buffers power supply.
15	$\overline{\text{EXTFB\_OUT}}$	O	Differential HSTL	External feedback output clock.
16	EXTFB_OUT	O	Differential HSTL	External feedback output clock.
17	V_{DDHSTL}	P	Power Supply	Output buffers power supply.
18	$\overline{\text{PCLK1}}$	O	Differential HSTL	Output clock 1.
19	PCLK1	O	Differential HSTL	Output clock 1.
20	$\overline{\text{PCLK0}}$	O	Differential HSTL	Output clock 0.
21	PCLK0	O	Differential HSTL	Output clock 0.
22	V_{DDHSTL}	P	Power Supply	Output buffers power supply.
23	PLLREF_EN	I	LVCMOS	PLL reference enable.
24	$\overline{\text{PLL\_BYPASS}}$	I	LVCMOS	Input signal PLL bypass.
25	V_{SS}	P	Ground	Analog ground for PLL.
26	$\overline{\text{RESET}}$	I	LVCMOS	PLL bypass reset (for test use).
27	SEL[4]	I	LVCMOS	Selection of input and feedback frequency.
28	SEL[3]	I	LVCMOS	Selection of input and feedback frequency.
29	SEL[2]	I	LVCMOS	Selection of input and feedback frequency.
30	SEL[1]	I	LVCMOS	Selection of input and feedback frequency.
31	SEL[0]	I	LVCMOS	Selection of input and feedback frequency.
32	V_{DDA}	P	Power Supply	3.3 V filtered for PLL (PLL power supply).

1. P = power, I = input, G = ground, O = output.

Pin Information (continued)

Table 2. Frequency Selection

Selection					Input Divide	Feedback Divide	PCLK (MHz) for Given Input Frequency (MHz)			
4	3	2	1	0	M	N	70	100	120	125
0	0	0	0	0	5	24	336	480	576	600
0	0	0	0	1	5	25	350	500	600	625
0	0	0	1	0	5	26	364	520	624	650
0	0	0	1	1	5	27	378	540	648	675
0	0	1	0	0	5	28	392	560	672	700
0	0	1	0	1	5	29	406	580	696	725
0	0	1	1	0	5	30	420	600	720	750
0	0	1	1	1	5	31	434	620	744	775
0	1	0	0	0	5	32	448	640	768	800
0	1	0	0	1	5	33	462	660	792	825
0	1	0	1	0	5	34	476	680	816	850
0	1	0	1	1	5	35	490	700	840	875
0	1	1	0	0	5	36	504	720	864	900
0	1	1	0	1	5	37	518	740	888	925
0	1	1	1	0	5	38	532	760	912	950
0	1	1	1	1	5	39	546	780	936	975
1	0	0	0	0	5	40	560	800	960	1000
1	0	0	0	1	5	41	564	820	984	NA
1	0	0	1	0	5	42	588	840	NA	NA
1	0	0	1	1	5	43	602	860	NA	NA
1	0	1	0	0	5	44	616	880	NA	NA
1	0	1	0	1	5	45	630	900	NA	NA
1	0	1	1	0	5	46	644	920	NA	NA
1	0	1	1	1	5	47	658	940	NA	NA
1	1	0	0	0	5	48	672	960	NA	NA
1	1	0	0	1	5	49	686	980	NA	NA
1	1	0	1	0	5	50	700	1000	NA	NA
1	1	0	1	1	5	51	714	NA	NA	NA
1	1	1	0	0	5	52	728	NA	NA	NA
1	1	1	0	1	5	53	742	NA	NA	NA
1	1	1	1	0	5	54	756	NA	NA	NA
1	1	1	1	1	5	55	770	NA	NA	NA

Pin Information (continued)

Table 3. Function Control

Control Pin	0	1
REF_SEL	HSTL_CLK.	PECL_CLK.
$\overline{\text{TESTM}}$	M divider test mode enabled.	Reference fed to bypass MUX.
PLLREF_EN	Disable the input to the PLL and reset the M divider.	Enable the input to the PLL.
$\overline{\text{PLL\_BYPASS}}$	Outputs fed by input reference or M divider.	Outputs fed by VCO.
$\overline{\text{EXTFB\_EN}}$	External feedback enabled.	Internal feedback enabled.
PCLK0_EN	PCLK0 = low, $\overline{\text{PCLK0}}$ = high.	PCLK0 = high, $\overline{\text{PCLK0}}$ = low.
PCLK1_EN	PCLK1 = low, $\overline{\text{PCLK1}}$ = high.	PCLK1 = high, $\overline{\text{PCLK1}}$ = low.
$\overline{\text{RESET}}$	Resets feedback N divider.	Feedback enabled.
SEL[4:0]	See Table 2 on page 4.	See Table 2 on page 4.

Absolute Maximum Characteristics

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Unit
Power Supply	V_{DDD}/V_{DDA}	–0.5	—	4.4	V
	V_{DDHSTL}	–0.5	—	4.4	
Input Voltage	V_{IN}	–0.5	—	V_{DDD} + 0.3	V
Write Current	I_{IN}	–1	—	1	mA
Storage Temperature	T_S	–50	—	150	°C

Electrical Characteristics

Table 5. dc Characteristics

V_{DDA} = V_{DDD} = 3.3 V ± 5%, V_{DDHSTL} = 1.7 V—2.1 V, T_A = 0 °C—70 °C.

Symbol	Description	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0	—	V_{DDD}	V	LVCMOS
V_{IL}	Input Low Voltage	0.0	—	0.8	V	LVCMOS
V_{CMR}	Input High Voltage[1]	1	—	V_{DDD} – 0.3	V	LVPECL
V_{PP}	Input Low Voltage[1]	0.5	—	1	V	LVPECL[2]
V_{IN} (dc)	dc Input Signal Voltage	–0.3	—	1.45	V	HSTL[3]
V_{DIF} (dc)	dc Differential Input Voltage	0.4	—	1.75	V	HSTL[4]
V_{CM} (dc)	dc Common Mode Input Voltage	0.4	—	1.0	V	HSTL[5]
V_{OH}	Output High Voltage	V_X + 0.3	V_X + 0.5	1.4	V	HSTL[6,1]
V_{OL}	Output Low Voltage	0	V_X – 0.5	V_X – 0.3	V	HSTL[6]
I_{DDI}	Core Supply Current	—		140	mA	—
I_{DDA}	PLL Supply Current	—	15	20	mA	—
I_{DDO}	Output Supply Current	—	150	—	mA	—[7]
$Theta_{JA}$	Junction to Ambient Thermal Resistance	—	53	—	°C/W	—[8]

1. dc levels will vary 1:1 with V_{DDD}.
2. V_{PP} characteristics required for ac specifications. Actual tolerance of V_{PP} is 200 mV.
3. V_{IN} (dc) specifies maximum dc excursion of each differential input.
4. The V_{DIF} (dc) minimum is calculated by V_{OH} – V_{OL}, where V_{OH} is the true input signal and V_{OL} is the complementary input signal.
5. V_{CM} specifies the maximum allowable voltage range of the input signal crosspoint.
6. V_X is the differential output crosspoint voltage (see Table 6 on page 7).
7. Two PCLK signals to 25 Ω, and one EXTFB signal through 50 Ω.
8. 1.3 M/s (250 fpm) airflow.

Electrical Characteristics (continued)

Table 6. ac Characteristics

V_{DDA} = V_{DDD} = 3.3 V ± 5%, V_{DDHSTL} = 1.7 V—2.1 V, T_A = 0 °C—70 °C.

Symbol	Description	Min	Typ	Max	Unit	Condition
fref	Input Frequency	—	70—125	—	MHz	—
fMAX	Maximum Output Frequency	336	—	1000	MHZ	—[1]
tsk (o)	Skew Error (PCLK)	—	—	35	ps	—[2]
$t_{jit\ (0)}$	Phase Jitter (I/O Jitter)	—	—	(output period)/2	—	—[2]
$t_{jit\ (cc)}$	Cycle-to-Cycle Jitter (Full Period)	—	—	5	%	—[2,3]
$t_{jit\ (1/2\ period)}$	Cycle-to-Cycle Jitter (Half Period)	—	—	8	%	—[2,4]
V_{DIFout}	Differential Output Peak-to-Peak Swing	0.6	—	—	V	For all HSTL output pairs.
V_X	Differential Output Crosspoint Voltage	0.68	—	0.9	V	For all HSTL output pairs.
t_{lock}	Maximum PLL Lock Time	—	—	10	ms	—

1. When the phase-locked loop is active but in bypass mode, fref maximum is limited by input the buffer; optimum performance is obtained from PECL input.
2. At differential pair crossover.
3. Full PCLK period.
4. Half PCLK period.

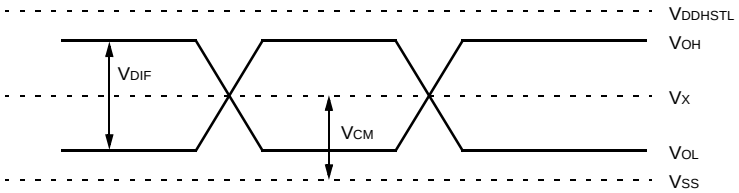

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Figure 3. HSTL Differential Input Levels

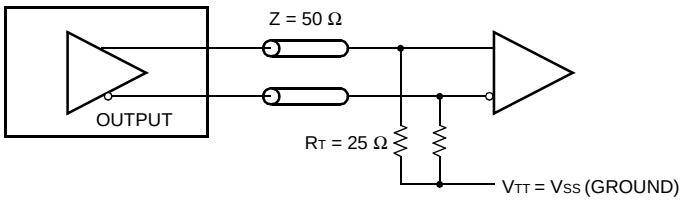

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Figure 4. Output Termination and ac Test Reference

Applications

Power Supply Filtering

The LCK4801 is a mixed analog/digital product. Because of this, it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is susceptible to random noise, the worst case being when this noise is seen on the power supply pins. The LCK4801 provides separate power supplies for the output buffers (V_{DDHSTL}) and the phase-locked loop (V_{DDA}) of the device in order to isolate the high digital output switching noise from the internal analog PLL. In a controlled evaluation board environment, this level of isolation is adequate. However, in a digital system, a second level of isolation is suggested.

The easiest way to accomplish this is to add a power supply filter on the V_{DDA} pin of the LCK4801. Figure 5 on page 9 shows the typical power supply scheme. The filter should be designed in the 10 kHz—1 MHz range, since this is the most likely frequency range to cause spectral content noise.

Note the dc voltage drop between V_{DDD} and V_{DDA} on the power supply filter. Very little dc voltage drop can be tolerated when a 3.3 V V_{DDD} supply is used. The power supply filter in Figure 5 must be 5 Ω—10 Ω in order to meet the drop criteria. The RC filter in Figure 5 will provide a broadband filter with approximately 100:1 attenuation above 20 kHz.

The impedance of an individual capacitor begins to appear inductive and increases with frequency as the noise frequency crosses the series resonant point of the capacitor. The parallel capacitor combination ensures that for frequencies much greater than the bandwidth of the PLL there is always a low-impedance path.

Applications (continued)

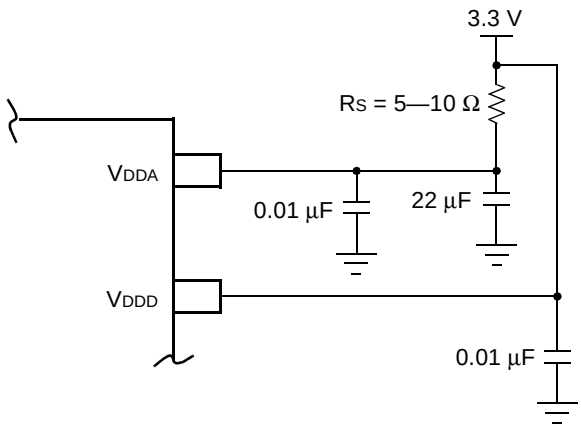

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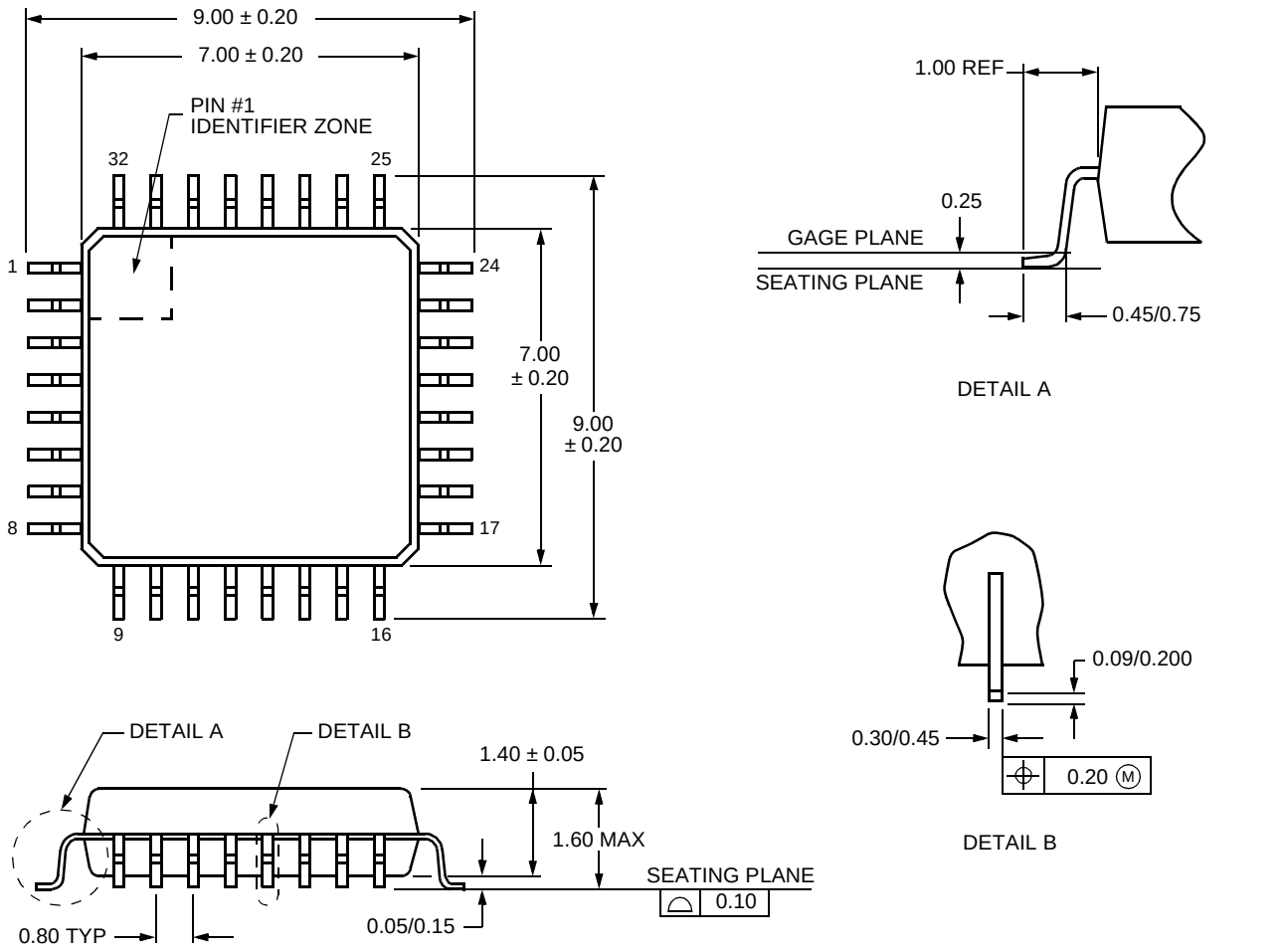
Figure 5. Power Supply Filter

Although the LCK4801 has an isolated power supply and grounds, as well as fully differential PLL, there still may be applications in which overall performance is being compromised due to system power supply noise. The power supply filter schemes discussed are adequate to eliminate power supply noise problems in most designs.

Outline Diagram

Dimensions are in millimeters.



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