agere systems

Data Sheet
June 2003

LCK4310
Low-Voltage PLL Clock Driver

Features

- Output operating frequencies up to 1.25 GHz max.
- 100 ps part–to–part skew.
- 40 ps typical output–to–output skew.
- Cycle-to-cycle jitter less than 7 ps max.
- 3.3 V and 2.5 V compatible.
- Internal input pulldown resistors.
- Q output will default low with inputs open or at V_{EE}.
- Meets or exceeds Joint Electron Device Engineering Council (JEDEC) specification *EIA*®/ JESD78 IC latchup test.
- Moisture sensitivity level 1.
- Flammability rating: *UL*®–94 code V–0 at 1/8 in., oxygen index 28 to 34.
- Pin-for-pin compatible with *ON Semiconductor*® part number MC100LVE310.

Description

The LCK4310 is a low-voltage, low-skew 2:8 differential emitter-coupled logic (ECL) fanout buffer designed with clock distribution in mind. The device features fully differential clock paths to minimize both device and system skew. The LCK4310 offers two selectable clock inputs to allow for redundant or test clocks to be incorporated into the system clock trees.

To ensure that the tight skew specification is met, it is necessary that both sides of the differential output are terminated into 50 Ω, even if only one side is being used. In most applications, all eight differential pairs will be used and therefore terminated. In the case where fewer than eight pairs are used and in order to maintain minimum skew, it is necessary to terminate at least the output pairs adjacent to the output pair being used. Failure to follow this guideline will result in small degradations of propagation delay (on the order of 10 ps—20 ps) of the outputs being used, while not catastrophic to most designs this will result in an increase in skew.

Note: The package corners isolate outputs from one another such that the guideline expressed above holds only for outputs on the same side of the package.

The LCK4310, as with most ECL devices, can be operated from a positive voltage supply (V_{DD}) in LVPECL mode. This allows the LCK4310 to be used for high performance clock distribution in 3.3 V/2.5 V systems. Designers can take advantage of the LCK4310's performance to distribute low-skew clocks across the backplane or the board. In a PECL environment (series or Thevenin), line terminations are typically used as they require no additional power supplies. If parallel termination is desired, a terminating voltage of V_{DD} – 2.0 V will need to be provided.

An internally generated voltage supply (V_{BB} pin) is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias ac coupled inputs. When used, decouple V_{BB} and V_{DD} via a 0.01 µF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

Pin Information

Pin Diagram

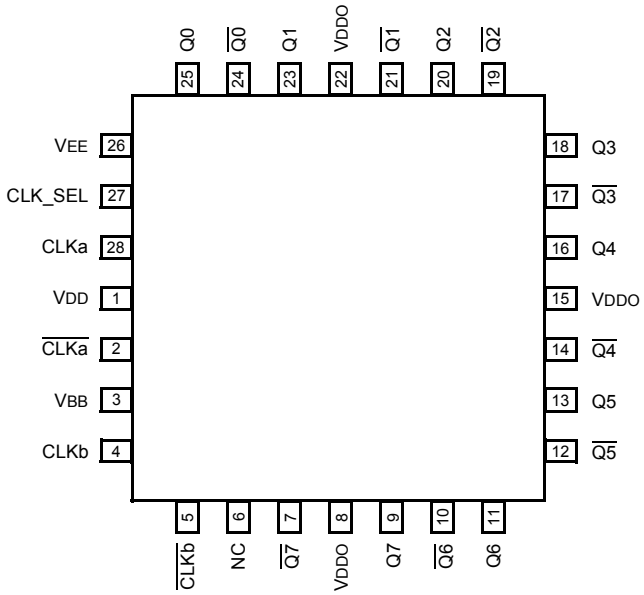


Figure 1. 28-Pin PLCC

WARNING: All V_{DD}, V_{DDO}, and V_{EE} pins must be externally connected to a power supply to guarantee proper operation.

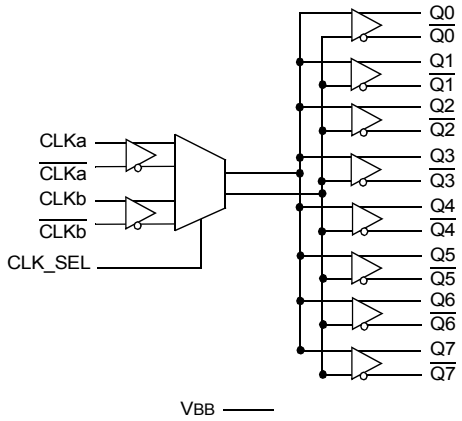
Pin Descriptions

Table 1. Pin Descriptions

Pin	Symbol	Type	I/O	Description
1	V_{DD}	Power	—	**Positive Power Supply.**
2	$\overline{CLKa}$	PECL	I	**ECL Differential Input Clock.** Makes input pair with CLKa.
3	V_{BB}	V_{REFOUT}	O	**Reference Voltage Output.**
4	CLKb	LVTTL	I	**ECL Differential Input Clock.** Makes input pair with $\overline{CLKb}$.
5	$\overline{CLKb}$	LVTTL	I	**ECL Differential Input Clock.** Makes input pair with CLKb.
6	NC	—	—	**No Connect.**
7, 10, 12, 14, 17, 19, 21, 24	$\overline{Q[7:0]}$	PECL	O	**ECL Differential Outputs.**
8, 15, 22	V_{DDO}	Power	—	**Positive Power Supply.**
9, 11, 13, 16, 18, 20, 23, 25	Q[7:0]	PECL	O	**ECL Differential Outputs.**
26	V_{EE}	Power	—	**Negative Power Supply.**
27	CLK_SEL	LVTTL	I	**ECL Input Clock Select.** 0 = CLKa selected. 1 = CLKb selected.
28	CLKa	LVTTL	I	**ECL Differential Input Clock.** Makes input pair with $\overline{CLKa}$.

Pin Information (continued)

Logic Symbol



CLK_SEL	Input Clock
L	CLKa/$\overline{\text{CLKa}}$ Selected
H	CLKb/$\overline{\text{CLKb}}$ Selected

Figure 2. Logic Symbol

Absolute Maximum Ratings

Stresses which exceed the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods of time can adversely affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min	Max	Unit
PECL Mode Positive Power Supply	V_{DD}	V_{EE} = 0 V	0	5	V
Input Voltage: PECL Mode Positive Input Voltage	V_I	V_{EE} = 0 V, $V_I \le V_{DD}$	0	5	V
Output Current	I_{OUT}	Continuous surge	50	100	mA
V_{BB} Sink/Source	I_{BB}	—	–0.5	0.5	mA
Storage Temperature Range	T_{stg}	—	–65	150	°C
Ambient Temperature	T_A	—	–40	85	°C
Thermal Resistance (junction to ambient)	θ_{JA}	0 LFPM, 28 PLCC 500 LFPM, 28 PLCC	— —	63.5 43.5	°C/W
Thermal Resistance (junction to case)	θ_{JC}	Standard board, 28 PLCC	22 ± 5%	26 ± 5%	°C/W
Wave Solder	T_{SOL}	<2 s to 3 s at 248 °C	—	265	°C

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Agere Systems employs a human-body model (HBM) and charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in the defined model. No industrywide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes.

Table 3. ESD Protection Characteristics

Device	Minimum Threshold
	HBM
LCK4310	>2,000 V

Electrical Characteristics

dc Characteristics

Table 4. LVPECL 3.3 V dc Characteristics

V_{DD} = 3.3 V, V_{EE} = 0 V. Input and output parameters vary 1:1 with V_{DD}. V_{EE} can vary ±0.3 V. Devices are designed to meet the dc specifications shown in Table 4 below, after thermal equilibrium has been established.

Parameter	Symbol	–40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Power Supply Current	I_{EE}	—	55	60	—	55	60	—	65	70	mA
Output High Voltage*	V_{OH}	2,215	2,295	2,420	2,275	2,345	2,420	2,275	2,345	2,420	mV
Output Low Voltage*	V_{OL}	1,470	1,605	1,745	1,490	1,595	1,680	1,490	1,595	1,680	mV
Input High Voltage (single-ended)	V_{IH}	2,135	—	2,420	2,135	—	2,420	2,135	—	2,420	mV
Input Low Voltage (single-ended)	V_{IL}	1,490	—	1,825	1,490	—	1,825	1,490	—	1,825	mV
Output Voltage Reference	V_{BB}	1.92	—	2.06	1.92	—	2.06	1.92	—	2.06	V
Input High Voltage Common-mode Range (differential)†	V_{IHCMR}	1.8	—	2.9	1.8	—	2.9	1.8	—	2.9	V
Input High Current	I_{IH}	—	—	150	—	—	150	—	—	150	µA
Input Low Current	I_{IL}	0.5	—	—	0.5	—	—	0.5	—	—	µA

* Outputs are terminated through a 50 Ω resistor to V_{DD} – 2 V.
† V_{IHCMR} minimum varies 1:1 with V_{EE}, maximum varies 1:1 with V_{DD}. V_{IHCMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0 V and greater than or equal to $V_{p\text{-}pmin}$.

Electrical Characteristics (continued)

dc Characteristics (continued)

Table 5. LVPECL 2.5 V dc Characteristics

V_{DD} = 2.5 V, V_{EE} = 0 V. Input and output parameters vary 1:1 with V_{DD}. V_{EE} can vary ±0.3 V. Devices are designed to meet the dc specifications shown in Table 5 below, after thermal equilibrium has been established.

Parameter	Symbol	–40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Power Supply Current	I_{EE}	—	55	60	—	55	60	—	65	70	mA
Output High Voltage*	V_{OH}	1425	1495	1620	1425	1507	1620	1425	1520	1620	mV
Output Low Voltage*	V_{OL}	730	790	955	730	820	955	730	825	955	mV
Input High Voltage (single-ended)	V_{IH}	2000	—	2400	2000	—	2400	2000	—	2400	mV
Input Low Voltage (single-ended)	V_{IL}	400	—	1030	400	—	1030	400	—	1030	mV
Output Voltage Reference	V_{BB}	1.019	—	1.361	1.019	—	1.361	1.019	—	1.361	V
Input High Voltage Common-mode Range (differential)†	V_{IHCMR}	1.0	—	2.1	1.0	—	2.1	1.0	—	2.1	V
Input High Current	I_{IH}	—	—	150	—	—	150	—	—	150	µA
Input Low Current	I_{IL}	0.5	—	—	0.5	—	—	0.5	—	—	µA

* Outputs are terminated through a 50 Ω resistor to V_{DD} – 2 V.
† V_{IHCMR} minimum varies 1:1 with V_{EE}, maximum varies 1:1 with V_{DD}. V_{IHCMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0 V and greater than or equal to $V_{p\text{-}pmin}$.

Electrical Characteristics (continued)

ac Characteristics

V_{DD} = 3.3/2.5 V, V_{EE} = 0 V, or V_{DD} = 0 V, V_{EE} = –3.3/2.5 V. V_{EE} can vary ±0.3 V.

Table 6. ac Characteristics

Parameter	Symbol	–40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Maximum Toggle Frequency	f_{MAX}	—	—	1.25	—	—	1.25	—	—	1.25	GHz
Propagation Delay to Output:											ps
In (differential)*	t_{PLH}	525	—	725	550	—	750	575	—	775	
In (single-ended)†	t_{PHL}	500	—	750	550	—	800	600	—	850	
Within Device Skew‡	t_{SKEW}	—	—	40	—	—	40	—	—	40	ps
Part-to-part Skew‡ (differential)	t_{SKEW}	—	—	100	—	—	100	—	—	100	ps
Cycle-to-cycle Jitter	t_{JITTER}	—	—	7	—	—	7	—	—	7	ps
Input Swing§	V_{p-p}	500	—	1,000	500	—	1,000	500	—	1,000	mV
Output Rise/Fall Time (20%—80%)	t_r/t_f	200	—	600	200	—	600	200	—	600	ps

* The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
† The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
‡ The within device skew is defined as the worst case difference between any two similar delay paths within a single device.
§ V_{p-pmin} is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{p-pmin} is ac limited for the LCK4310 as a differential input as low as 50 mV will still produce full ECL levels at the output.

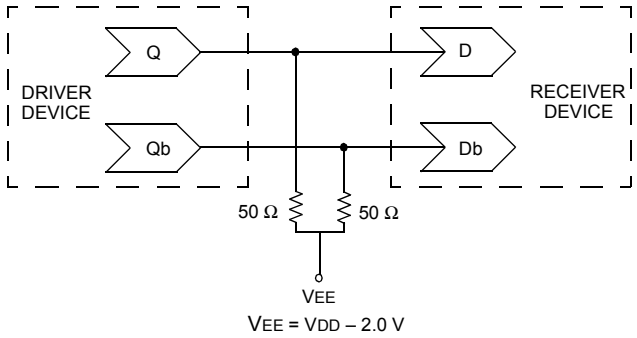
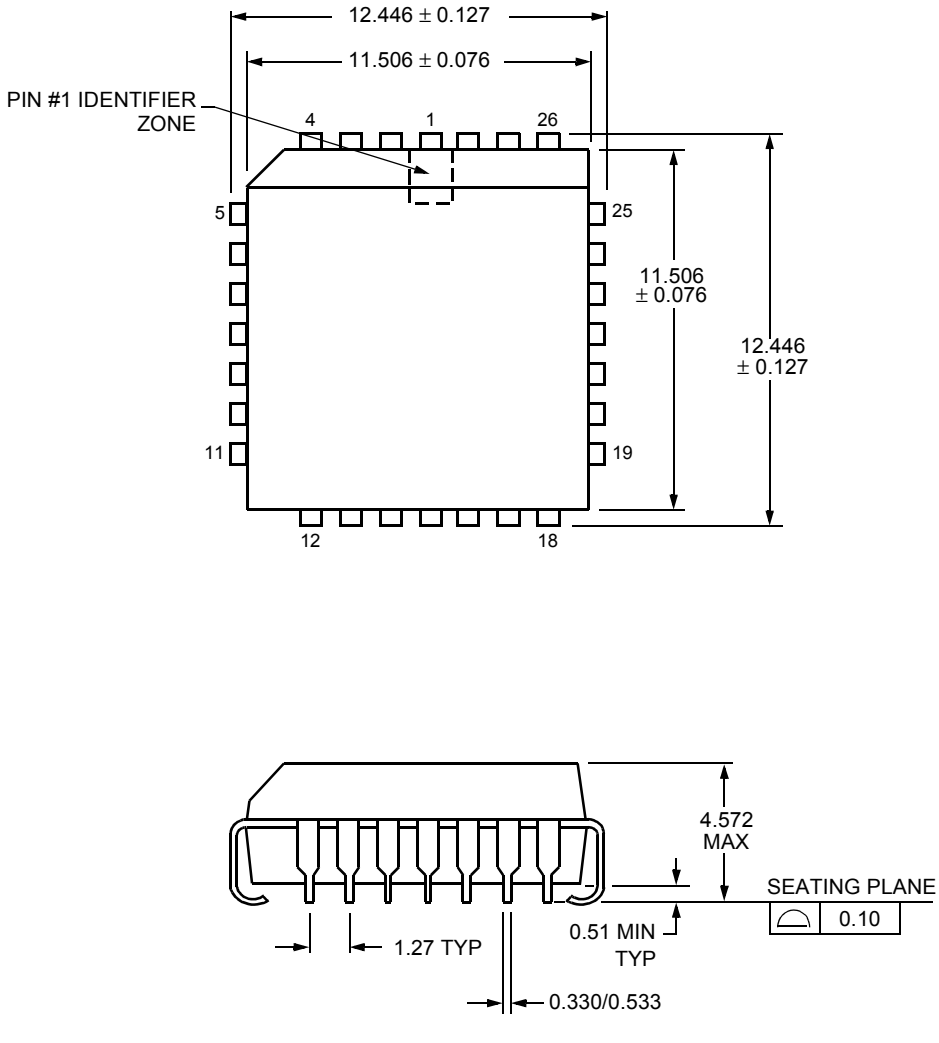


Figure 3. Typical Termination for Output Driver and Device Evaluation

Outline Diagrams

Dimensions are in millimeters.



5-2608 (F)

Ordering Information

Device	Part Number	Pin Count	Package	Type	Comcode
LCK4310	LCK4310GF-DB	28	PLCC	Reel	700020216
	LCK4310GF-DT	28	PLCC	Tape	700020217

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June 2003
DS03-158LCK (Replaces DS02-144LCK)