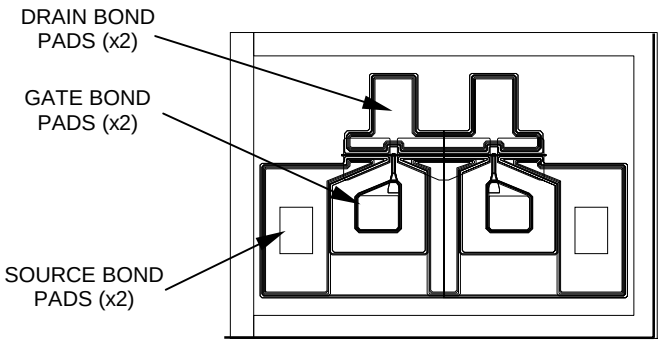
Filtronic LP7612

Solid State

High Dynamic Range PHEMT

FEATURES

- **+21 dBm Typical Power at 18 GHz**
- **9.5 dB Typical Power Gain at 18 GHz**
- **1.0 dB Typical Noise Figure at 18 GHz**
- **Low Intermodulation Distortion**
- **55% Power-Added-Efficiency at 18 GHz**



DIE SIZE: 18 x 13 mils (460 x 330 µm)
DIE THICKNESS: 3.9 mils typ. (100 µm typ.)
BONDING PADS: 1.9 x 1.9 mils (50 x 50 µm typ.)

DESCRIPTION AND APPLICATIONS

The LP7612 is an Aluminum Gallium Arsenide / Indium Gallium Arsenide (AlGaAs/InGaAs) Pseudomorphic High Electron Mobility Transistor (PHEMT), utilizing an Electron-Beam direct-write 0.25 µm by 200 µm Schottky barrier gate. The recessed "mushroom" gate structure minimizes parasitic gate-source and gate resistances. The epitaxial structure and processing have been optimized for high dynamic range. The LP7612 also features Si_3N_4 passivation and is available in a 70 mil ceramic (P70) and the SOT-23.

Typical applications include high dynamic range receiver preamplifiers for commercial applications including Cellular/PCS systems, broad bandwidth commercial instrumentation, military EW amplifiers, and commercial Space applications.

The LP7612 may be procured in a variety of grades, depending upon specific user requirements. Standard lot screening is patterned after MIL-STD-19500, JANC grade. Space-level screening to FSS JANS grade is also available.

PERFORMANCE SPECIFICATIONS (T_A = 25°C)

SYMBOLS	PARAMETERS		MIN	TYP	MAX	UNITS
I_{DSS}	Saturated Drain-Source Current V_{DS} = 2V V_{GS} = 0V		40	65	65	mA
P_{1dB}	Output Power at 1dB Gain Compression at V_{DS} = 5.0V, I_{DS} = 50% I_{DSS}	*f* = 18 GHz	19.0	21		dBm
G_{1dB}	Power Gain at 1dB Gain Compression at V_{DS} = 5.0V, I_{DS} = 50% I_{DSS}	*f* = 18 GHz	8.0	9.5		dB
η_{ADD}	Power-Added Efficiency			55		%
I_{MAX}	Maximum Drain-Source Current	V_{DS} = 2V V_{GS} = +1V		125		mA
G_M	Transconductance	V_{DS} = 2V V_{GS} = 0V	60	90		mS
V_P	Pinch-Off Voltage	V_{DS} = 2V I_{DS} = 1mA	-0.25	-0.8	-1.5	V
I_{GSO}	Gate-Source Leakage Current	V_{GS} = -5V		1	10	µA
BV_{GS}	Gate-Source Breakdown Voltage	I_{GS} = 1mA	-6	-7		V
BV_{GD}	Gate-Drain Breakdown Voltage	I_{GD} = 1mA	-8	-9		V
Θ_J	Thermal Resistivity (V_{DS} = 5.5V)			275		°C/W

DSS-036 WF

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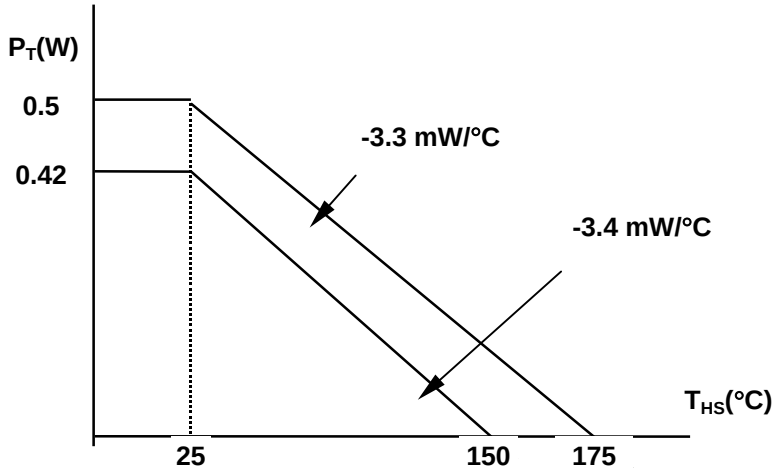
ABSOLUTE MAXIMUM RATINGS (25°C)		
SYMBOL	**PARAMETER**	**RATING[1]**
V_{DS}	Drain-Source Voltage	8V
V_{GS}	Gate-Source Voltage	-3V
I_{DS}	Drain-Source Current	2 x I_{DSS}
I_G	Gate Current	10 mA
P_{IN}	RF Input Power	100 mW
T_{CH}	Channel Temperature	175°C
T_{STG}	Storage Temperature	-65/175°C
P_T	Power Dissipation	500mW[3,4]

RECOMMENDED CONTINUOUS OPERATING LIMITS		
SYMBOL	**PARAMETER**	**RATING[2]**
V_{DS}	Drain-Source Voltage	5V
V_{GS}	Gate-Source Voltage	-0.8V
I_{DS}	Drain-Source Current	0.85 x I_{DSS}
I_G	Gate Current	2 mA
P_{IN}	RF Input Power	50 mW
T_{CH}	Channel Temperature	150°C
T_{STG}	Storage Temperature	-20/50°C
P_T	Power Dissipation	415 mW[3,4]
G_{XdB}	Gain Compression	7 dB

NOTES:

1. Operating conditions that exceed the Absolute Maximum Ratings could result in permanent damage to the device.
2. Recommended Continuous Operating Limits should be observed for reliable device operation.
3. Power Dissipation defined as: $P_T \equiv (P_{DC} + P_{IN}) - P_{OUT}$, where: P_{DC} = DC bias power, P_{OUT} = RF output power, and P_{IN} = RF input power.
4. Power Dissipation to be de-rated as follows:
5. Specifications subject to change without notice.



Example #1:
V_{DS} = 5V, I_{DS} = 45 mA
$P_{IN} = P_{OUT}$ = 0 dBm (quiescent condition):
$P_T = P_{DC}$ = 0.23W
Max. continuous T_{HS} = 83°C

Example #2:
V_{DS} = 5V, I_{DS} = 45 mA
P_{IN} = 11.5 dBm P_{OUT} = 21 dBm
P_T = (0.23+0.01) - 0.126 = 0.114W
Max. continuous T_{HS} = 116°C

HANDLING PRECAUTIONS:

PHEMT chips should be stored in a dry nitrogen environment until assembly. Care should be exercised during handling to avoid damage to the devices. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 1A (0-500V), and further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

ASSEMBLY INSTRUCTIONS:

The recommended die attach is gold/tin eutectic solder under a nitrogen atmosphere. Stage temperature should be 280-290°C; maximum time at temperature is 1 min. The recommended wire bond method is thermo-compression wedge bonding with 0.7 or 1.0 mil (0.018 or 0.025 mm) gold wire. Stage temperature should be 250-260°C.

APPLICATIONS NOTES AND DESIGN DATA:

Applications Notes are available from your local FSS Sales Representative, or directly from the factory. Complete design data, including S-parameters, Noise data, and Large-Signal models, is available on 3.5" diskette, or may be down-loaded from our Web Page.

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