10/100 BASE-TX "LAN-MATE"
P/N: LU1S114A DATA SHEET

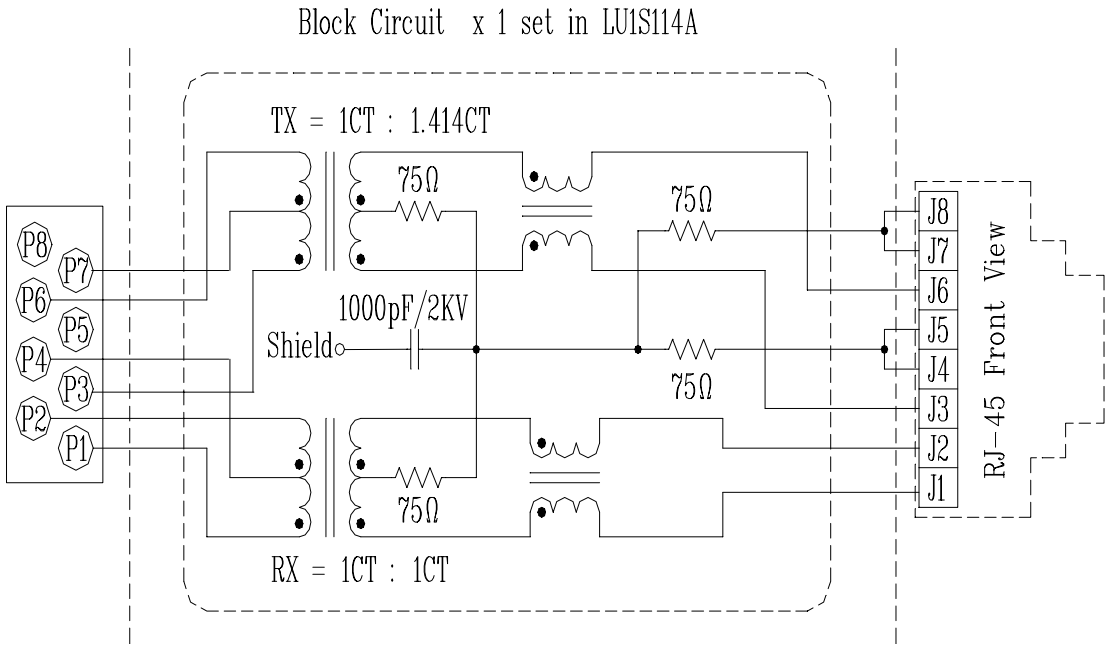
A. GENERAL SPECIFICATIONS:

1.DESIGNED FOR HUB APPLICARION.
2.DESIGNED TO MEET IEEE.802.3U REQUIREMENT.
3.AVAILABLE IN ALL TUM RATIOS USCD BY LAN IC MANUFACTURCS.
4.PRIMATY CENTER TAPS AVAILABLE FOR ADDITIONAL EMI REDUCTION.
5.SIMPLEST MAGNETIC COMPONENT TO PLACE AND ROUTE ON PCB,
6.CONSERVES MINIMIZING PCB SPACE.

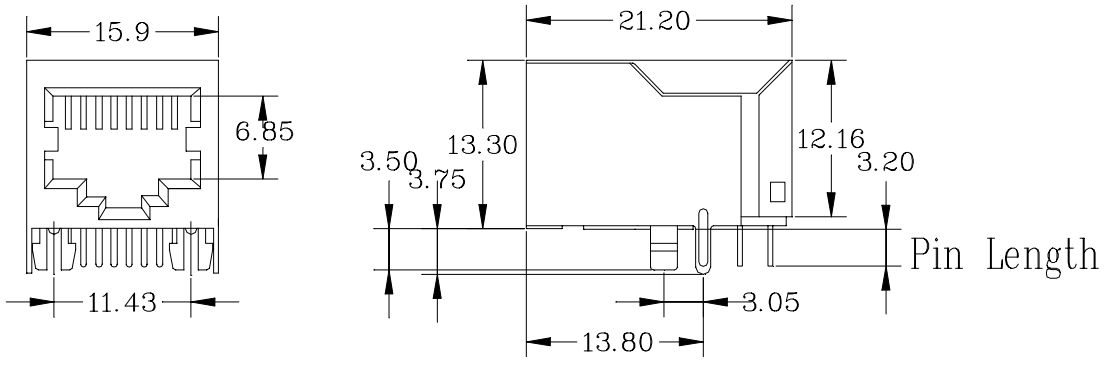
B. ELECTRICAL SPECIFICATIONS: (25°C)

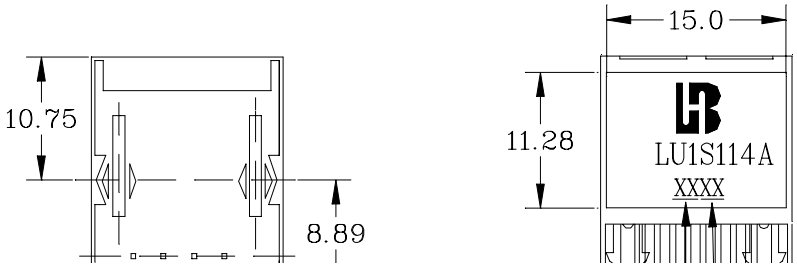
1.TURN RATIOS (±5%): RX =1CT: 1CT & TX=1CT: 1.414CT
2.PRIMARY OCL INDUCTANCE: 350 μH MIN AT 0.2 Vrms/100 KHz, 8.0mA Bias
3.C W/W: 28 pF MAX.
4.LEAKAGE INDUCTANCEAT 1 MHz: RX=0.5 μH MAX, TX=0.8 μH MAX
5.HI-POT ISOLATION (100% TEST): 1500 Vrms/0.5mA 1Sec.
6.INSERTION LOSS (0.1 TO 100 MHz): –1.15 dB MAX
7.RETURN LOSS (dB MIN): 30MHz 40MHz 50MHz 60MHz 80MHz
-16 -14 -13.5 -13 -10
8.CMRR (dB MIN): -30 (FREQUENCY 1-100MHz)
9.CROSS TALK (dB MIN): -35 (FREQUENCY: 1-80 MHz)

C. SCHEMATIC:



D:MECHNICAL DIMENSION(Unit mm)：





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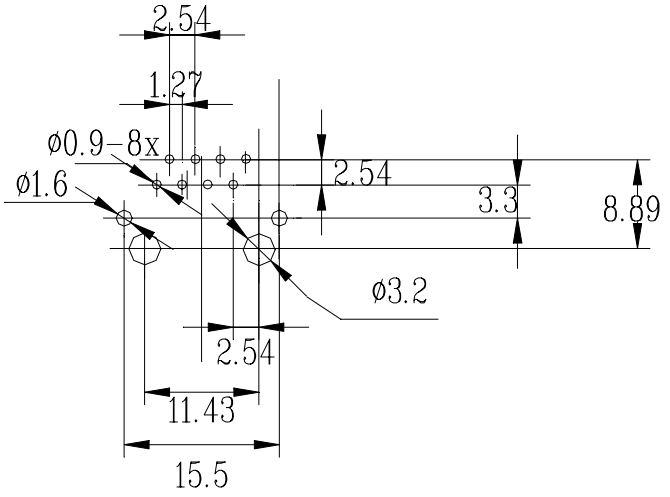
1.Plastic Material : PBT 15% Glass Filled (UL 94V-0) , Black Housing
2.Metal Shield : Brass C2680-H, 20u Nickle Plated, t=0.25mm
3.Spring Wire : 0.45mm Dia. Phosphor bronze with 6u gold plated .
4.Solder Pin : 0.4*0.4mm ,Phosphor bronze with Solder plated .
5.Durability : 300 Mating cycles Min .

E. PCB LAYOUT MOUNTING HOLE (Top View)



Unit: mm
Tolerance : ± 0.25