LSI403LP Digital Signal Processor

ZSP DSP Freedom™

ZSP™ ARCHITECTURE PERFORMANCE WITH LOW POWER CONSUMPTION

OVERVIEW

The LSI403LP is an extremely low power 16-bit fixed-point digital signal processor (DSP) based on the LSI Logic ZSP400 DSP core, running less than 250µW per DSP MIP (MMAC). The device has been designed for applications requiring high throughput and flexibility coupled with a high speed I/O, such as Voice over Packet CPE devices and consumer audio applications. The LSI403LP is capable of a maximum clock rate of 150 MHz for 600 MIPS peak performance and sustained effective throughput of 300 DSP MIPS (MMACs). The device is also software compatible with all other products in the ZSP architecture, and offers an unrivalled combination of code density, performance and ease of use.

MEMORY

The internal memory structure of the LSI403LP comprises of 16K words of instruction memory, 16K words of data memory, 16K words of configurable memory for instruction or data, 1K words of memory for bootloading and interrupt support and peripherals. Additionally, the external memory interface unit interfaces the LSI403LP to external memory devices. Both asynchronous and synchronous devices are supported. The external memory is logically segmented into instruction, data, and peripheral spaces.

DMA

The DMA controller of the LSI403LP supports zero-overhead instruction or data transfers to or from the entire 48K words of internal RAM to the memory interface unit, host processor interface, or a serial port. The eight DMA channels are segmented between four “indexed” and four “non-indexed” channels. Indexed channels have the ability to buffer data from either of the serial TDM interfaces, and non-indexed channels perform sequential accesses to or from internal memory. All DMA channels feature an auto-reload capability to restart transfers with no processor overhead.

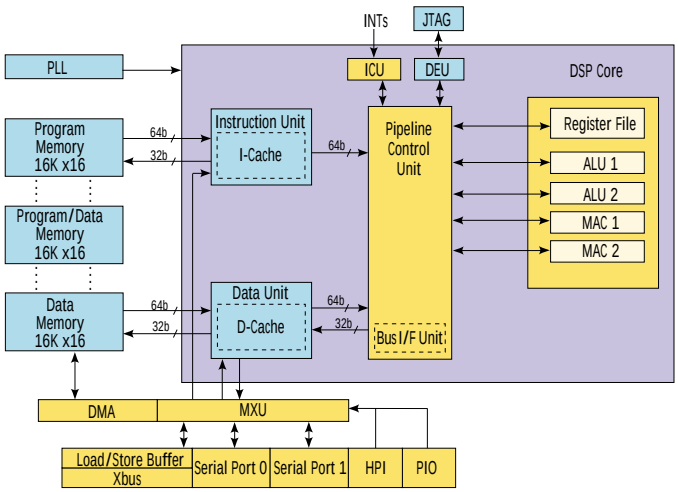

Figure 1. LSI403LP Functional Block Diagram

FEATURES

- 150 MHz operation at 1.2V
- 2 high-speed serial/TDM ports (T1/E1 framer, H.100/H.110 bit stream compatible)
- Low power dissipation (70mW typical at 150 MHz)
- Sleep power mode consumes <30µW/MHz
- 48K words on-chip RAM
- 8-channel DMA controller
- On-board PLL for clock generation
- 32-/16-bit external memory interface
- 2 on-board timers
- 8-bit host processor interface with hardware byte pack/unpack
- IEEE 1149.1-compliant JTAG port for in-system debug
- 208 PQFP package
- Available in 120 or 150 MHz versions

BENEFITS

- 300 MMAC sustained DSP performance at 150 MHz
- Direct interfacing to standard telecommunications interfaces, reducing system cost
- Low power per voice or audio channel
- Suitable for very low power applications
- High data throughput without processor overhead
- Flexibility to optimize power consumption
- High data bandwidth to off-chip devices
- Simple interfacing to industry-standard micros
- Low overhead on chip debug
- Ideal for low-cost IAD/MTA designs

LSI LOGIC

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TIMERS

The LSI403LP has two identical 16-bit on board timers for real-time interrupt generation. Each timer is fully programmable, and has a 6-bit prescaler and interrupt capability. The timers can automatically reload with the initial count so that periodic interrupts can be generated.

TDM SERIAL PORTS

The LSI403LP provides two identical synchronous serial ports that support 8- or 16-bit active or passive transfers, which can be either burst or continuous, with a maximum clock speed of one-half the processor clock. Both serial ports support mu- and A-law hardware companding and provide the programmable feature of a TDM (time division multiplex) mode that is compatible with T1/E1 framers or the local serial bus of H.100/H.110 interface devices. The TDM mode can also be used to establish a serial multiprocessor communication link with only three signals.

HOST PROCESSOR INTERFACE (HPI)

The Host Processor Interface, or HPI, is an asynchronous 8-bit parallel port that is used to interface with off-chip devices. It is compatible with both Motorola and Intel style memory interfaces, and supports word transfers. The maximum transfer rate for the HPI is one-third of the processor clock frequency. The HPI includes hard support to pack/unpack bytes to/from 16-bit words, removing the overhead of this task from the ZSP400 core.

DEVELOPMENT TOOLS

The LSI403LP is fully supported by both LSI Logic and 3rd party commercial tools. LSI Logic provides a GNU-based compiler, linker, and assembler available for Windows and Solaris platforms. The compiler supports C fixed-point data types and employs a variety of C intrinsic functions. Also supported is the MULTI® development environment from Green Hills Software. The ZSP architecture enables the C compiler to produce code unrivaled in code density and execution speed by any DSP in its class, offering a fast time to market with optimal performance and cost. JTAG-based, in-circuit debug can be performed using emulation interfaces from Corelis, Green Hills or Macraigor.

A LSI403LP development board is available, offering the following features:

- JTAG and serial port debug interfaces
- Two daughter module sites (Two, 16-bit stereo audio codecs supplied)
- Support for up to 8 voice channels via FXS daughter modules
- Flash memory (256K words)
- Parallel port interface to PC host
- SBSRAM and asynchronous expansion RAM (128K words each)

For more information please call:

LSI Logic Corporation
North American Headquarters
Milpitas, CA
Tel: 800 574 4286

LSI Logic Europe Ltd.
European Headquarters
United Kingdom
Tel: 44 1344 426544
Fax: 44 1344 481039

LSI Logic KK Headquarters
Tokyo, Japan
Tel: 81 3 5463 7165
Fax: 81 3 5463 7820

LSI Logic web site
www.lsilogic.com

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