



LP62S16256F-T Series

Preliminary

256K X 16 BIT LOW VOLTAGE CMOS SRAM

Document Title

256K X 16 BIT LOW VOLTAGE CMOS SRAM

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Issue Date</u>	<u>Remark</u>
0.3	Change operation voltage from 2.7V~3.3V to 2.7V~3.6V Add -55ns specification	November 22, 2002	Preliminary
0.4	Change Icc2 from 15mA to 8mA	April 18, 2003	



LP62S16256F-T Series

Preliminary

256K X 16 BIT LOW VOLTAGE CMOS SRAM

Features

- Operating voltage: 2.7V to 3.6V
- Access times: 55ns / 70ns (max.)
- Current:
 - Very low power version: Operating: 40mA (max.)
 - Standby: 10 μ A (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Data retention voltage: 2.0V (min.)
- Available in 44-pin TSOP and 48-ball CSP (6 $\times$ 8mm) packages

General Description

The LP62S16256F-T is a low operating current 4,194,304-bit static random access memory organized as 262,144 words by 16 bits and operates on low power voltage from 2.7V to 3.6V. It is built using AMIC's high performance CMOS process.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

The chip enable input is provided for POWER-DOWN, device enable. Two byte enable inputs and an output enable input are included for easy interfacing.

Data retention is guaranteed at a power supply voltage as low as 2.0V.

Product Family

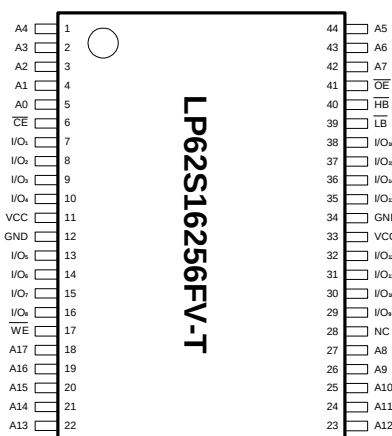
Product Family	Operating Temperature	VCC Range	Speed	Power Dissipation			Package Type
				Data Retention (I _{CCDR} , Typ.)	Standby (I _{SB1} , Typ.)	Operating (I _{CC2} , Typ.)	
LP62S16256F-T	-25°C ~ +85°C	2.7V~3.6V	55ns / 70ns	0.08 μ A	0.3 μ A	5mA	44L TSOP 48B CSP

1. Typical values are measured at VCC = 3.0V, T_A = 25°C and not 100% tested.

2. Data retention current VCC = 2.0V.

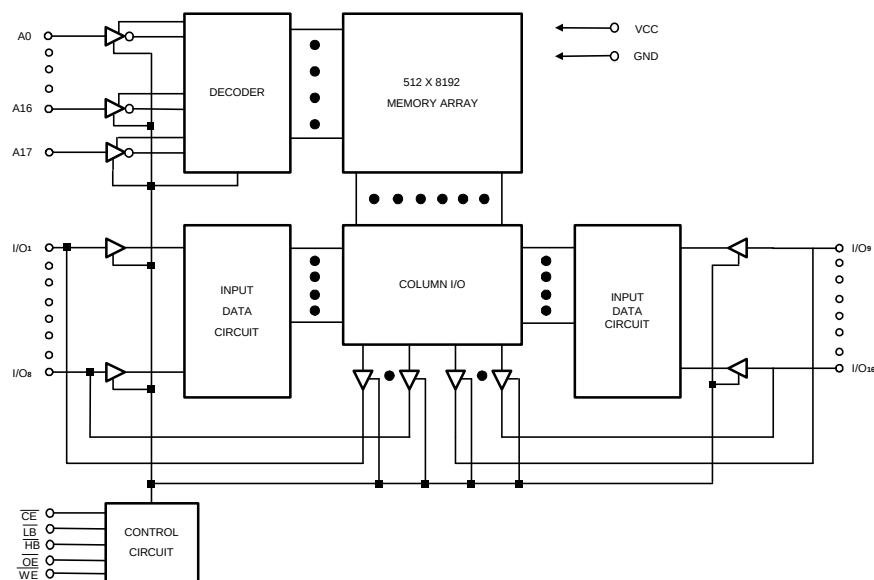
Pin Configurations

■ TSOP



■ CSP (Chip Size Package) 48-pin Top View

	1	2	3	4	5	6
A	LB	OE	A0	A1	A2	NC
B	I/O ₉	HB	A3	A4	CE	I/O ₁
C	I/O ₁₆	I/O ₁₁	A5	A6	I/O ₂	I/O ₃
D	GND	I/O ₁₂	A17	A7	I/O ₄	VCC
E	VCC	I/O ₁₃	NC	A16	I/O ₅	GND
F	I/O ₁₅	I/O ₁₄	A14	A15	I/O ₆	I/O ₇
G	I/O ₁₈	NC	A12	A13	WE	I/O ₈
H	NC	A8	A9	A10	A11	NC

Block Diagram

Pin Descriptions -- TSOP

Pin No.	Symbol	Description
1 - 5, 18 - 27, 42 - 44	A0 - A17	Address Inputs
6	$\overline{CE}$	Chip Enable Input
7 - 10, 13 - 16, 29 - 32, 35 - 38	I/O ₁ - I/O ₁₆	Data Inputs/Outputs
17	$\overline{WE}$	Write Enable Input
39	$\overline{LB}$	Lower Byte Enable Input (I/O ₁ to I/O ₈)
40	$\overline{HB}$	Higher Byte Enable Input (I/O ₉ to I/O ₁₆)
41	$\overline{OE}$	Output Enable Input
11, 33	VCC	Power
12, 34	GND	Ground
28	NC	No Connection

Pin Description - CSP

Symbol	Description	Symbol	Description
A0 - A17	Address Inputs	$\overline{\text{HB}}$	Higher Byte Enable Input (I/O ₉ - I/O ₁₆)
$\overline{\text{CE}}$	Chip Enable	$\overline{\text{OE}}$	Output Enable
I/O ₁ - I/O ₁₆	Data Input/Output	VCC	Power Supply
$\overline{\text{WE}}$	Write Enable Input	GND	Ground
$\overline{\text{LB}}$	Byte Enable Input (I/O ₁ - I/O ₈)	NC	No Connection

Recommended DC Operating Conditions

(T_A = -25°C to + 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	2.7	3	3.6	V
GND	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	-	VCC + 0.3	V
V _{IL}	Input Low Voltage	-0.3	-	+0.6	V
C _L	Output Load	-	-	30	pF
TTL	Output Load	-	-	1	-

Absolute Maximum Ratings*

VCC to GND-0.5V to +4.0V
 IN, IN/OUT Volt to GND -0.5V to VCC + 0.5V
 Operating Temperature, T_{opr}-25°C to +85°C
 Storage Temperature, T_{stg}.....-55°C to +125°C
 Power Dissipation, P_r.....0.7W

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = -25°C to + 85°C, VCC = 2.7V to 3.6V, GND = 0V)

Symbol	Parameter	LP62S16256F-55LLT / 70LLT			Unit	Conditions
		Min.	Typ.	Max.		
I _{LI}	Input Leakage Current	-	-	1	μA	V _{IN} = GND to VCC
I _{LO}	Output Leakage Current	-	-	1	μA	$\overline{CE} = V_{IH}$ $\overline{HB} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IH}$ V _{I/O} = GND to VCC
I _{CC}	Active Power Supply Current	-	-	5	mA	$\overline{CE} = V_{IL}$, I _{I/O} = 0mA
I _{CC1}	Dynamic Operating Current	-	25	40	mA	Min. Cycle, Duty = 100% $\overline{CE} = V_I$, I _{I/O} = 0mA
I _{CC2}		-	5	8	mA	$\overline{CE} = V_{IL}$, V _{IH} = VCC, V _{IL} = 0V, f = 1MHz, I _{I/O} = 0 mA
I _{SB}	Standby Current	-	-	1	mA	VCC ≤ 3.3V $\overline{CE} = V_{IH}$
I _{SB1}		-	0.3	10	μA	VCC ≤ 3.3V $\overline{CE} \geq VCC - 0.2V$, V _{IN} ≥ 0V
V _{OL}	Output Low Voltage	-	-	0.4	V	I _{OL} = 2.1 mA
V _{OH}	Output High Voltage	2.2	-	-	V	I _{OH} = -1.0 mA

Truth Table

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{LB}}$	$\overline{\text{HB}}$	I/O ₁ to I/O ₈ Mode	I/O ₉ to I/O ₁₆ Mode	VCC Current
H	X	X	X	X	Not selected	Not selected	I _{SB1} , I _{SB}
X	X	X	H	H	High - Z	High - Z	I _{SB1} , I _{SB}
L	L	H	L	L	Read	Read	I _{CC1} , I _{CC2} , I _{CC}
			L	H	Read	High - Z	I _{CC1} , I _{CC2} , I _{CC}
			H	L	High - Z	Read	I _{CC1} , I _{CC2} , I _{CC}
L	X	L	L	L	Write	Write	I _{CC1} , I _{CC2} , I _{CC}
			L	H	Write	High - Z	I _{CC1} , I _{CC2} , I _{CC}
			H	L	High - Z	Write	I _{CC1} , I _{CC2} , I _{CC}
L	H	H	L	X	High - Z	High - Z	I _{CC1} , I _{CC2} , I _{CC}
L	H	H	X	L	High - Z	High - Z	I _{CC1} , I _{CC2} , I _{CC}

Note: X = H or L

Capacitance (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C _{IN} *	Input Capacitance		6	pF	V _{IN} = 0V
C _{I/O} *	Input/Output Capacitance		8	pF	V _{I/O} = 0V

* These parameters are sampled and not 100% tested.

AC Characteristics ($T_A = -25^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7\text{V}$ to 3.6V)

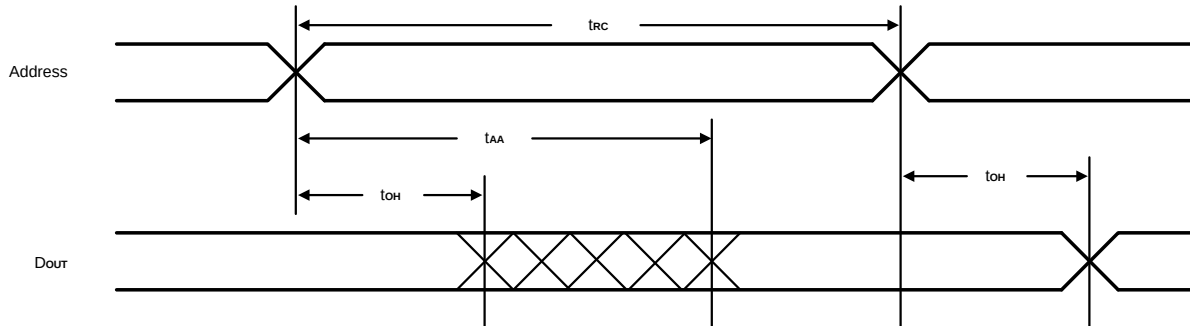
Symbol	Parameter	LP62S16256F-55LLT		LP62S16256F-70LLT		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
trc	Read Cycle Time	55	-	70	-	ns
tAA	Address Access Time	-	55	-	70	ns
tACE	Chip Enable Access Time	-	55	-	70	ns
tBE	Byte Enable Access Time	-	55	-	70	ns
toE	Output Enable to Output Valid	-	30	-	35	ns
tCLZ	Chip Enable to Output in Low Z	10	-	10	-	ns
tBLZ	Byte Enable to Output in Low Z	10	-	10	-	ns
toLZ	Output Enable to Output in Low Z	5	-	5	-	ns
tCHZ	Chip Disable to Output in High Z	-	20	-	25	ns
tBHZ	Byte Disable to Output in High Z	-	20	-	25	ns
toHZ	Output Disable to Output in High Z	-	20	-	25	ns
toH	Output Hold from Address Change	5	-	5	-	ns
Write Cycle						
twc	Write Cycle Time	55	-	70	-	ns
tcw	Chip Enable to End of Write	50	-	60	-	ns
tbw	Byte Enable to End of Write	50	-	60	-	ns
tAS	Address Setup Time	0	-	0	-	ns
tAW	Address Valid to End of Write	50	-	60	-	ns
tWP	Write Pulse Width	40	-	50	-	ns
tWR	Write Recovery Time	0	-	0	-	ns
tWHZ	Write to Output in High Z	-	25	-	25	ns
tdw	Data to Write Time Overlap	25	-	30	-	ns
tdH	Data Hold from Write Time	0	-	0	-	ns
tow	Output Active from End of Write	5	-	5	-	ns

Note: t_{CHZ} , t_{BHZ} and t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

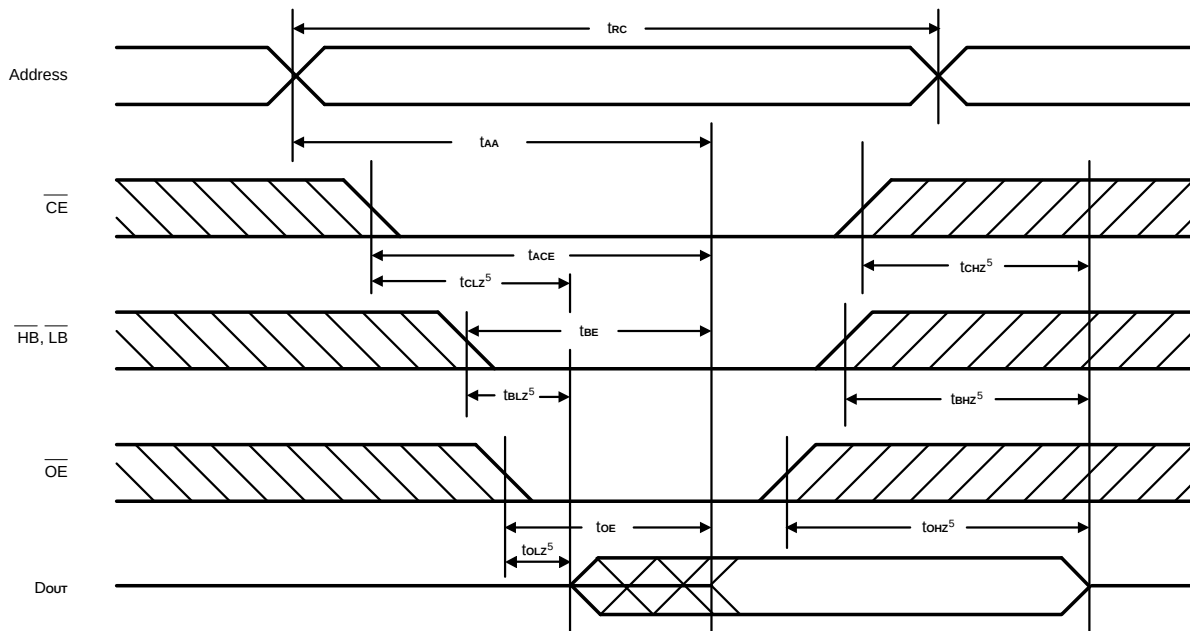


Timing Waveforms

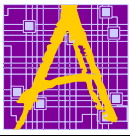
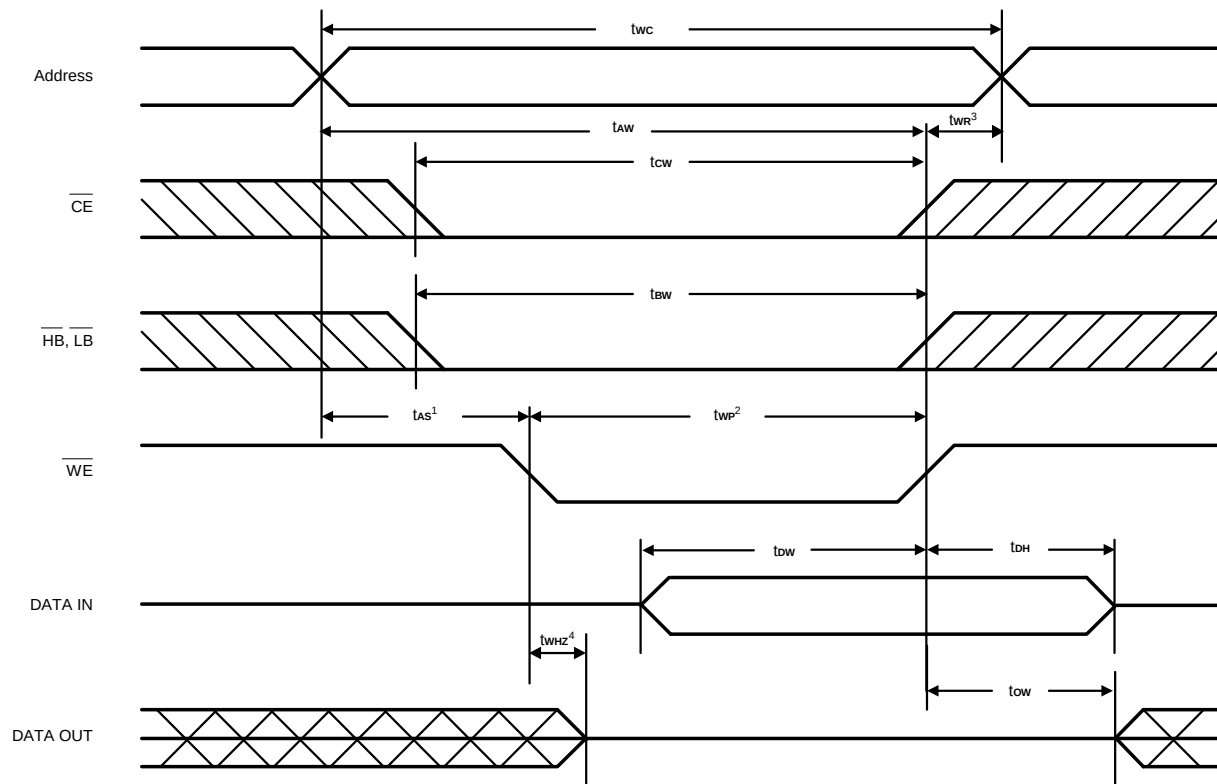
Read Cycle 1^(1, 2, 4)



Read Cycle 2^(1, 2, 3)



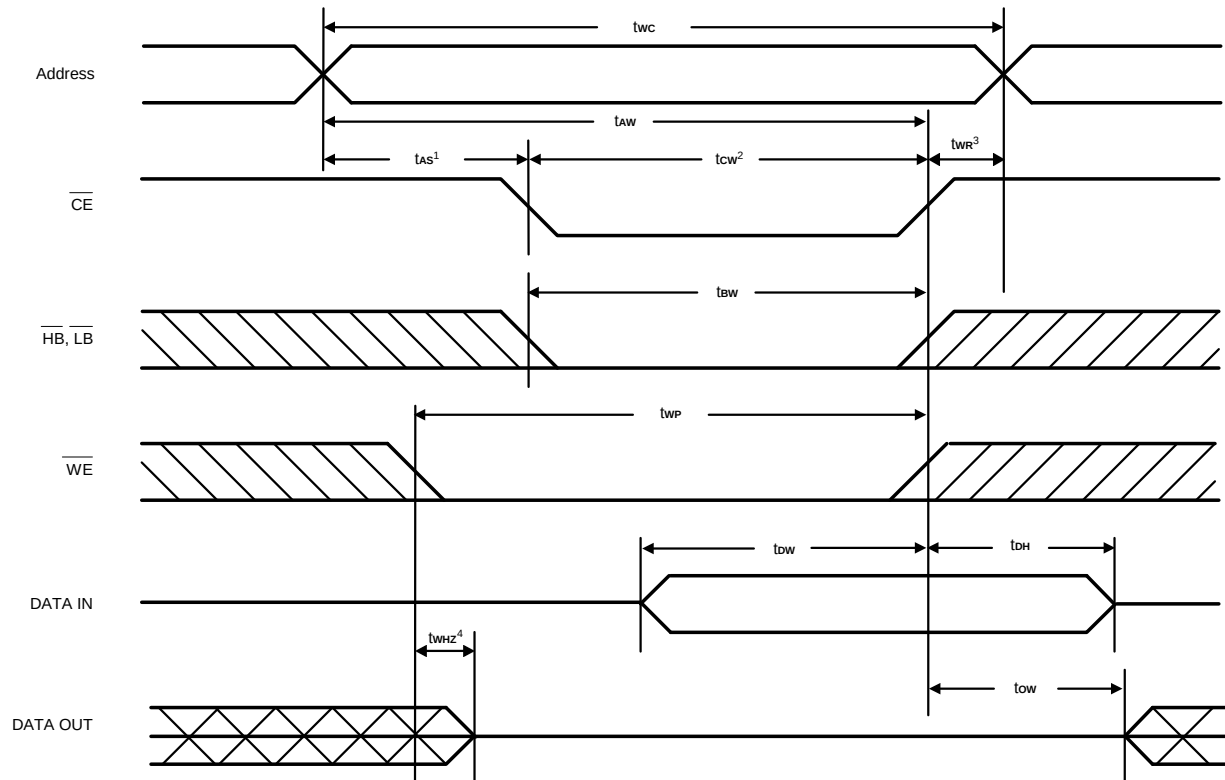
- Notes:
1. $\overline{WE}$ is high for Read Cycle.
 2. Device is continuously enabled $\overline{CE} = V_{IL}$, $\overline{HB} = V_{IL}$ and, or $\overline{LB} = V_{IL}$.
 3. Address valid prior to or coincident with $\overline{CE}$ and ($\overline{HB}$ and, or $\overline{LB}$) transition low.
 4. $\overline{OE} = V_{IL}$.
 5. Transition is measured $\pm 500\text{mV}$ from steady state. This parameter is sampled and not 100% tested.

**Timing Waveforms (continued)****Write Cycle 1
(Write Enable Controlled)**



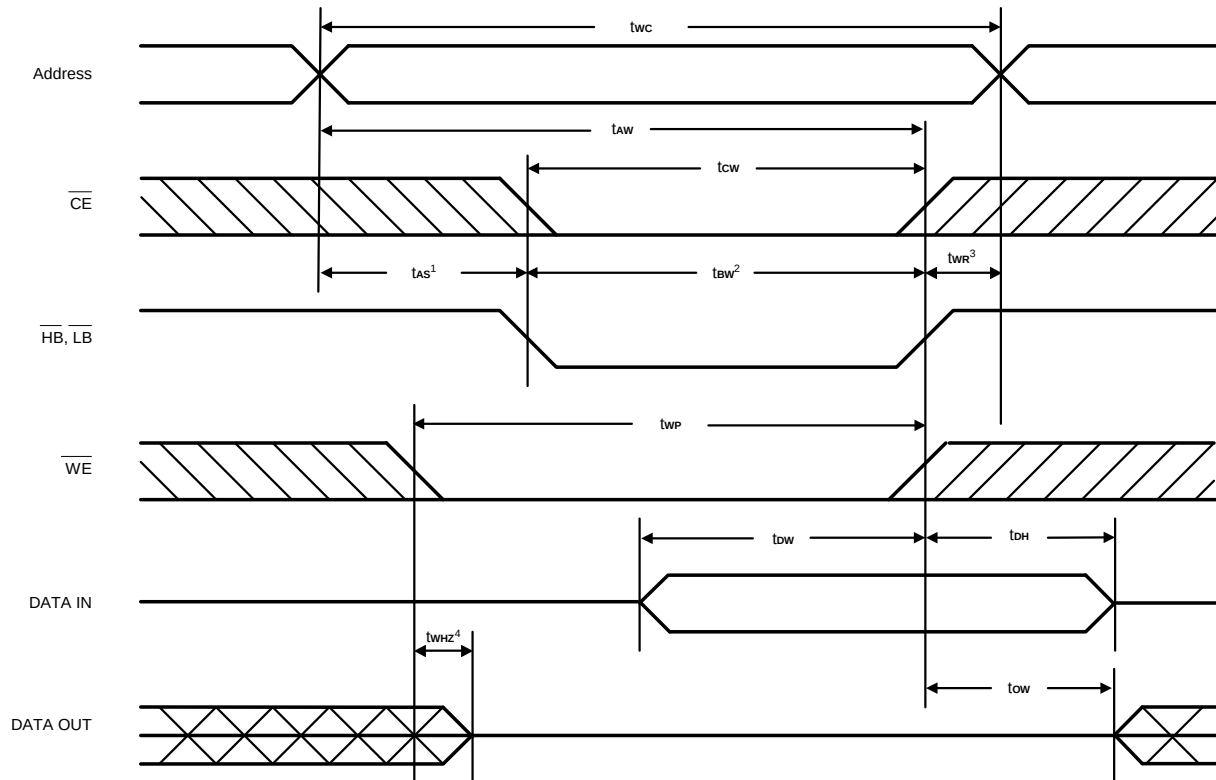
Timing Waveforms (continued)

Write Cycle 2 (Chip Enable Controlled)





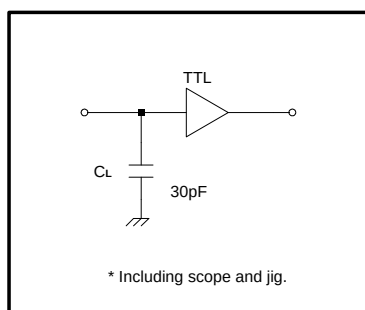
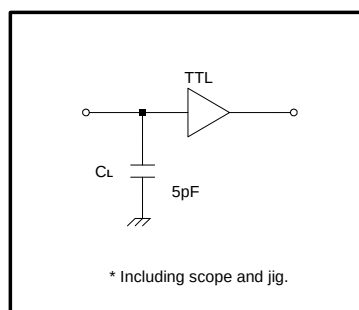
Timing Waveforms (continued)

Write Cycle 3
(Byte Enable Controlled)

- Notes:
1. t_{as} is measured from the address valid to the beginning of Write.
 2. A Write occurs during the overlap (t_{wp} , t_{bw}) of a low $\overline{CE}$, $\overline{WE}$ and ($\overline{HB}$ and , or $\overline{LB}$).
 3. t_{wr} is measured from the earliest of $\overline{CE}$ or $\overline{WE}$ or ($\overline{HB}$ and , or $\overline{LB}$) going high to the end of the Write cycle.
 4. $\overline{OE}$ level is high or low.
 5. Transition is measured $\pm 500\text{mV}$ from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

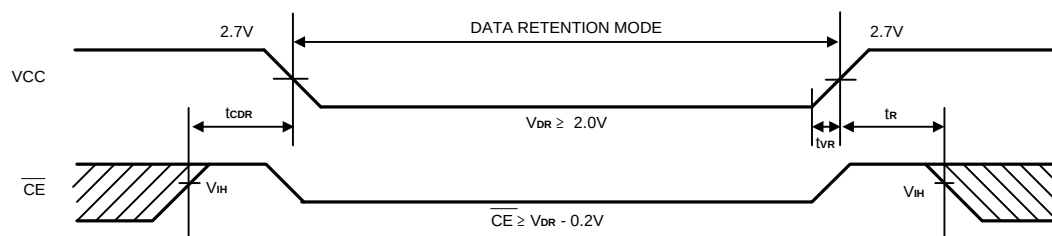
Input Pulse Levels	0.4V to 2.4V
Input Rise And Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 1 and 2


Figure 1. Output Load

Figure 2. Output Load for t_{CLZ} , t_{OLZ} , t_{CHZ} , t_{OHZ} , t_{WHZ} , and t_{OW}
Data Retention Characteristics ($T_A = -25^{\circ}\text{C}$ to 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DR}	VCC for Data Retention	2.0	-	3.6	V	$\overline{CE} \geq V_{CC} - 0.2V$
I_{CCDR}	Data Retention Current	-	0.08	3*	μA	$V_{CC} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq 0V$
t_{CDR}	Chip Disable to Data Retention Time	0	-	-	ns	See Retention Waveform
t_R	Operation Recovery Time	t_{RC}	-	-	ns	
t_{VR}	VCC Rising Time from Data Retention Voltage to Operating Voltage	5	-	-	ms	

* LP62S16256F-55LLT / 70LLT

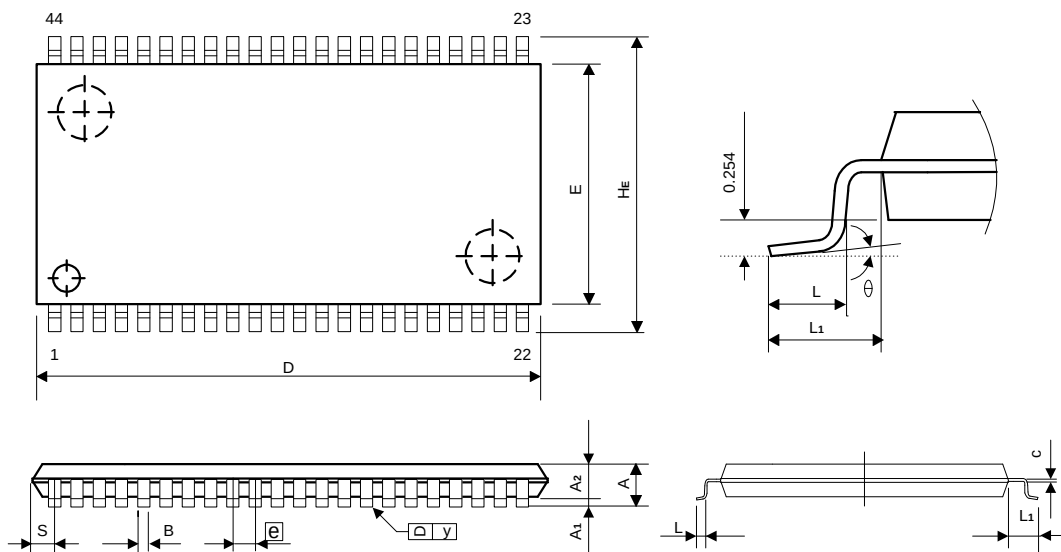
I_{CCDR} : max. $1\mu A$ at $T_A = 0^{\circ}\text{C}$ to $+40^{\circ}\text{C}$

Low VCC Data Retention Waveform

Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package
LP62S16256FV-55LLT	55	40	10	44L TSOP
LP62S16256FU-55LLT		40	10	48L CSP
LP62S16256FV-70LLT	70	40	10	44L TSOP
LP62S16256FU-70LLT		40	10	48L CSP

Package Information
TSOP 44L TYPE II Outline Dimensions

unit: inches/mm



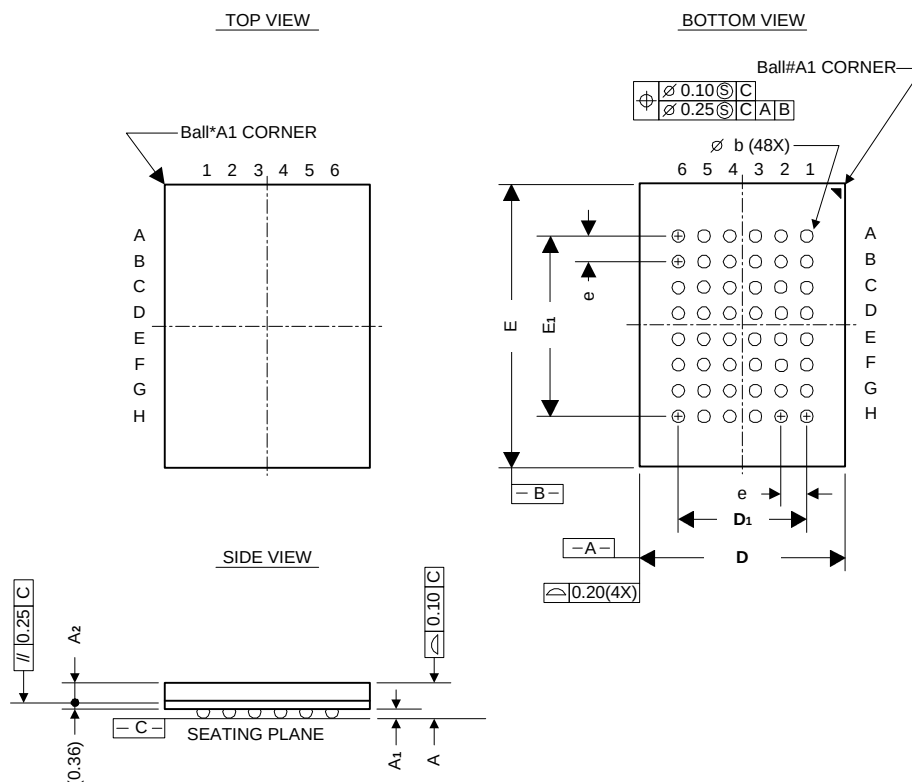
Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.047	-	-	1.20
A1	0.002	-	-	0.05	-	-
A2	0.037	0.039	0.041	0.95	1.00	1.05
B	0.010	0.014	0.018	0.25	0.35	0.45
c	-	0.006	-	-	0.15	-
D	0.721	0.725	0.729	18.31	18.41	18.51
E	0.396	0.400	0.404	10.06	10.16	10.26
[e]	-	0.031	-	-	0.80	-
HE	0.455	0.463	0.471	11.56	11.76	11.96
L	0.016	0.020	0.024	0.40	0.50	0.60
L1	-	0.031	-	-	0.80	-
S	-	-	0.036	-	-	0.93
y	-	-	0.004	-	-	0.10
θ	0°	-	5°	0°	-	5°

Notes:

1. Dimension D&E do not include interlead flash.
2. Dimension B does not include dambar protrusion/intrusion.
3. Dimension S includes end flash.

Package Information
**48LD CSP (6 x 8 mm) Outline Dimensions
(48TFBGA)**

unit: mm


Note:

1. THE BALL DIAMETER, BALL PITCH, STAND-OFF & PACKAGE THICKNESS ARE DIFFERENT FROM JEDEC SPEC MO192 (LOW PROFILE BGA FAMILY).
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM.
THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
4. BALL PAD OPENING OF SUBSTRATE IS Φ 0.3mm (SMD)
SUGGEST TO DESIGN THE PCB LAND SIZE AS Φ 0.3mm (NSMD)