

PWRLITE LS1106S

High Performance N-Channel JFET Transistor with Schottky Diode

Features

- ❖ Trench Power JFET with low threshold voltage V_{th} .
- ❖ Device fully "ON" with $V_{gs} = 0.7V$
- ❖ Optimum for "Low Side" Buck Converters
- ❖ Optimized for Secondary Rectification in isolated DC-DC
- ❖ Low R_g and low C_{ds} for high speed switching
- ❖ No "Body Diode"; extremely low C_{ds}
- ❖ Added Fast Recovery Schottky Diode in same package

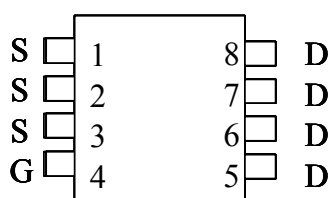
Applications

- ❖ DC-DC Converters for DDR and Graphic designs
- ❖ Synchronous Rectifiers
- ❖ PC Motherboard Converters
- ❖ Step-down power supplies
- ❖ Brick Modules
- ❖ VRM Modules

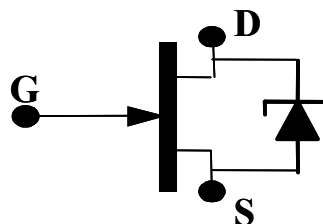
Description

The Power JFET transistor from Lovoltech is a device that presents a Low $R_{ds(on)}$ allowing for improved efficiencies in DC-DC switching applications. The device is designed with a low threshold such that drivers can operate at 5V, which reduces the driver power dissipation and increases the overall efficiency. Lower threshold produces faster turn-on/turn-off, which minimizes the required dead time. The transistor "No Body Diode" provides a very low associated parasitic capacitance C_{ds} . A Schottky Diode is added for applications where a freewheeling diode is required. Ringing is also reduced so that a lower voltage device may be a better solution.

DPAK Pin Assignments



Top View



N- Channel Power JFET

Pin Definitions

Pin Number	Pin Name	Pin Function Description	Product Summary		
4	Gate	Gate. Transistor Gate	V_{DS} (V)	$R_{ds(on)}$ (Ω)	I_D (A)
1, 2, 3	Source	Source. Transistor Source	15V	0.009	30
5, 6, 7, 8	Drain	Drain. Transistor Drain			

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Units
Drain-Source Voltage	V_{DS}	15	V
Gate-Source Voltage	V_{GS}	-10	V
Gate-Drain Voltage	V_{GD}	-18	V
Continuous Drain Current	I_D	30	A
Pulsed Drain Current	I_D	60	A
Single Pulse Drain-to-Source Avalanche Energy at 25°C ($V_{DD} = 5V_{DC}$, $I_L = 30A_{PK}$, $L = 0.3mH$, $R_G = 100\Omega$)	E_{AS}	120	mJ
Junction Temperature	T_J	-55 to 150°C	°C
Storage Temperature	T_{STG}	-65 to 150°C	°C
Lead Soldering Temperature, 10 seconds	T	260°C	°C
Power Dissipation (Derated at 25°C on large heat sink)	P_D	60	W



Thermal Resistance

Symbol	Parameter		DPAK Ratings		Units
$R_{\theta JA}$	Thermal Resistance Junction-to-Ambient		85		°C/W
$R_{\theta JC}$	Thermal Resistance Junction-to-Case		2.0		°C/W

Electrical Specifications

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

The ϕ denotes a specification which apply over the full operating temperature range.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
	Static						
BV _{DSX}	Breakdown Voltage Drain to Source	I _D = 0.5 mA V _{GS} = -4 V	ϕ	15			V
BV _{GDO}	Breakdown Voltage Gate to Drain	I _G = -50μA	ϕ			-18	V
BV _{GSO}	Breakdown Voltage Gate to Source	I _G = -1 mA	ϕ		-12	-10	V
R _{DS(ON)}	Static Drain to Source ¹ On Resistance (Current flows drain-to-source) See Fig. 1	I _G = 40 mA, I _D =10A I _G = 10 mA, I _D =10A I _G = 5 mA, I _D =10A			5.5 6 7	8 9	mΩ mΩ
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =0.1 V, I _D =250μA		-1200	-800	-500	mV
	Dynamic						
Q _G	Total Gate Charge	ΔV _{Drive} =5V, I _D =10A, V _{DS} =15V			11		nC
Q _{GD}	Gate to Drain Charge				6.5		nC
Q _{GS}	Gate to Source Charge				1.0		nC
Q _{SW}	Switching Charge				7.5		nC
R _G	Gate Resistance				1		Ω
T _{D(ON)}	Turn-on Delay Time	V _{DD} =12V, I _D =10A V _{Drive} = 5 V Clamped Inductive Load	ϕ		5		ns
T _R	Rise Time		ϕ		10		
T _{D(OFF)}	Turn-off Delay				2		
T _F	Fall Time				8		
C _{ISS}	Input Capacitance	V _{DS} =10V, V _{GS} = -5 V, 1MHz.			1600		pF
C _{OSS}	Output Capacitance				450		
C _{GS}	Gate-Source Capacitance				1100		
C _{GD}	Gate-Drain Capacitance				400		
C _{DS}	Drain-Source Capacitance				110		
	Diode						
I _R	Reverse Leakage	V _R =15V			0.25	0.5	mA
V _F	Forward Voltage	I _F = 1 A				400	mV
V _F	Forward Voltage	I _F = 10 A			750	900	mV
V _F	Forward Voltage	I _F = 20 A			1100		mV
Q _{rr}	Reverse Recovery Charge	I _s = 20 A di/dt = 200A/us,			8		nC

Notes:

1. Pulse width $\leq 500\mu\text{s}$, duty cycle $\leq 2\%$

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

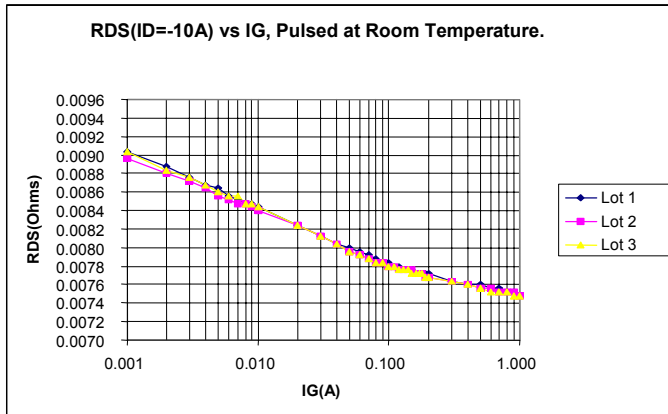


Figure 1 – $R_{DS(on)}$ vs Gate Current at $I_D = 10\text{A}$

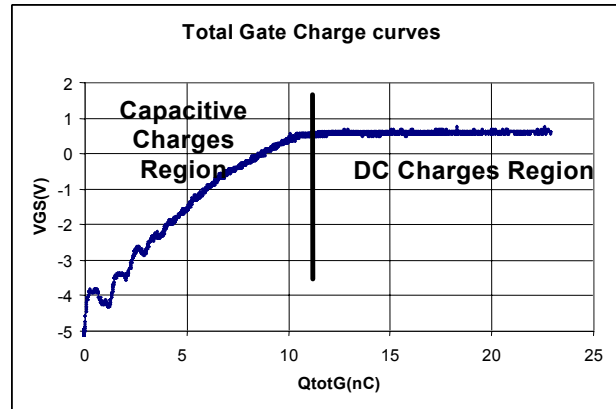


Figure 2 – Total Gate Charge

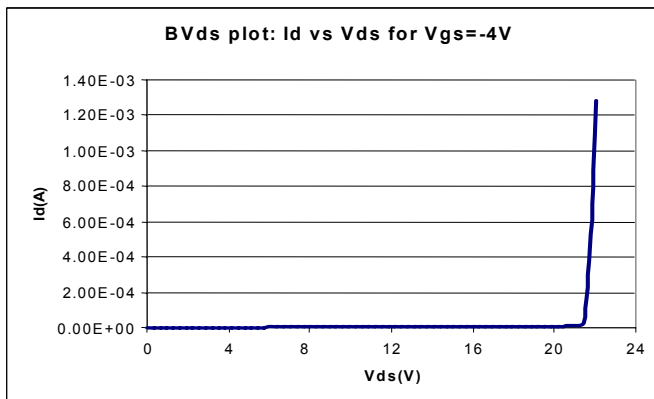


Figure 3 – Breakdown Voltage V_{ds} vs I_d

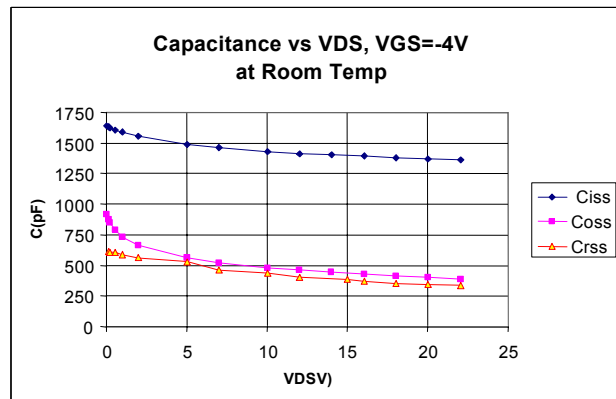


Figure 4 – Capacitance vs Drain Voltage V_{ds}

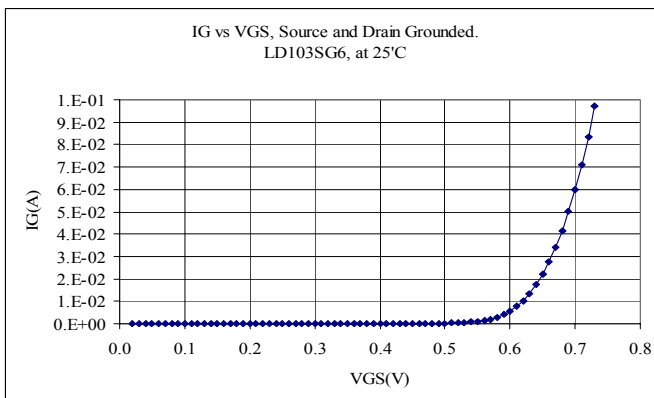


Figure 5 – I_G vs Gate Voltage V_{GS}

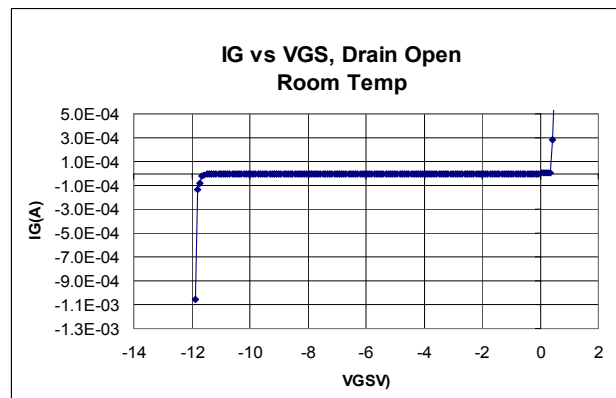


Figure 6 – Typical Gate Voltage Characteristic

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

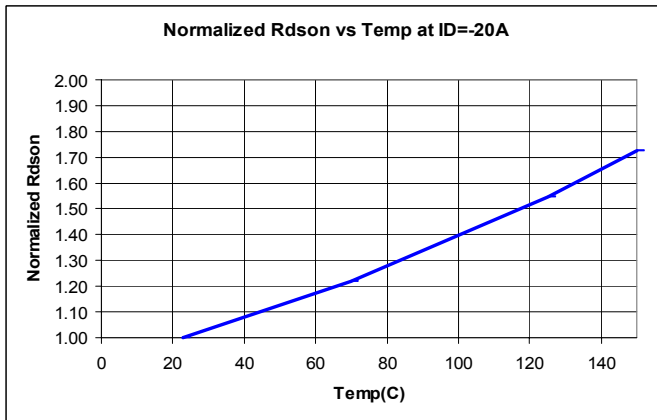


Figure 7 – $R_{DS(on)}$ Temperature Coefficient

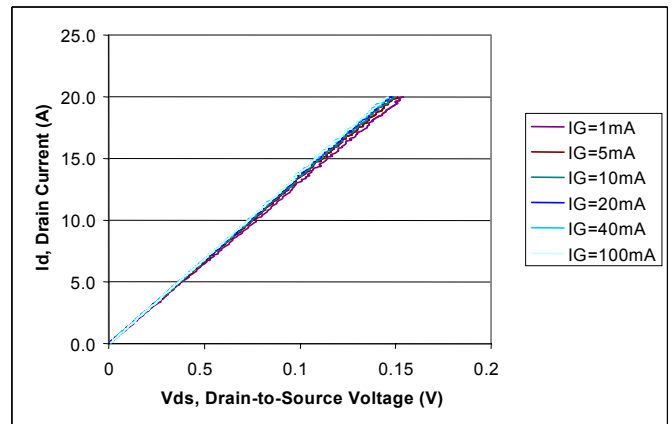


Figure 8 – On-Region Characteristics

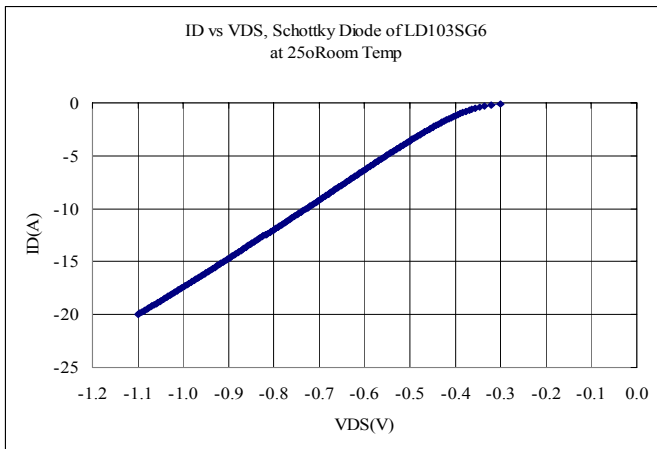


Figure 9 – Diode Voltage vs Current

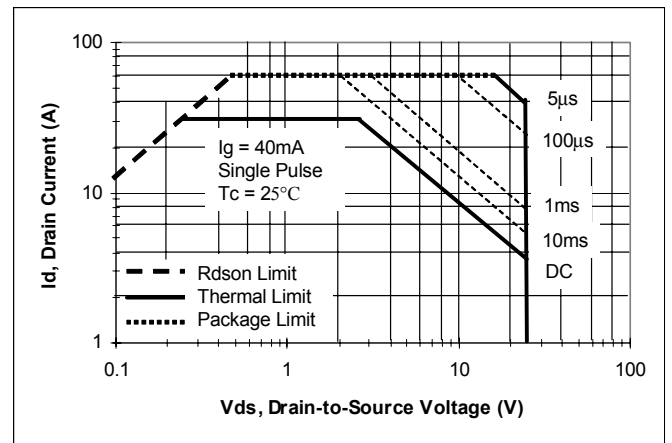


Figure 10 – Safe Operating Area

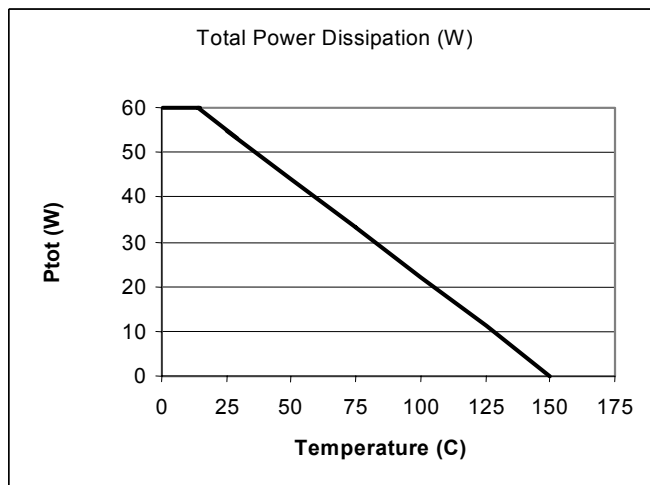


Figure 11 – Total Power Dissipation

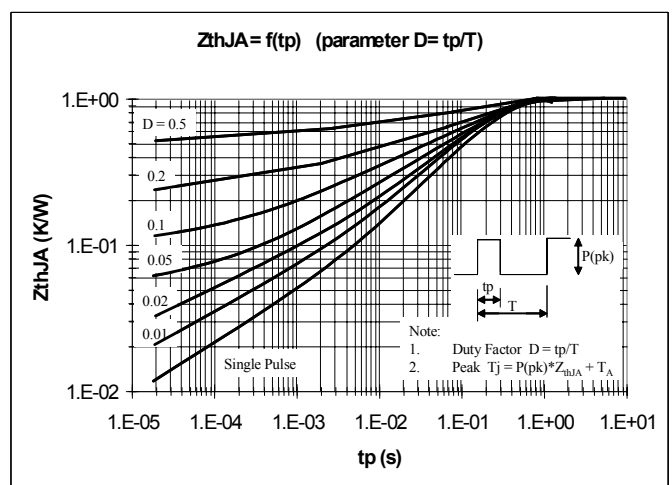


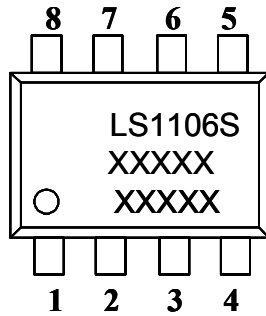
Figure 12 – Normalized Thermal Response



Ordering Information

Product Number	PN Marking	Package
LS1106S	LS1106S	TO252 (DPAK)

Package and Marking Information



Life Support Policy

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- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Datasheet Identification	Product Status	Definition
Advance Information	In definition or in Design	This datasheet contains the design specifications for product development. Specifications may change without notice.
Preliminary	Initial Production	This datasheet contains preliminary data; additional and application data will be published at a later date. Lovoltech, Inc. reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	In Production	This datasheet contains final specifications. Lovoltech reserves the right to make changes at any time without notice in order to improve the design.