



PWRLITE-LS1105S

Enhanced N-Channel Power JFET Transistor, Trench Technology

Features

- ❖ Trench Power JFET with low threshold voltage
- ❖ Device fully “ON” with $V_{GS} = 0.7V$
- ❖ Optimum for “Low Side” Buck and DC-DC Converters
- ❖ Low R_g and low C_{ds} for high speed switching
- ❖ No “Body Diode”; extremely low C_{ds}

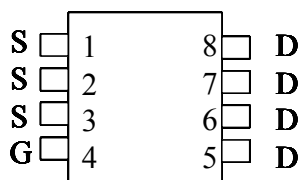
Applications

- ❖ VGA and Graphic Cards for stand-by operation
- ❖ DDR, SDRAM for stand-by operation Power Supply
- ❖ DC-DC Converters
- ❖ Synchronous Rectifiers
- ❖ PC Motherboard Converters
- ❖ Step-down power supplies
- ❖ Brick Modules
- ❖ VRM Modules

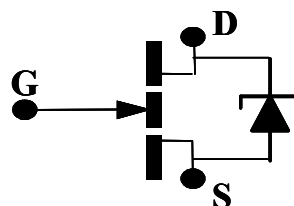
Description

The Power JFET transistor from Lovoltech is a device that presents a Low $R_{ds(on)}$ allowing for improved efficiencies in DC-DC switching applications. The device is designed with a low threshold such that drivers can operate at 5V, which reduces the driver power dissipation and increases the overall efficiency. Lower threshold produces faster turn-on/turn-off, which minimizes the required dead time. The transistor “No Body Diode” provides a very low associated parasitic capacitance C_{ds} .

SO8 Pin Assignments



Top View



N – Channel Power JFET

Pin Definitions

Pin Number	Pin Name	Pin Function Description	Product Summary		
4	Gate	Gate. Transistor Gate	V_{DS} (V)	$R_{ds(on)}$ (Ω)	I_D (A)
1, 2, 3	Source	Source. Transistor Source	20V	0.011	30
5, 6, 7, 8	Drain	Drain. Transistor Drain			

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Units
Drain-Source Voltage	V_{DS}	25	V
Gate-Source Voltage	V_{GS}	-10	V
Gate-Drain Voltage	V_{GD}	-25	V
Continuous Drain Current	I_D	30	A
Pulsed Drain Current	I_D		A
Junction Temperature	T_J	-55 to 150°C	°C
Storage Temperature		-65 to 150°C	-65 to 150°C
Lead Soldering Temperature, 10 seconds	300°C	300°C	300°C
Power Dissipation	P_D	3	W

Thermal Resistance

Symbol	Parameter		SO8 Ratings		Units
$R\Theta_{JA}$	Thermal Resistance Junction-to-Ambient		65		°C/W
$R\Theta_{JC}$	Thermal Resistance Junction-to-Case		20		°C/W

Electrical Specifications

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

The ϕ denotes specifications which apply over the full operating temperature range.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
	Static						
BV _{DSX}	Breakdown Voltage Drain to Source	I _D = 1 mA	ϕ	20	25		V
BV _{GDO}	Breakdown Voltage Gate to Drain	I _G = -50μA	ϕ		-25	-20	V
BV _{GSO}	Breakdown Voltage Gate to Source	I _G = -1 mA	ϕ		-12	-10	V
R _{DS(ON)}	Static Drain to Source ¹ On Resistance (Current flows drain-to-source)	I _G = 100 mA, I _D =10A I _G = 40 mA, I _D =10A			10 12	11 16	mΩ mΩ
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =1 V, I _D =250μA	ϕ	150	250		mV
	Dynamic						
Q _G	Total Gate Charge	ΔV _{Drive} =5V, I _D =10A, V _{DS} =15V			10		nC
Q _{GD}	Gate to Drain Charge				6		nC
Q _{GS}	Gate to Source Charge				0.7		nC
Q _{SW}	Gate to Source Charge				6.7		nC
R _G	Gate Resistance				0.8		Ω
T _{D(ON)}	Turn-on Delay Time	V _{DS} =15V, I _D =10A V _{Drive} = 5 V Clamped Inductive Load	ϕ		4		ns
T _R	Rise Time		ϕ		8		
T _{D(OFF)}	Turn-off Delay				2		
T _F	Fall Time				8		
C _{ISS}	Input Capacitance (C _{gs} +C _{gd})	V _{DS} =10V, V _{GS} = -5 V, 1MHz.			1250		pF
C _{OSS}	Output Capacitance (C _{ds} +C _{gd})				500		
C _{GS}	Gate-Source Capacitance				900		
C _{GD}	Gate-Drain Capacitance (Crss)				350		
C _{DS}	Drain-Source Capacitance				150		
	Schottky Diode						
B _V	Reverse Breakdown Voltage	I _R = 0.1 mA		25	30		V
I _R	Reverse Leakage	V _R =25V			0.25	0.3	mA
V _F	Forward Voltage	I _F = 1 A				500	mV
V _F	Forward Voltage	I _F = 3 A				550	mV
V _F	Forward Voltage	I _F = 15 A			800		mV
Q _{rr}	Reverse Recovery Charge	I _s = 25 A di/dt = 700A/us, V _{ds} =16V, V _{gs} = 0V					nC

Notes:

1. Pulse width $\leq 500\mu\text{s}$, duty cycle $\leq 2\%$

Typical Application

Because of the absence of a body diode, the LVTS101N is suitable to power VGA, Graphic, DDR and SDRAM memory modules that are used in normal operation mode or can be switch in stand-by mode to save energy when memory access is not required. The typical JFET application is compared to a MOSFET design. One can identify the reduction in component count by taking advantage of the trench JFET technology (figures 5 and 6):

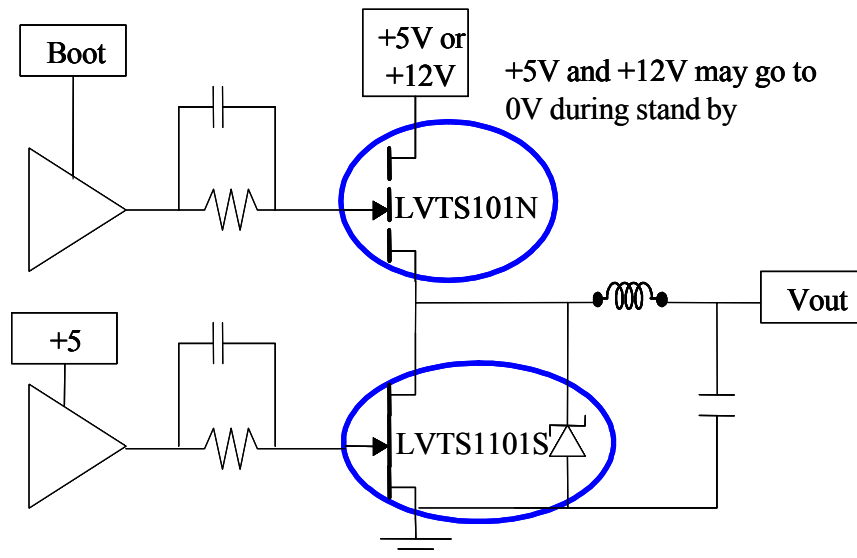
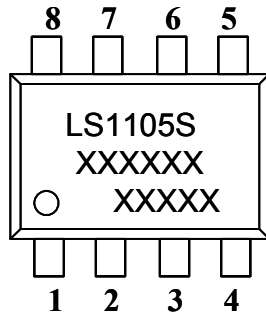


Figure 5 – Typical JFET Buck Converter best suitable for VGA and DDR designs

Ordering Information

Product Number	PN Marking	Package
LS1105S	LS1105S	8 pin SOIC

Package and Marking Information



Life Support Policy

LOVOLTECH's PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF LOVOLTECH, Inc. As used herein:

1. Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Datasheet Identification	Product Status	Definition
Advance Information	In definition or in Design	This datasheet contains the design specifications for product development. Specifications may change without notice.
Preliminary	Initial Production	This datasheet contains preliminary data; additional and application data will be published at a later date. Lovoltech, Inc. reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	In Production	This datasheet contains final specifications. Lovoltech reserves the right to make changes at any time without notice in order to improve the design.