PWRLITE-LS1101S

Enhanced N-Channel Power JFET Transistor, Trench Technology

Features

- Trench Power JFET with low threshold voltage
- Device fully "ON" with Vgs = 0.7V
- Optimum for "Low Side" Buck and DC-DC Converters
- Low Rg and low Cds for high speed switching
- No "Body Diode"; extremely low Cds

Applications

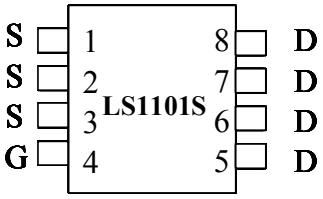
- VGA and Graphic Cards for stand-by operation
- DDR, SDRAM for stand-by operation Power Supply
- DC-DC Converters
- Synchronous Rectifiers
- PC Motherboard Converters
- Step-down power supplies
- Brick Modules
- VRM Modules

Description

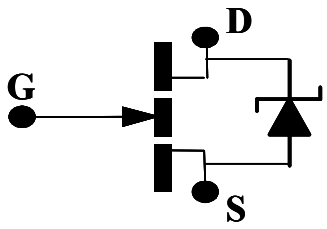
The Power JFET transistor from Lovoltech is a device that presents a Low Rdson allowing for improved efficiencies in DC-DC switching applications. The device is designed with a low threshold such that drivers can operate at 5V, which reduces the driver power dissipation and increases the overall efficiency. Lower threshold produces faster turn-on/turn-off, which minimizes the required dead time. The transistor "No Body Diode" provides a very low associated parasitic capacitance Cds.

Advanced Information

SO8 Pin Assignments



Top View



N – Channel Power JFET

Pin Definitions

Pin Number	Pin Name	Pin Function Description
4	Gate	**Gate.** Transistor Gate
1, 2, 3	Source	**Source.** Transistor Source
5, 6, 7, 8	Drain	**Drain.** Transistor Drain

Product Summary		
V_{DS} (V)	Rdson (Ω)	I_D (A)
20V	0.012	15

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Units
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	-10	V
Gate-Drain Voltage	V_{GD}	-20	V
Continuous Drain Current	I_D	15	A
Pulsed Drain Current	I_D		A
Junction Temperature	T_J	-55 to 150°C	°C
Storage Temperature	T_{STG}	-65 to 150°C	°C
Lead Soldering Temperature, 10 seconds	T	260°C	°C
Power Dissipation	P_D	80	W

Thermal Resistance

Symbol	Parameter		SO8 Ratings		Units
$R\Theta_{JA}$	Thermal Resistance Junction-to-Ambient		65		°C/W
$R\Theta_{JC}$	Thermal Resistance Junction-to-Case		20		°C/W

Electrical Specifications

(T_A = +25°C, unless otherwise noted.)

The ϕ denotes specifications which apply over the full operating temperature range.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
	Static						
BV_{DSX}	Breakdown Voltage Drain to Source	I_D = 1 mA	ϕ	20	25		V
BV_{GDO}	Breakdown Voltage Gate to Drain	I_G = -50µA	ϕ		-25	-20	V
BV_{GSO}	Breakdown Voltage Gate to Source	I_G = -1 mA	ϕ		-12	-10	V
$R_{DS(ON)}$	Static Drain to Source[1] On Resistance (Current flows drain-to-source)	I_G = 100 mA, I_D=10A I_G = 40 mA, I_D=10A			10 12	12 16	mΩ mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=1 V, I_D=250µA	ϕ	150	250		mV
	Dynamic						
Q_G	Total Gate Charge	ΔV_{Drive}=5V, I_D=10A,V_{DS}=15V			10		nC
Q_{GD}	Gate to Drain Charge				6		nC
Q_{GS}	Gate to Source Charge				0.7		nC
Q_{SW}	Gate to Source Charge				6.7		nC
R_G	Gate Resistance				0.8		Ω
$T_{D(ON)}$	Turn-on Delay Time	V_{DS}=15V, I_D=10A V_{Drive} = 5 V Clamped Inductive Load	ϕ		4		ns
T_R	Rise Time		ϕ		8		
$T_{D(OFF)}$	Turn-off Delay				2		
T_F	Fall Time				8		
C_{ISS}	Input Capacitance (Cgs+Cgd)	V_{DS}=10V, V_{GS}= -5 V, 1MHz.			1250		pF
C_{OSS}	Output Capacitance (Cds+Cgd)				500		
C_{GS}	Gate-Source Capacitance				900		
C_{GD}	Gate-Drain Capacitance (Crss)				350		
C_{DS}	Drain-Source Capacitance				150		
	Schottky Diode						
B_V	Reverse Breakdown Voltage	I_R = 0.1 mA		25	30		V
I_R	Reverse Leakage	V_R=25V			0.25	0.3	mA
V_F	Forward Voltage	I_F = 1 A				500	mV
V_F	Forward Voltage	I_F = 3 A				550	mV
V_F	Forward Voltage	I_F = 15 A			800		mV
Qrr	Reverse Recovery Charge	I_s = 25 A di/dt = 700A/us, Vds=16V, Vgs = 0V					nC

Notes:

1. Pulse width <= 500µs, duty cycle < = 2%

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Typical Application

Because of the absence of a body diode, the LVTS101N is suitable to power VGA, Graphic, DDR and SDRAM memory modules that are used in normal operation mode or can be switch in stand-by mode to save energy when memory access is not required. The typical JFET application is compared to a MOSFET design. One can identify the reduction in component count by taking advantage of the trench JFET technology (figures 5 and 6):

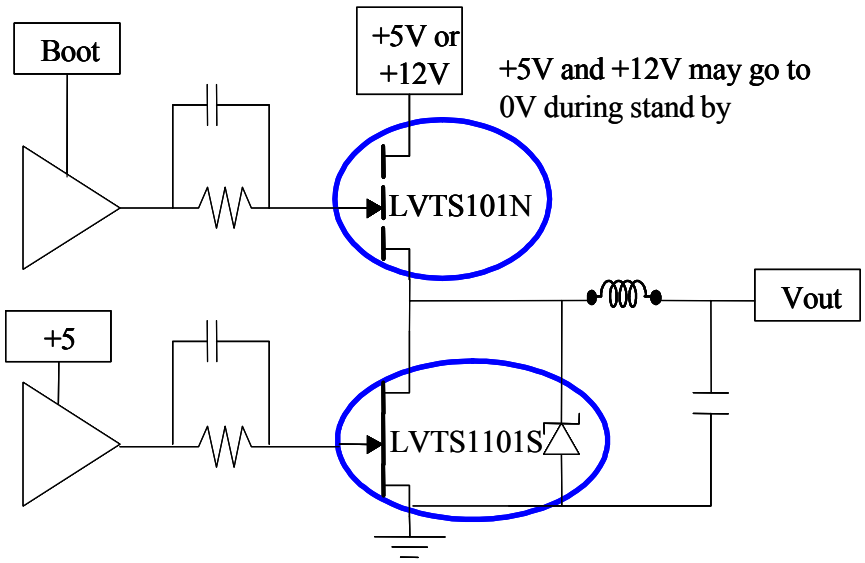
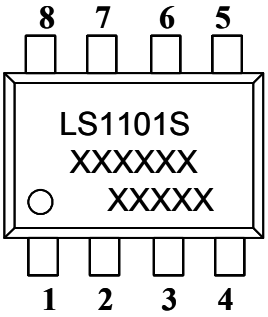


Figure 5 – Typical JFET Buck Converter best suitable for VGA and DDR designs

Ordering Information

Product Number	PN Marking	Package
LS1101S	LS1101S	8 pin SOIC

Package and Marking Information



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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Datasheet Identification	Product Status	Definition
Advance Information	In definition or in Design	This datasheet contains the design specifications for product development. Specifications may change without notice.
Preliminary	Initial Production	This datasheet contains preliminary data; additional and application data will be published at a later date. Lovoltech, Inc. reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	In Production	This datasheet contains final specifications. Lovoltech reserves the right to make changes at any time without notice in order to improve the design.

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