

PWRLITE LB1010SD

High Performance N-Ch JFET Transistor with Schottky and PN Diodes

Features

- ❖ Trench Power JFET with low threshold voltage V_{th} .
- ❖ Device fully "ON" with $V_{gs} = 0.7V$
- ❖ Optimum for "Low Side" Buck Converters
- ❖ Optimized for Secondary Rectification in isolated DC-DC
- ❖ Low R_g and low C_{ds} for high speed switching
- ❖ No "Body Diode"; extremely low C_{ds}
- ❖ Added Fast Recovery Schottky Diode in same package

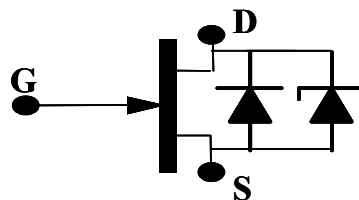
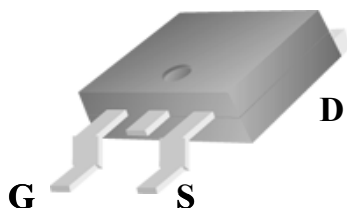
Applications

- ❖ DC-DC Converters
- ❖ Synchronous Rectifiers
- ❖ PC Motherboard Converters
- ❖ Step-down power supplies
- ❖ Brick Modules
- ❖ VRM Modules

Description

The Power JFET transistor from Lovoltech is a device that presents a Low $R_{ds(on)}$ allowing for improved efficiencies in DC-DC switching applications. The device is designed with a low threshold such that drivers can operate at 5V, which reduces the driver power dissipation and increases the overall efficiency. Lower threshold produces faster turn-on/turn-off, which minimizes the required dead time. The transistor "No Body Diode" provides a very low associated parasitic capacitance C_{ds} . A Schottky Diode is added for applications where a freewheeling diode is required. Ringing is also reduced so that a lower voltage device may be a better solution.

D2PAK Pin Assignments



**N – Channel Power JFET
PN & Schottky Diodes**

Pin Definitions

Pin Number	Pin Name	Pin Function Description	Product Summary		
1	Gate	Gate. Transistor Gate	V_{DS} (V)	$R_{ds(on)}$ (Ω)	I_D (A)
2	Drain	Drain. Transistor Drain	24V	0.00375	50
3	Source	Source. Transistor Source			

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Units
Drain-Source Voltage	V_{DS}	24	V
Gate-Source Voltage	V_{GS}	-10	V
Gate-Drain Voltage	V_{GD}	-28	V
Continuous Drain Current	I_D	50	A
Pulsed Drain Current	I_D	100	A
Single Pulse Drain-to-Source Avalanche Energy at 25°C ($V_{DD}=5V_{DC}$, $I_L=60A_{PK}$, $L=0.3mH$, $R_G=100\Omega$)	E_{AS}	220	mJ
Junction Temperature	T_J	-55 to 150°C	°C
Storage Temperature	T_{STG}	-65 to 150°C	°C
Lead Soldering Temperature, 10 seconds	T	260°C	°C
Power Dissipation (Derated at 25°C)	P_D	110	W



Thermal Resistance

Symbol	Parameter		D2PAK Ratings		Units
$R\Theta_{JA}$	Thermal Resistance Junction-to-Ambient		60		°C/W
$R\Theta_{JC}$	Thermal Resistance Junction-to-Case		1.2		°C/W

Electrical Specifications

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

The ϕ denotes a specification which apply over the full operating temperature range.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
	Static						
BV _{DSX}	Breakdown Voltage Drain to Source	I _D = 0.5 mA V _{GS} = -4 V		24			V
BV _{GDO}	Breakdown Voltage Gate to Drain	I _G = -50μA				-28	V
BV _{GSO}	Breakdown Voltage Gate to Source	I _G = -1 mA			-12	-10	V
R _{DS(ON)}	Static Drain to Source ¹ On Resistance (Current flows drain-to-source) See Fig. 1	I _G = 40 mA, I _D =10A I _G = 10 mA, I _D =10A I _G = 5 mA, I _D =10A			3.3 3.5 4.0	3.75 4.2	mΩ mΩ
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =0.1 V, I _D =250μA		-1200		-600	mV
	Dynamic						
Q _G	Total Gate Charge	ΔV _{Drive} =5V, I _D =10A, V _{DS} =15V			21		nC
Q _{GD}	Gate to Drain Charge				13		nC
Q _{GS}	Gate to Source Charge				1.5		nC
Q _{SW}	Switching Charge				14.5		nC
R _G	Gate Resistance				1		Ω
T _{D(ON)}	Turn-on Delay Time	V _{DD} =16V, I _D =15A V _{Drive} = 5 V Clamped Inductive Load			5		ns
T _R	Rise Time				12		
T _{D(OFF)}	Turn-off Delay				2		
T _F	Fall Time				10		
C _{ISS}	Input Capacitance	V _{DS} =10V, V _{GS} = -5 V, 1MHz.			3000		pF
C _{OSS}	Output Capacitance				900		
C _{GS}	Gate-Source Capacitance				2250		
C _{GD}	Gate-Drain Capacitance				750		
C _{DS}	Drain-Source Capacitance				200		
	Combo Schottky and PN-Diodes						
I _R	Reverse Leakage	V _R =24V			0.25	0.5	mA
V _F	Forward Voltage	I _F = 1 A				400	mV
V _F	Forward Voltage	I _F = 10 A			750	900	mV
V _F	Forward Voltage	I _F = 25 A			1100		mV
Q _{rr}	Reverse Recovery Charge	I _s = 25 A di/dt = 700A/us,			7		nC

Notes:

1. Pulse width $\leq 500\mu\text{s}$, duty cycle $\leq 2\%$

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

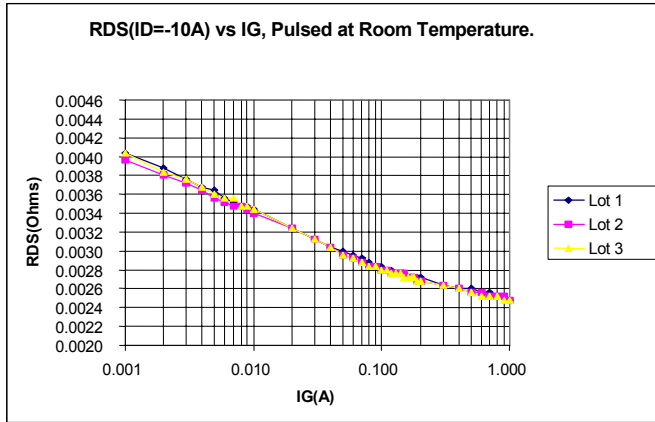


Figure 1 – $R_{DS(on)}$ vs Gate Current at $I_D = 10\text{A}$

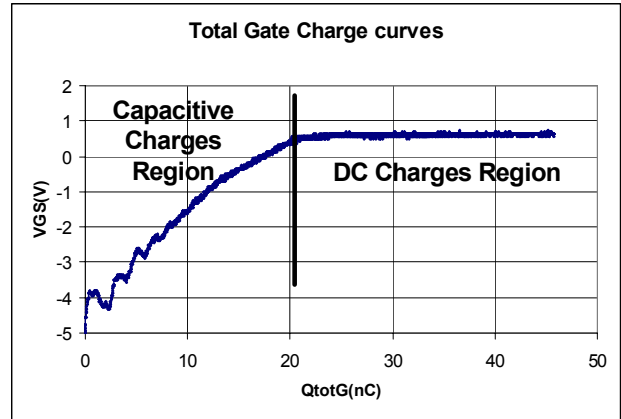


Figure 2 – Total Gate Charge

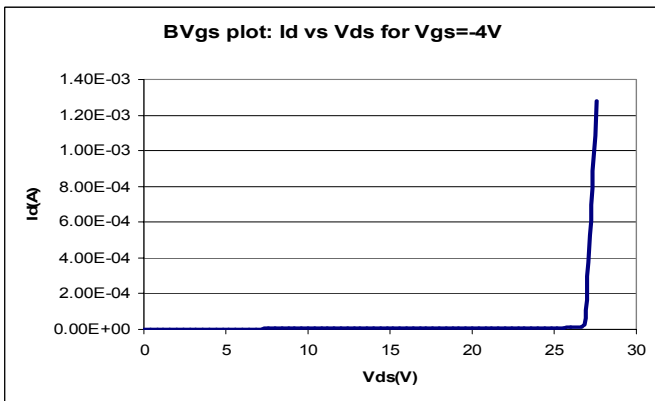


Figure 3 – Breakdown Voltage V_{ds} vs I_d

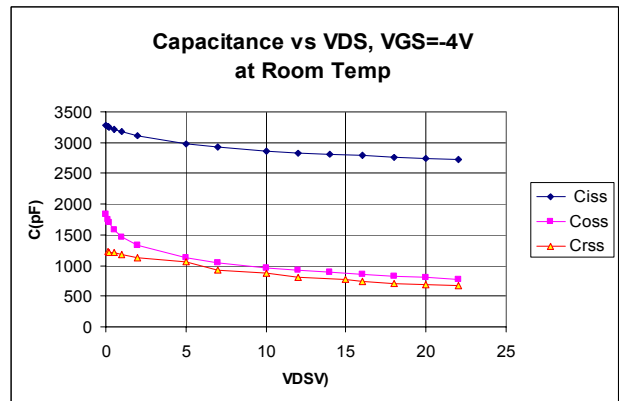


Figure 4 – Capacitance vs Drain Voltage V_{ds}

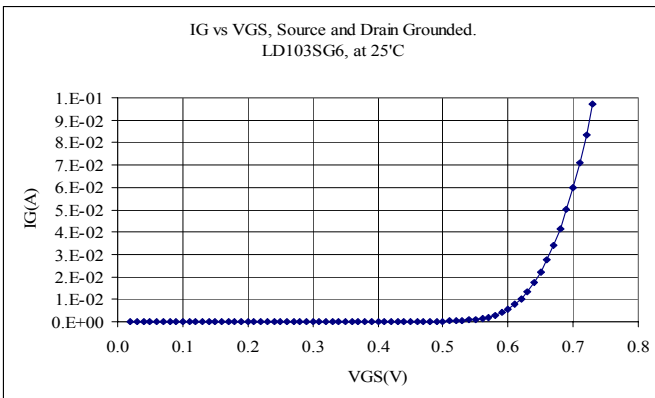


Figure 5 – I_G vs Gate Voltage V_{GS}

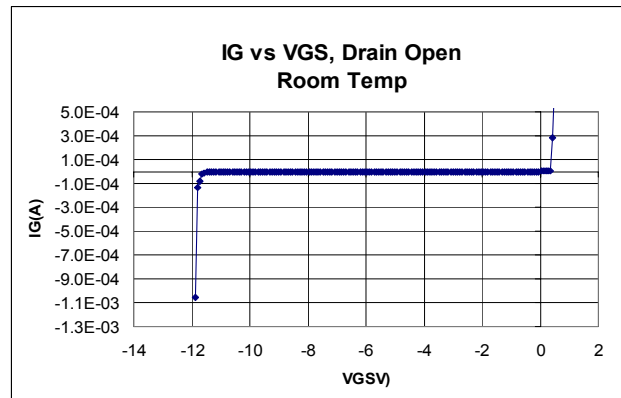


Figure 6 – Typical Gate Voltage Characteristic

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

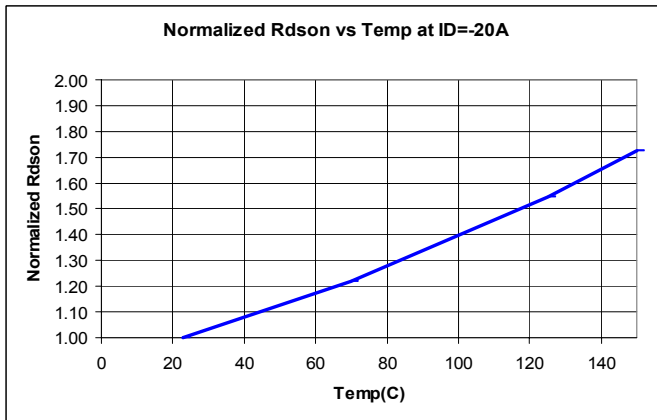


Figure 7 – $R_{DS(on)}$ Temperature Coefficient

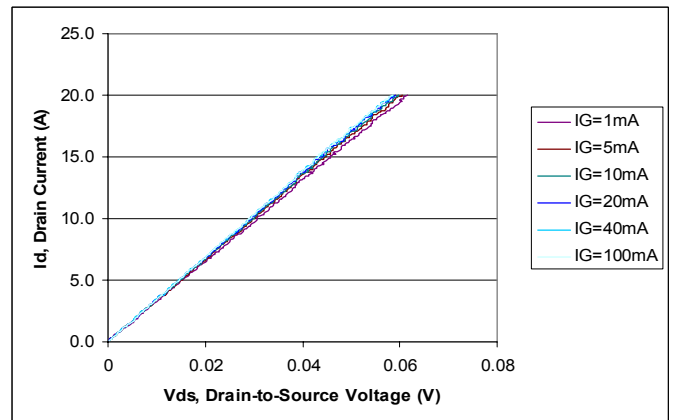


Figure 8 – On-Region Characteristics

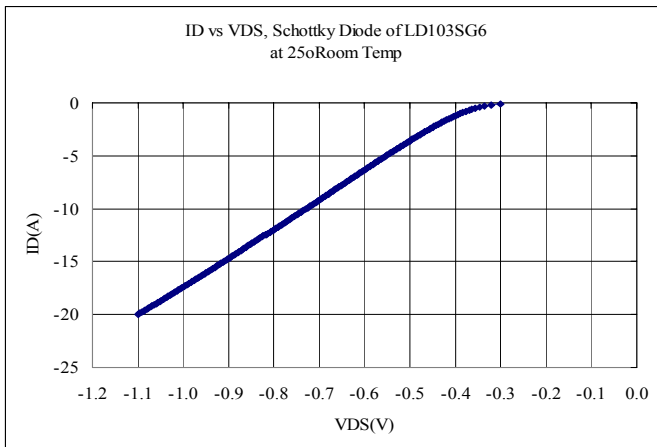


Figure 9 – Schottky Diode Voltage vs Current

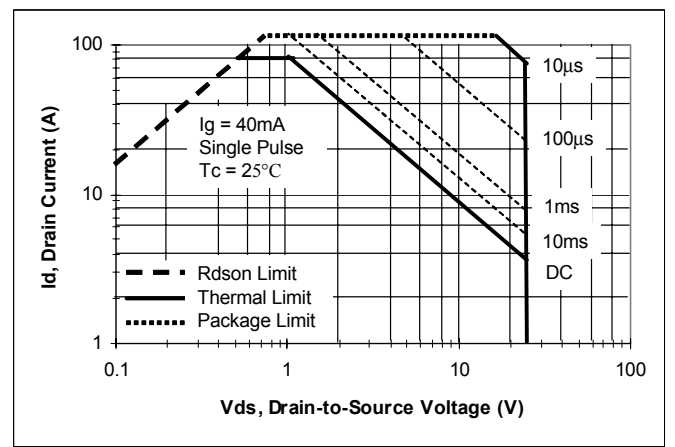


Figure 10 – Safe Operating Area

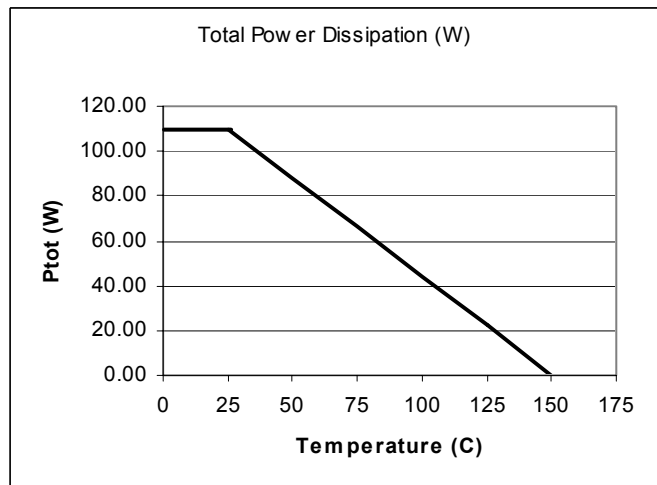


Figure 11 – Total Power Dissipation

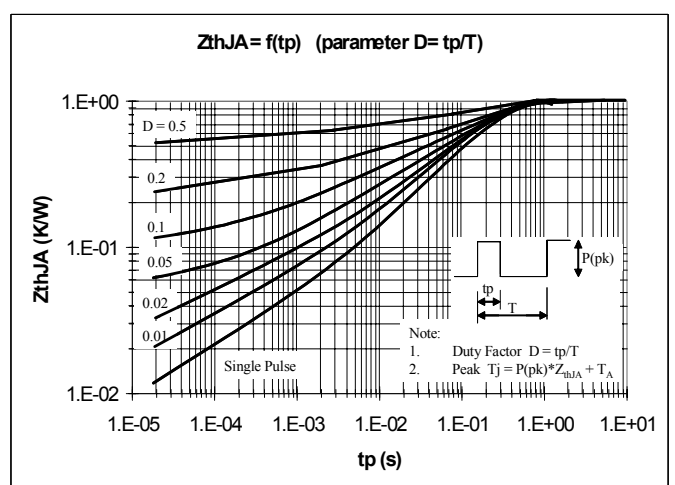


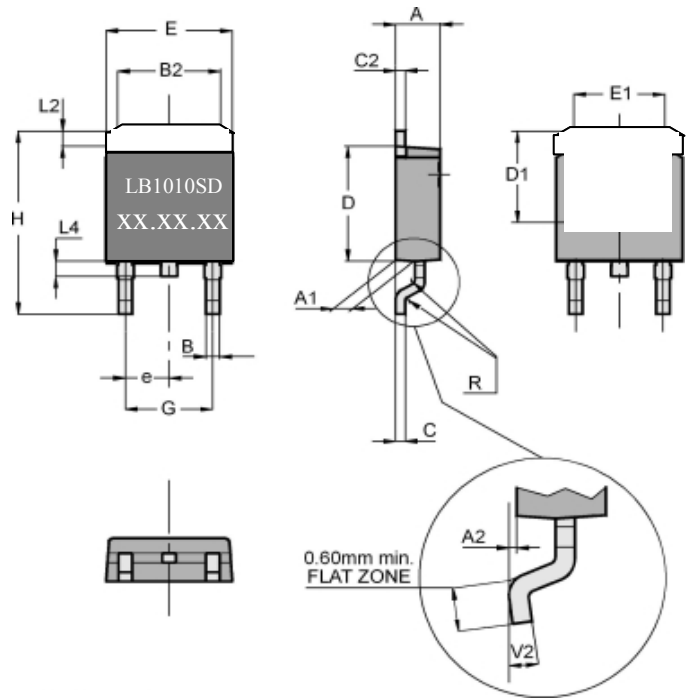
Figure 12 – Normalized Thermal Response

**Ordering Information**

Product Number	PN Marking	Package
LB1010SD	LB1010SD	TO263 (D2PAK)

Package and Marking Information**D2PAK DIMENSIONS**

DIM.	mm.			inch		
	TYP.	MIN.	MAX.	TYP.	MIN.	MAX.
A		4.06	4.83		0.160	0.190
A1		2.05	2.79		0.08	0.11
A2		0.03	0.23		0.001	0.009
B		0.51	0.89		0.020	0.035
B2						
C		0.45	0.60		0.018	0.025
C2		1.14	1.40		0.045	0.055
D		8.65	9.65		0.340	0.380
D1						
E		9.65	10.29		0.380	0.405
E1						
e	2.54			0.100		
G	5.08			0.200		
H		14.60	15.88		0.575	0.625
L2		1.14	1.40	0.031	0.045	0.055
L4		0.60	1.00	0.023	0.039	
R	0.20			0.008		
V2		0°	8°		0°	8°

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Datasheet Identification	Product Status	Definition
Advance Information	In definition or in Design	This datasheet contains the design specifications for product development. Specifications may change without notice.
Preliminary	Initial Production	This datasheet contains preliminary data; additional and application data will be published at a later date. Lovoltech, Inc. reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	In Production	This datasheet contains final specifications. Lovoltech reserves the right to make changes at any time without notice in order to improve the design.