PWRLITE LVTD103N

High Performance N-Ch Vertical Power JFET Transistor “No Diode”

Features

- Trench Power JFET with low threshold voltage Vth.
- Device fully “ON” with Vgs = 0.7V
- Optimum for “Low Side” Buck Converters
- Optimized for Secondary Rectification in isolated DC-DC Converters
- Low Rg and low Cds for high speed switching
- No “Body Diode”; extremely low Cds

Applications

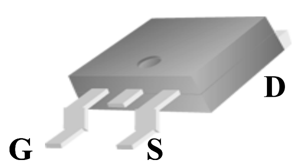
- DC-DC Converters
- Synchronous Rectifiers
- PC Motherboard Converters
- Step-down power supplies
- Brick Modules
- VRM Modules

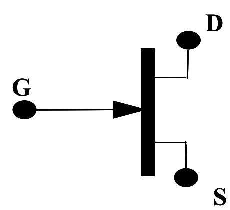
Description

The Power JFET transistor from Lovoltech is a device that presents a Low Rdson allowing for improved efficiencies in DC-DC switching applications. The device is designed with a low threshold such that drivers can operate at 5V, which reduces the driver power dissipation and increases the overall efficiency. Lower threshold produces faster turn-on/turn-off, which minimizes the required dead time. The transistor “No Body Diode” provides a very low associated parasitic capacitance Cds. Ringing is also reduced so that a lower voltage device may be a better solution.

Advanced Information

DPAK Pin Assignments





N – Channel Power JFET

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	Gate	**Gate.** Transistor Gate
2	Drain	**Drain.** Transistor Drain
3	Source	**Source.** Transistor Source

Product Summary		
V_{DS} (V)	Rdson (Ω)	I_D (A)
25V	0.005 @ Ig = 10mA	50
25V	0.0045 @ Ig = 40mA	50

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Units
Drain-Source Voltage	V_{DS}	25 (selection @ 30V)	V
Gate-Source Voltage	V_{GS}	-10	V
Gate-Drain Voltage	V_{GD}	-25(selection @ -30V)	V
Continuous Drain Current	I_D	50	A
Pulsed Drain Current	I_D		A
Junction Temperature	T_J	-55 to 150°C	°C
Storage Temperature	-65 to 150°C	-65 to 150°C	-65 to 150°C
Lead Soldering Temperature, 10 seconds	300°C	300°C	300°C
Power Dissipation (derated at 25°C)	P_D	80	W

Thermal Resistance

Symbol	Parameter		DPAK Ratings		Units
$R\Theta_{JA}$	Thermal Resistance Junction-to-Ambient		80		°C/W
$R\Theta_{JC}$	Thermal Resistance Junction-to-Case		1.6		°C/W

Electrical Specifications

(T_A = +25°C, unless otherwise noted.)

The ϕ denotes specifications which apply over the full operating temperature range.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
	Static						
BV_{DSX}	Breakdown Voltage Drain to Source	See Figure 3	ϕ		25		V
BV_{GDO}	Breakdown Voltage Gate to Drain	I_G = -50µA	ϕ		-25		V
BV_{GSO}	Breakdown Voltage Gate to Source	I_G = -1 mA	ϕ		-11	-10	V
$R_{DS(ON)}$)	Static Drain to Source[1] On Resistance (Current flows drain-to-source) See Fig. 1	I_G = 40 mA, I_D=10A I_G = 10 mA, I_D=10A			4.5 5.0	5.5 6	mΩ mΩ mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=0.1 V, I_D=250µA	ϕ	-0.4	-0.3	-0.2	V
	Dynamic						
Q_G	Total Gate Charge	ΔV_{Drive} =5V, I_D=15A,V_{DS}=16V			20		nC
Q_{GD}	Gate to Drain Charge				12		nC
Q_{GS}	Gate to Source Charge				1.5		nC
Q_{SW}	Switching Charge				13.5		nC
R_G	Gate Resistance				0.3		Ω
$T_{D(ON)}$)	Turn-on Delay Time		ϕ		5		
T_R	Rise Time	V_{DD}=16V, I_D=15A V_{Drive} = 5 V Clamped Inductive Load	ϕ		12		ns
$T_{D(OFF)}$	Turn-off Delay				2		
T_F	Fall Time				10		
C_{ISS}	Input Capacitance				3000		
C_{OSS}	Output Capacitance				760		
C_{GS}	Gate-Source Capacitance	V_{DS}=10V, V_{GS}= -5 V, 1MHz.			2250		pF
C_{GD}	Gate-Drain Capacitance				750		
C_{DS}	Drain-Source Capacitance				10		

Notes:

1. Pulse width <= 500µs, duty cycle < = 2%

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Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

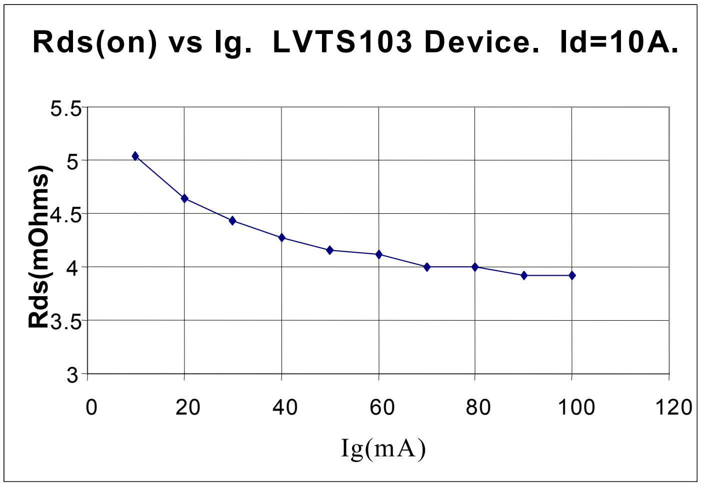


Figure 1 – R_{DSON} vs Gate Current at I_D – 10A

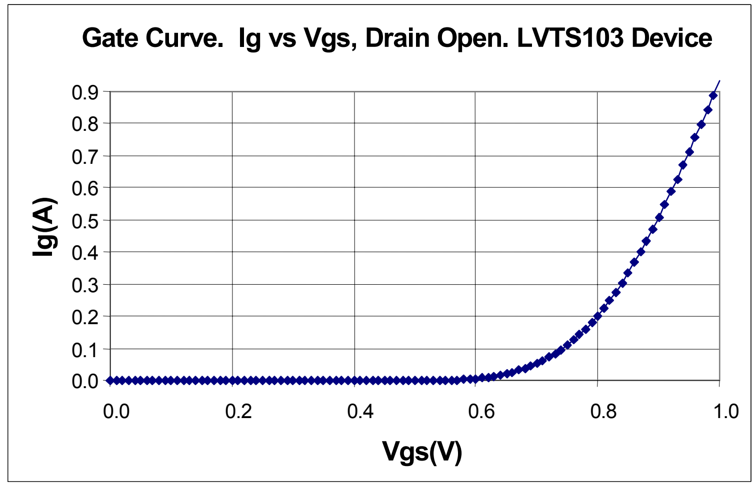


Figure 2 – I_G vs Gate Voltage V_{GS}

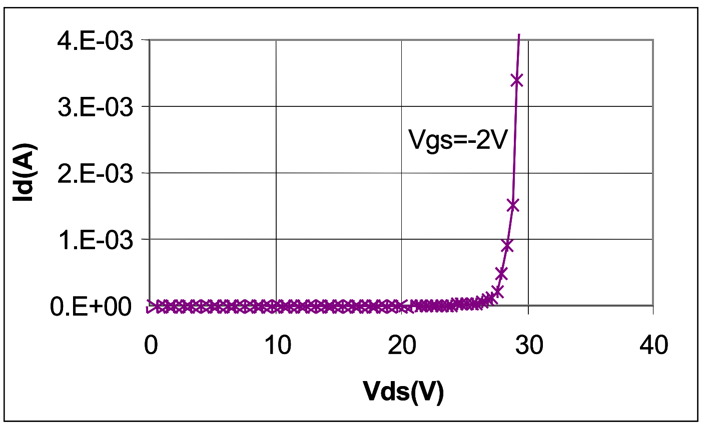


Figure 3 – Breakdown Voltage Vds

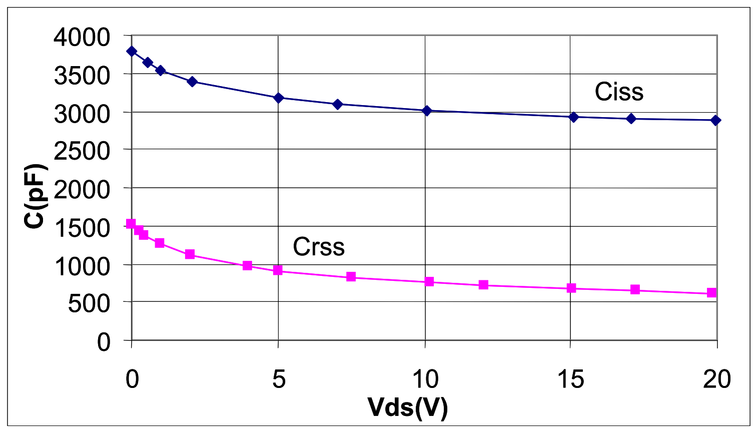


Figure 4 – Capacitance vs Drain Voltage Vds

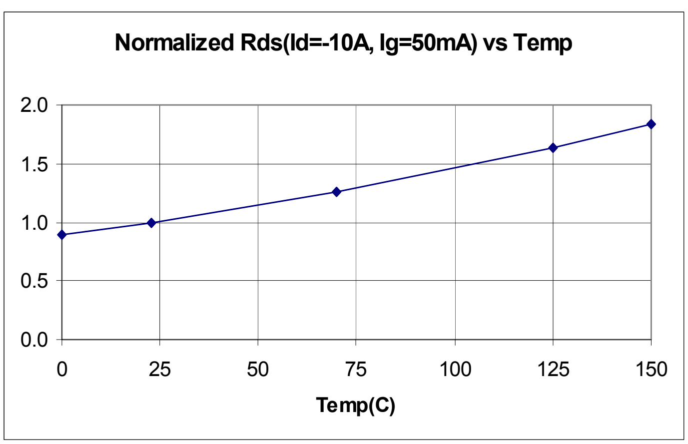


Figure 5 – Normalized On-Resistance vs. Temperature

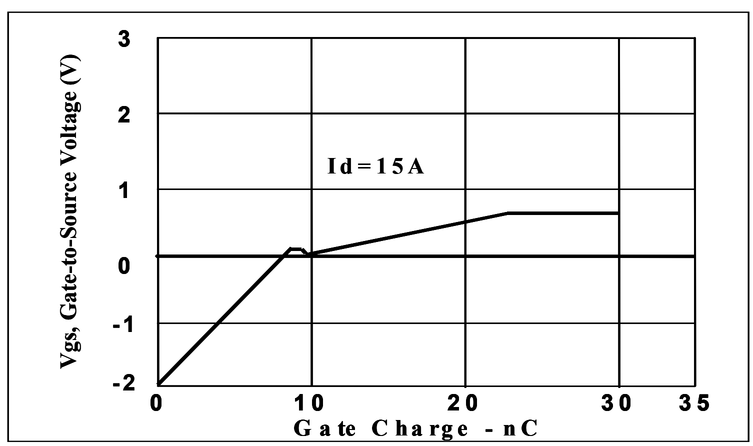


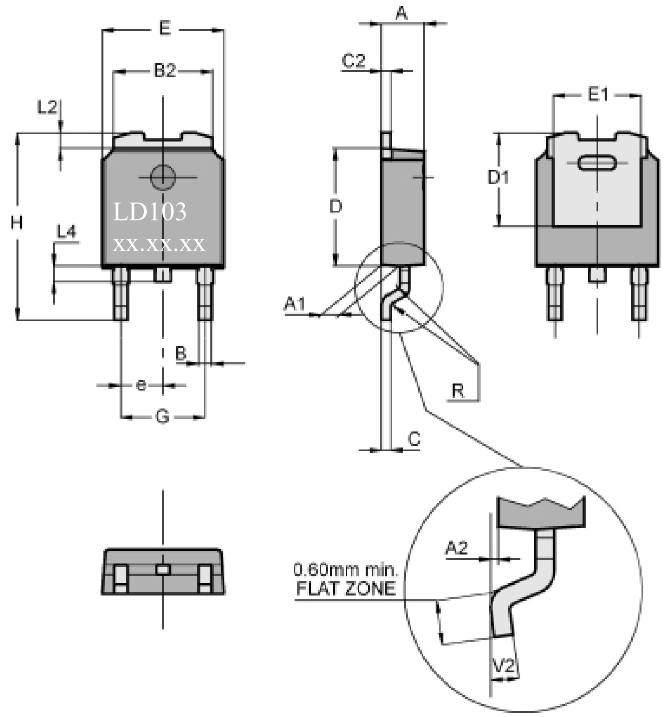
Figure 6 – Typical Gate Charge vs. Gate-to-Source Voltage

Ordering Information

Product Number	PN Marking	Package
LD103Nx x= 0, 2, 5, 6	LD103Nx x = Lot Source	TO252 (DPAK)

Package and Marking Information

DPAK DIMENSIONS						
DIM.	mm.			inch		
	TYP.	MIN.	MAX.	TYP.	MIN.	MAX.
A		2.20	2.40		0.086	0.094
A1		0.90	1.10		0.035	0.043
A2		0.03	0.23		0.001	0.009
B		0.64	0.90		0.025	0.035
B2		5.20	5.40		0.204	0.212
C		0.45	0.60		0.017	0.023
C2		0.48	0.60		0.019	0.023
D		6.00	6.20		0.236	0.244
D1	5.10			0.201		
E		6.40	6.60		0.252	0.260
E1	4.70			0.185		
e	2.28			0.090		
G		4.40	4.60		0.173	0.181
H		9.35	10.10		0.368	0.397
L2	0.80			0.031		
L4		0.60	1.00		0.023	0.039
R	0.20			0.008		
V2		0°	8°		0°	8°



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Datasheet Identification	Product Status	Definition
Advance Information	In definition or in Design	This datasheet contains the design specifications for product development. Specifications may change without notice.
Preliminary	Initial Production	This datasheet contains preliminary data; additional and application data will be published at a later date. Lovoltech, Inc. reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	In Production	This datasheet contains final specifications. Lovoltech reserves the right to make changes at any time without notice in order to improve the design.

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