LSI402Z Digital Signal Processor

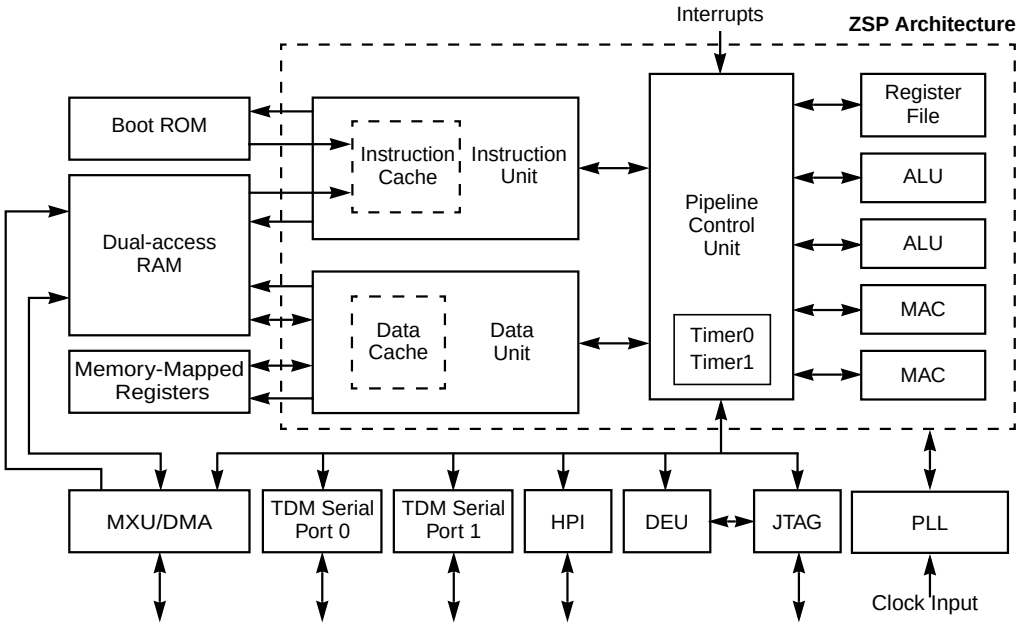
Preliminary Datasheet

The LSI402Z is a 16-bit fixed-point digital signal processor (DSP) based on the LSI Logic superscalar ZSP™ architecture. The LSI402Z is designed for applications requiring high throughput and flexibility coupled with high speed I/O, such as communications infrastructure equipment.

The LSI402Z operates at a maximum clock rate of 200 MHz for a sustained effective throughput of 400 DSP MIPS. The LSI402Z's RISC architecture is easy to program and uses a four-way superscalar pipeline with five stages to process up to 20 instructions at a time. The processor's execution unit contains two multiply-accumulate units (MACs) and two arithmetic logic units (ALUs). The LSI402Z also supports single cycle add-compare-select, bit manipulation and 32-bit arithmetic and logic operations.

Figure 1 shows a block diagram of the LSI402Z.

Figure 1 LSI402Z Block Diagram



The LSI402Z provides 62 Kwords of dual-access RAM supported by an eight channel DMA controller, which can transfer instructions and data. For optimum I/O performance and flexibility, the LSI402Z contains two high speed time-division multiplex (TDM) serial ports, a single 16-bit host interface port, an external memory interface unit, and an eight-pin programmable I/O port. An IEEE 1149.1 JTAG port supports system download and debug.

LSI Logic provides a software development kit containing an assembler, linker, GUI debugger, profiler, C compiler, and JTAG-based hardware emulator.

The LSI402Z is fabricated in LSI Logic G12™-p technology. The LSI402Z is powered by a 1.8 V core and a 3.3 V I/O supply, and is packaged in a 208-ball mini-BGA package.

LSI402Z Overview and Features

Processor

- RISC architecture
  - Instruction grouping by hardware for parallel execution
- Four-way superscalar architecture
  - Two multiply-accumulate units (MAC)
  - Two arithmetic logic units (ALUs)
- 400 MIPS maximum throughput at 200 MHz (1.8 V nominal V_{DD})
- Multitasking support
  - Low latency interrupt structure with programmable priority levels
  - Efficient context switch support

Applications

- Optimized for communications infrastructure applications
  - Single-cycle dual 16-bit MAC with 40-bit result
  - Single-cycle high-precision (32-bit) MAC with 40-bit result
  - Two-cycle complex multiply
  - Single-cycle add-compare-select for Viterbi decoding

Technology

- 208-ball mini-BGA package
- Low power dissipation: 860 mW typical at 200 MHz; 1 W (max) at 200 MHz (two MACs per cycle, peak internal memory access)

Memory

- 62 Kword internal dual-access RAM
- Eight channel DMA
  - Supports fast I/O transfers without cycle stealing
  - Transfer instructions or data to and from internal memory
- 32-bit external memory interface unit
  - Glueless interface to SRAMs and SBSRAMs
  - 20-bit address space (1 Mwords) for both instruction and data memory
- 2 Kword internal boot ROM

I/O

- Two high speed serial ports with time-division multiplex (TDM) mode
  - H.100 / H.110 bit stream compatible
- 16-bit host processor interface
- 8-pin programmable I/O port
- IEEE 1149.1 compliant JTAG port

Timers

- Two 16-bit timers with a 6-bit prescale value
- Single-shot and continuous mode

Phase-Locked Loop (PLL)

- On-chip PLL for clock generation

Functional Description

The LSI402Z contains an entire DSP system and allows attachment of external memory and peripherals. Refer to Figure 1 for a block diagram of the LSI402Z.

The pipeline control unit groups instructions, resolves dependencies, and schedules instructions for execution by the execution unit. The pipeline control unit also processes interrupt requests forwarded from the interrupt control unit.

The LSI402Z contains a four-way superscalar five-stage pipeline. At any time, up to 20 instructions may be in the various stages of the pipeline. The five pipeline stages of this machine are: Fetch/Decode (F/D), Group (G), Read (R), Execute (E), and Write (W).

The pipeline control unit also contains two 16-bit timers for interrupt generation. Each timer is fully programmable and has a 6-bit prescaler. Once enabled, the timers count down from the user-specified initial value to zero at a rate determined by the scaled output of the LSI402Z output clock. The timers generate an interrupt when zero is reached. The timers can be configured to automatically reload with the initial count to generate periodic interrupts.

The interrupt control unit interfaces with the pipeline control unit. A nonmaskable interrupt (NMI) pin into the LSI402Z allows for a separate interrupt control unit.

The data unit fetches data and sends them to the data cache. The data unit contains the data prefetcher and cache, and contains the logic for two circular buffers.

The instruction unit fetches instructions, decodes and dispatches them, and places the instructions in the instruction cache. The instruction unit contains the instruction cache, the instruction prefetcher, and the instruction dispatch unit. The instruction unit also contains branch prediction logic.

The control register file contains a set of 32 16-bit control registers, used for mode control, status, and flag information.

The execution unit performs all arithmetic and logical operations in the LSI402Z. The execution unit contains two 16 bit arithmetic logic units (ALUs), two 16 x 16 multiply and accumulate (MAC) units, and a general purpose (operand) register file.

The two ALUs are identical and can be combined as a single 32-bit ALU. The MAC units can perform two 16-bit x 16-bit multiply operations and a single 40-bit accumulation per cycle or one 32-bit x 32-bit multiply operation and a single 40-bit accumulation per cycle.

The boot ROM provides processor self-test capabilities and JTAG- and UART-based emulation support.

The LSI402Z's 8-channel DMA controller reduces the interrupt overhead during data transfers to or from internal memory. Each channel supports zero-overhead instruction or data transfers to or from the entire 62 Kwords of internal dual-access RAM to either the memory interface unit (external memory), one of the serial ports, or the host processor interface. The eight DMA channels are segmented between four nonindexed and four indexed channels.

Nonindexed DMA channels perform only sequential accesses to or from internal memory. A transfer occurs at the specified memory location whenever an interrupt from the specified peripheral request occurs. The interrupt request may come from the host processor interface or one of the two serial ports. After the interrupt, the pointer register updates with the next internal memory location. When the DMA channel pointer reaches the buffer length, the processor generates a DMA interrupt request and terminates the DMA transaction.

Indexed DMA channels perform sequential or indexed accesses to or from internal memory. These channels are designed specifically to work with the TDM serial ports. Data buffers can read from or write to DSP memory corresponding to logical TDM channels (time slots). The user specifies the buffer length and the number of buffers to service, and the DMA controller automatically updates the pointer for each transfer within a frame. When a frame transfer completes, the pointer updates the memory address and begins transferring data for the next frame.

When the DMA channel pointer reaches the last location of the last buffer, the processor generates a DMA interrupt and sets the bit

corresponding to the channel in the DMA status register. This terminates the DMA transaction.

The memory interface unit connects the LSI402Z to off-chip memory or peripherals through a 32-bit data bus and a pin-multiplexed 20-bit address bus. Simultaneous address and data transfers are not allowed. The memory interface unit provides a glueless interface to 16-bit asynchronous memory devices (ROM, EPROM, and SRAM) and 32-bit synchronous-burst SRAMs (SBSRAM).

The LSI402Z contains two identical serial ports capable of 8- or 16-bit active or passive transfers. In active mode, the serial port generates its own bit clock and sync signals. The serial port bit clock frequency is determined by the processor clock rate divided by a user-specified value. The maximum transfer rate in both modes is one-half the processor clock rate.

Both serial ports of the LSI402Z provide a time-division multiplex (TDM) mode compatible with T1/E1 framers or the local serial bus of H.100/H.110 interface devices. The TDM mode can also be used to establish a serial multiprocessor communication link with only three signals. The user selects the word length (8- or 16-bits) and frame length (1–128 time slots) for TDM transfers. Transmit and receive time slots are programmed individually and can be modified on the fly.

The host processor interface (HPI) provides an asynchronous 16-bit parallel port for interfacing with off-chip devices. The HPI is compatible with both Motorola and Intel style memory interfaces, and supports word transfers.

The HPI transfers data at a maximum rate of one-half the processor clock frequency. The control, transmit data, and receive data registers are memory-mapped.

Eight programmable I/O signals support general-purpose hardware interface. Each programmable I/O may be configured as either an input or an output pin.

The JTAG port is an IEEE 1149.1-compliant test access port (TAP). When coupled with the device emulation unit, JTAG provides access to all on-chip resources. The DEU works in conjunction with code residing in the internal ROM to provide full-speed in-circuit emulation, allowing full visibility and control of the device memory and registers. Using the JTAG

port, device emulation unit, and internal ROM together provides the capability to download code to internal and external RAM.

The LSI402Z uses a phase-locked loop (PLL) to generate a high frequency processor clock from a slower, off-chip external clock source. The off-chip clock source is applied to the CLKIN pin of the DSP and must be a crystal oscillator within the frequency range of 2 to 40 MHz. The CLKOUT pin reflects the processor clock frequency. The processor clock can use an off-chip clock source directly by bypassing the on-chip PLL.

Instruction Set Summary

Table 1 summarizes the ZSP instruction set used by the LSI402Z.

Table 1 ZSP Instruction Set

Instruction	Description
ABS	Absolute Value
ABS.E	Absolute Value (Extended Precision)
ADD	Add Immediate/Registers
ADD.E	Add Registers (Extended Precision)
ADDC.E	Add With Carry (Extended Precision)
AGN0	Again 0
AGN1	Again 1
AND	Logical AND
AND.E	Logical AND (Extended Precision)
BC	Branch on Carry
BGE	Branch on Greater Than or Equal To
BGT	Branch on Greater Than
BITC	Bit Clear Control/Operand Register
(Sheet 1 of 6)	

Table 1 ZSP Instruction Set (Cont.)

Instruction	Description
BITI	Bit Invert Control/Operand Register
BITS	Bit Set Control/Operand Register
BITT	Bit Test Control/Operand Register
BLE	Branch On Less Than Or Equal To
BLT	Branch On Less Than
BNC	Branch On No Carry
BNZ	Branch On Not Zero
BNOV	Branch On No Overflow
BOV	Branch On Overflow
BR	Unconditional Branch
BZ	Branch On Zero
CALL	Call Label/Operand Register
CMACR.A	Complex MAC Real To Accumulator A
CMACR.B	Complex MAC Real To Accumulator B
CMACI.A	Complex MAC Imaginary To Accumulator A
CMACI.B	Complex MAC Imaginary To Accumulator B
CMP	Compare Immediate/Register To Register
CMP.E	Compare (Extended Precision)
CMULR.A	Complex Multiplication Real To Accumulator A
CMULR.B	Complex Multiplication Real To Accumulator B
CMULI.A	Complex Multiplication Imaginary To Accumulator A
CMULI.B	Complex Multiplication Imaginary To Accumulator B
DMAC.A	Double MAC To Accumulator A
DMAC.B	Double MAC To Accumulator B
(Sheet 2 of 6)	

Table 1 ZSP Instruction Set (Cont.)

Instruction	Description
DMUL.A	Multiplication (Extended Precision) To Accumulator A
DMUL.B	Multiplication (Extended Precision) To Accumulator B
IMUL.A	Integer Multiply To Accumulator A
IMUL.B	Integer Multiply To Accumulator B
LD	Load
LDU	Load With Update
LDDU	Load Double With Update
LDX	Load With Register Based Offset
LDXU	Load With Register Based Offset And Update
MAC2.A	Dual MAC To Accumulator A
MAC2.B	Dual MAC To Accumulator B
MAC.A	Multiply Accumulate To Accumulator A
MAC.B	Multiply Accumulate To Accumulator B
MACN.A	Multiply Accumulate With Negation To Accumulator A
MACN.B	Multiply Accumulate With Negation To Accumulator B
MAX	Maximum
MAX.E	Maximum (Extended Precision)
MIN	Minimum
MIN.E	Minimum (Extended Precision)
MOV	Move To PC
MOV	Move Operand Register To Control Register
MOV	Move Control Register To Operand Register
MOV	Move Operand Register To Operand Register
MOV	Move Immediate To Operand Register
(Sheet 3 of 6)	

Table 1 ZSP Instruction Set (Cont.)

Instruction	Description
MOVH	Move Immediate To Higher Byte Of Control Register
MOVH	Move Immediate To Higher Byte Of Operand Register
MOVL	Move Immediate To Lower Byte Of Control Register
MOVL	Move Immediate To Low Byte Of Operand Register
MUL.A	Multiply To Accumulator A
MUL.B	Multiply To Accumulator B
MULN.A	Multiply With Negation To Accumulator A
MULN.B	Multiply With Negation To Accumulator B
NEG	Negate
NEG.E	Negate (Extended Precision)
NOP	No Operation
NORM	Normalize
NORM.E	Normalize (Extended Precision)
NOT	Logical Not
NOT.E	Logical Not (Extended Precision)
OR	Logical Or
OR.E	Logical Or (Extended Precision)
PADD.A	Parallel Add Registers To Accumulator A
PADD.B	Parallel Add Registers To Accumulator B
PSUB.A	Parallel Subtract Registers To Accumulator A
PSUB.B	Parallel Subtract Registers To Accumulator B
RET	Return From Subroutine
RETI	Return From Interrupt
REVB	Reverse Bit
(Sheet 4 of 6)	

Table 1 ZSP Instruction Set (Cont.)

Instruction	Description
ROUND.E	Round (Extended Precision)
SHLA	Shift Left Arithmetic Immediate
SHLA	Shift Left Arithmetic Register
SHLA.E	Shift Left Arithmetic Immediate (Extended Precision)
SHLA.E	Shift Left Arithmetic Register (Extended Precision)
SHLL	Shift Left Logical Immediate
SHLL	Shift Left Logical Register
SHLL.E	Shift Left Logical Immediate (Extended Precision)
SHLL.E	Shift Left Logical Register (Extended Precision)
SHRA	Shift Right Arithmetic Immediate/Register
SHRA.E	Shift Right Arithmetic Immediate/Register (Extended Precision)
SHRL	Shift Right Logical Immediate/Register
SHRL.E	Shift Right Logical Immediate/Register (Extended Precision)
ST	Store
STU	Store With Update
STDU	Store Double With Update
STX	Store With Register Based Offset
STXU	Store With Register Based Offset And Update
SUB	Subtract
(Sheet 5 of 6)	

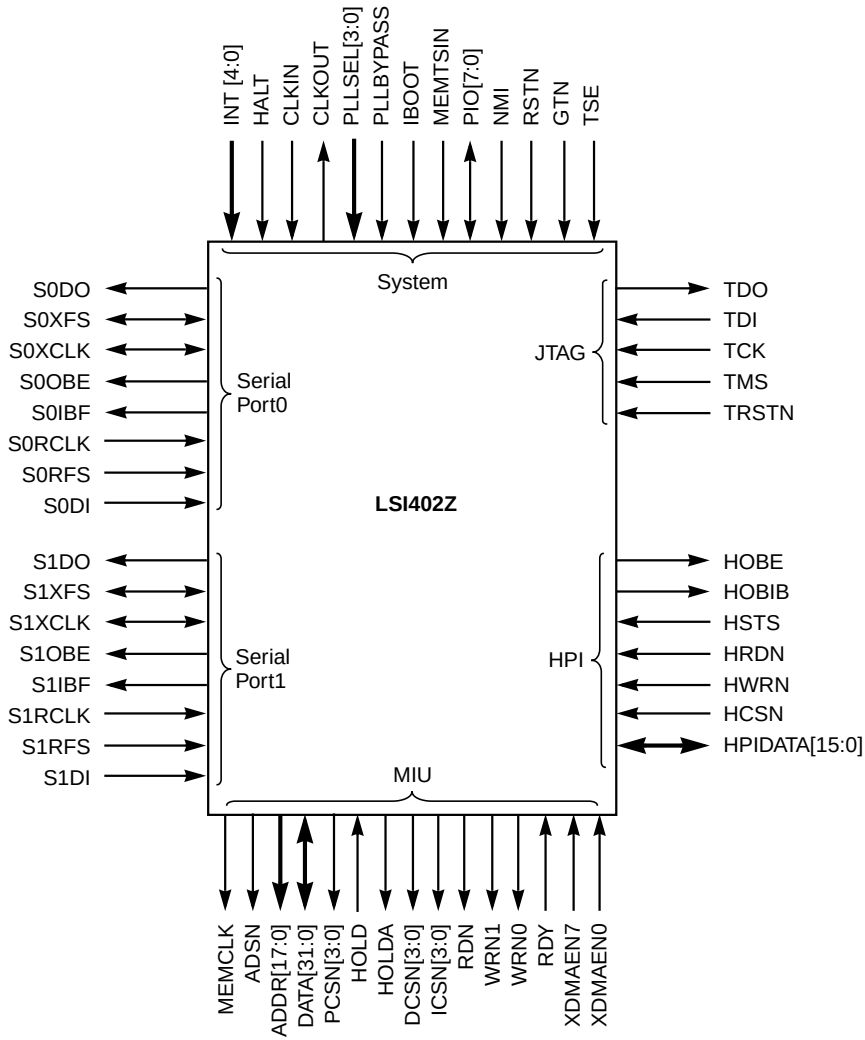
Table 1 ZSP Instruction Set (Cont.)

Instruction	Description
SUB.E	Subtract (Extended Precision)
SUBC.E	Subtract With Carry (Extended Precision)
VIT_A	Viterbi Instruction For Point A
VIT_B	Viterbi Instruction For Point B
XOR	Exclusive Or
XOR.E	Exclusive Or (Extended Precision)
(Sheet 6 of 6)	

Signal Descriptions

This section describes all external LSI402Z signals. Figure 2 shows the LSI402Z interface.

Figure 2 LSI402Z System Interfaces



The signals have been divided into the following tables:

Table 2 System Interface Signals

Signal	I/O	Description
CLKIN	Input	Clock Source
CLKOUT	Output	Clock Output
GTN	Input	Global 3-State Enable
HALT	Input	Stop The Processor Clock
IBOOT	Input	Memory Map Select
INT[4:0]	Input	External Hardware Interrupts
MEMTSTN	Input	Memory Test Enable
NMI	Input	Nonmaskable Interrupt
PIO[7:0]	Bidirectional	Programmable I/O
PLLBYPASS	Input	PLL Bypass
PLLSEL[3:0]	Input	PLL Mode Select
RSTN	Input	Device Reset
TSE	Input	Test Scan Enable

Table 3 Memory Interface Unit (MIU) Signals

Signal	I/O	Description
ADDR[17:0]	Output	External Memory Address Bus
ADSN	Output	SBSRAM Address Strobe
DATA[31:0]	Bidirectional	External Memory Data Bus
DCSN[3:0]	Output	Data Memory Chip Select
HOLD	Input	External Memory Access Hold Request
HOLDA	Output	External Memory Access Hold Acknowledge
ICSN[3:0]	Output	Instruction Memory Chip Select
MEMCLK	Output	SBSRAM Clock
PCSN[3:0]	Output	Memory-Mapped Peripheral Chip Select
RDN	Output	Read Strobe
RDY	Input	Reserved. Tie this pin HIGH for compatibility with future ZSP-based devices.
WRN0	Output	Write Strobe (DATA[15:0])
WRN1	Output	Write Strobe (DATA[31:16])
XDMAEN0	Input	External DMA Channel 0 Enable
XDMAEN7	Input	External DMA Channel 7 Enable

Table 4 Serial Port Signals

Signal[1]	I/O	Description
DI	Input	Serial Data In
DO	Output	Serial Data Out
IBF	Output	Input Buffer Full
OBE	Output	Output Buffer Empty
RCLK	Input	Receive Clock
RFS	Input	Receive Frame Sync
XCLK	Bidirectional	Transmit Clock
XFS	Bidirectional	Transmit Frame Sync

1. Each serial port signal exists for both serial port 0 and serial port 1. The signal names are prepended with SP0 and SP1 (for example, SP0DO and SP1DO).

Table 5 Host Processor Interface (HPI) Signals

Signal	I/O	Description
HCSN	Input	Host Chip Select
HOBE	Output	HPI Output Buffer Empty Flag
HOBIB	Output	Host Processor Interface Output Status
HPIDATA[15:0]	Bidirectional	Host Processor Interface Data Bus
HRDN	Input	Intel Mode Read Strobe/Motorola Mode Data Strobe
HSTS	Input	Host Processor Interface Input Status
HWRN	Input	Intel Mode Write Strobe/Motorola Mode Data Direction Select

Table 6 JTAG Interface Signals

Signal	I/O	Description
TCK	Input	Test Clock
TDI	Input	Test Data In
TDO	Output	Test Data Out
TMS	Input	Test Mode Select
TRSTN	Input	Test Port Reset

Functional Waveforms

This section contains functional waveforms for selected LSI402Z operations.

Serial Port TDM Mode Timing

The two serial ports on the LSI402Z can transmit and receive in various modes, including time-division multiplex (TDM) mode. TDM mode is T1/E1 and H.100/H.110 bit stream compatible. Figure 3 shows the timing relationships for TDM mode receive. Table 7 describes the annotations shown in Figure 3.

Figure 3 Serial Port TDM Mode Receive Waveform

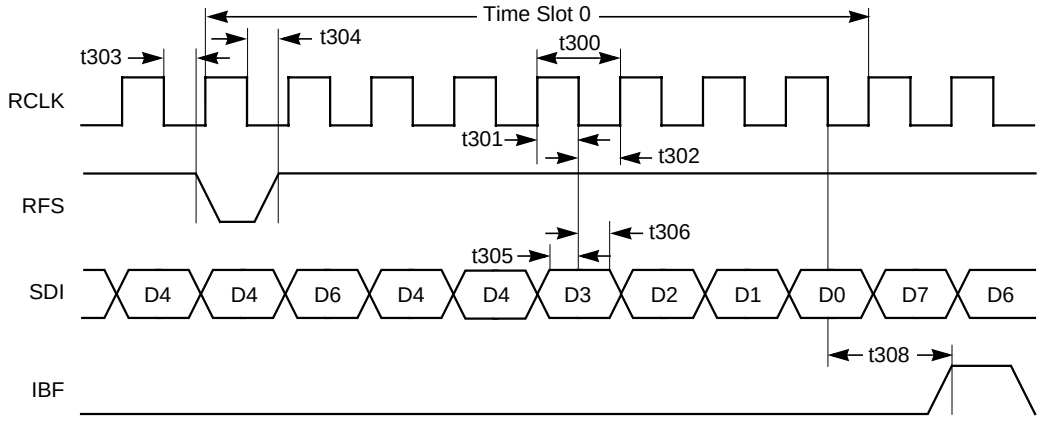


Table 7 Serial Port TDM Mode Receive Timing

Figure Reference	Description	Min	Max	Units
t300	Bit-clock period (RCLK HIGH to RCLK HIGH)	2T	–	ns
t301	Bit-clock LOW time (RCLK LOW to RCLK HIGH)	T	–	ns
t302	Bit-clock HIGH time (RCLK HIGH to RCLK LOW)	T	–	ns
t303	Frame sync hold time (RCLK LOW to RFS HIGH)	1	–	ns
t304	Frame sync hold time	1	–	ns
t305	Data setup time (data valid to RCLK LOW)	4	–	ns
t306	Data hold time (RCLK LOW to Data Invalid)	–	1	ns
t308	RCLK LOW to OBE HIGH	–	2T	ns

Figure 4 shows the timing relationships for TDM transmit mode. Table 8 describes the annotations on Figure 4.

Figure 4 Serial Port TDM Mode Transmit Waveform

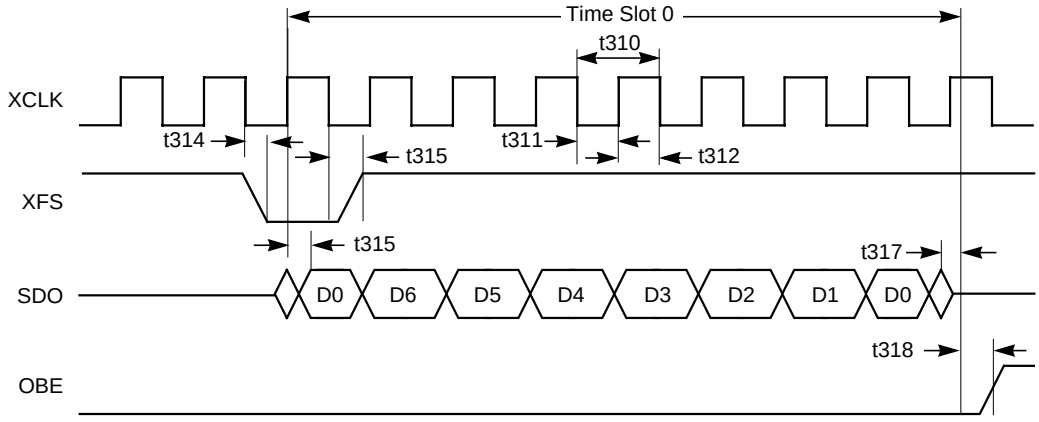


Table 8 TDM Mode Transmit Timing

Reference	Description	Min	Max	Units
t310	Bit-clock period (RCLK LOW to RCLK LOW)	2T	–	ns
t311	Bit-clock low time (RCLK LOW to RCLK HIGH)	T	–	ns
t312	Bit-clock high time (RCLK HIGH to RCLK LOW)	T	–	ns
t314	Frame Sync HIGH Hold Time	1	–	ns
t315	Frame Sync LOW Hold Time (RCLK LOW to XFS HIGH)	1	–	ns
t316	Data Delay Time (LOW to Valid)	–	4	ns
t317	Data Hold Time (HIGH to Invalid)	1	–	ns
t318	OBE Delay Time (LOW to HIGH)	–	0	ns

Memory Interface Unit Timing

The memory interface unit connects the LSI402Z to external memory and peripherals.

Asynchronous Mode

Figure 5 shows the timing relationships for asynchronous external instruction or data reads. Table 9 describes the annotations shown in Figure 5.

Figure 5 Asynchronous External Instruction or Data Memory Read (4 Cycle Wait State)

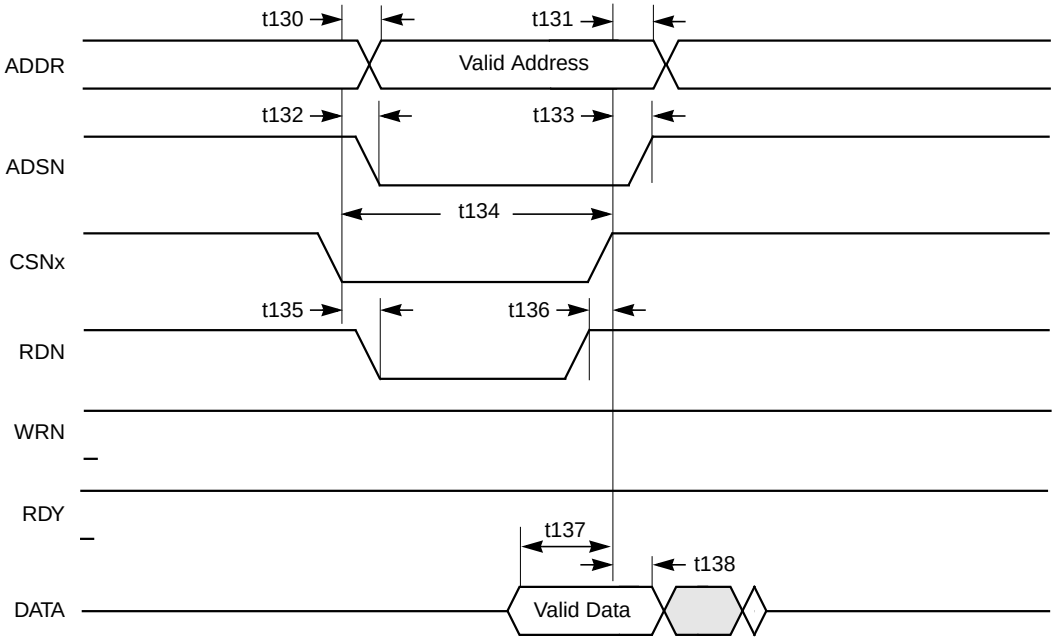


Table 9 External Instruction or Data Read Timing (Asynchronous)

Reference	Description	Min	Max	Unit
t130	CSNx LOW to ADDR Valid	–	1	ns
t131	ADDR Hold Time (CSNx HIGH to ADDR Invalid)	2	–	ns
t132	CSNx LOW to ADSN LOW	–	1	ns
t133	ADSN Hold Time (CSNx HIGH to ADSN HIGH)	0	–	ns
t134	Enable Pulsewidth (CSNx LOW to CSNx HIGH)	T • (csrw + rwpw + rwes)[1]	–	ns

Table 9 External Instruction or Data Read Timing (Asynchronous) (Cont.)

Reference	Description	Min	Max	Unit
t135	CSNx LOW to RDN LOW	–	T • (csrw)[1]	ns
t136	RDN HIGH to CSNx HIGH	–	T • (rwes)[1]	ns
t137	Data Valid to CSNx HIGH	T[1]	–	ns
t138	Data Hold Time	0	–	ns

1. T is the processor clock cycle; csrw, rwpw, and rwes refer to fields in the dwait register.

The memory interface unit connects the LSI402Z to external memory and peripherals. Figure 6 shows the timing relationships for asynchronous external instruction or data reads. Table 10 describes the annotations shown in Figure 6.

Figure 6 Asynchronous External Data Memory Write (4 Cycle Wait State)

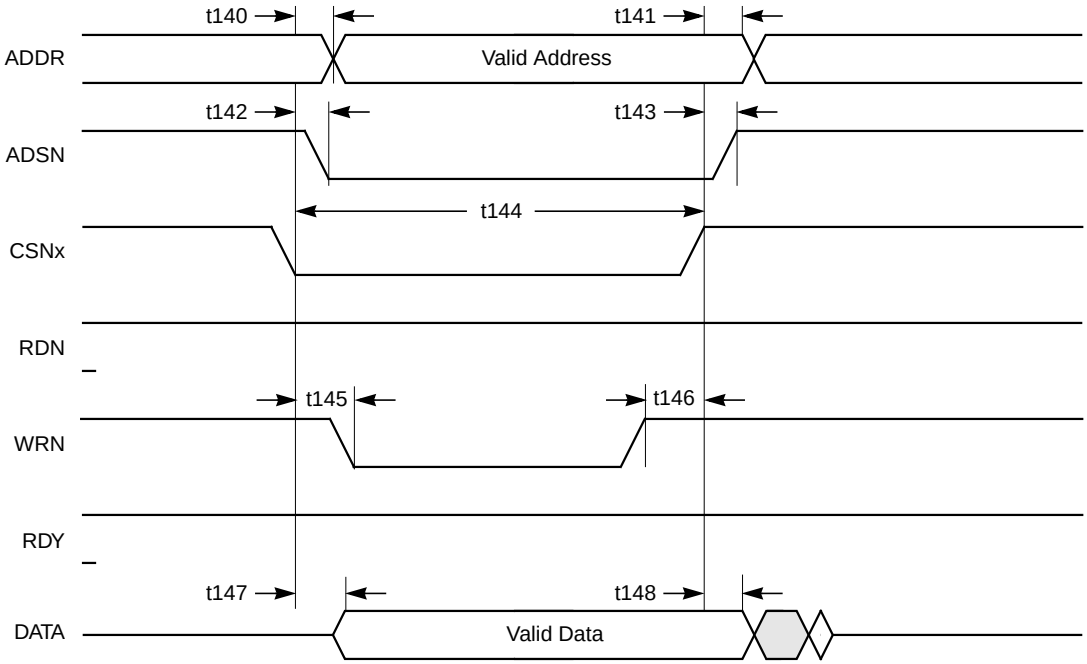


Table 10 External Instruction or Data Write Timing (Asynchronous)

Reference	Description	Min	Max	Units
t140	CSNx LOW to ADDR Valid	–	1	ns
t141	ADDR Hold Time (CSNx HIGH to ADDR Invalid)	2	–	ns
t142	CSNx LOW to ADSN LOW	–	1	ns
t143	ADSN Hold Time (CSNx HIGH to ADSN HIGH)	0	–	ns
t144	CSNx LOW to CSNx HIGH	T • (csrw + rwpw + rwes)[1]	–	ns
t145	CSNx LOW to WRN LOW	–	csrw[1]	ns
t146	WRN HIGH to CSNx HIGH	–	wes[1]	ns
t147	CSNx LOW to Data Valid	–	1	ns
t148	Data Hold Time (CSNx HIGH to Data Invalid)	0	–	ns

1. T is the processor clock cycle; csrw, rwpw, and rwes refer to fields in the dwait register.

Synchronous Mode

Figure 7 shows the timing relationships for synchronous external instruction or data reads. Table 11 describes the annotations shown in Figure 7.

Figure 7 shows the MEMCLK to CLKOUT ratio is 2:1.

Figure 7 Synchronous Mode Timing (Divide by Two)

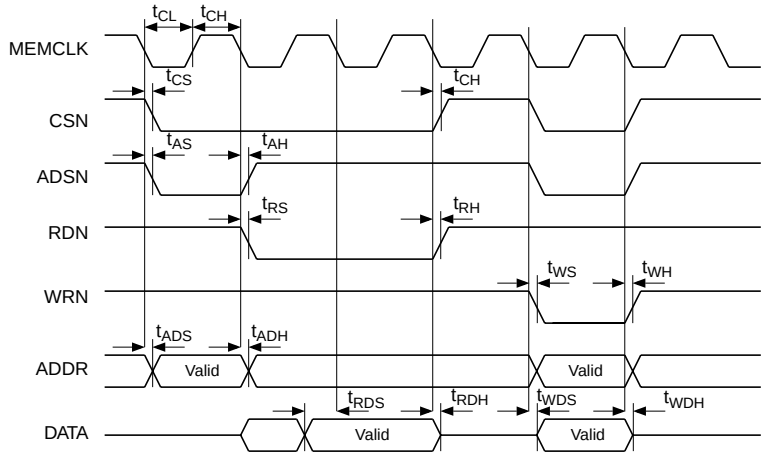


Table 11 Synchronous Memory Timing, 2:1 Mode

Symbol	Description	Min	Max	Units
t_{CL}	Clock LOW	2	–	Cycles
t_{CH}	Clock HIGH	2	–	Cycles
t_{CS}	Clock LOW to CSN LOW	–	1	ns
t_{CH}	Clock LOW to CSN HIGH	–	1	ns
t_{AS}	Clock LOW to ADSN LOW	–	1	ns
t_{AH}	Clock LOW to ADSN HIGH	–	1	ns
t_{RS}	Clock LOW to RDN LOW	–	1	ns
t_{RH}	Clock LOW to RDN HIGH	–	1	ns
t_{ADS}	Clock LOW to ADDR Valid	–	1	ns
t_{ADH}	Clock LOW to ADDR Invalid	–	1	ns

Table 11 Synchronous Memory Timing, 2:1 Mode

Symbol	Description	Min	Max	Units
t_{WS}	Clock Low to WRN Low	–	1	ns
t_{WH}	Clock Low to WRN High	–	1	ns
t_{WDS}	Clock Low to Write Data Valid	–	1	ns
t_{WDH}	Clock Low to Write Data Invalid	–	1	ns
t_{RDS}	Read Data Setup	2	–	ns
t_{RDH}	Read Data Hold	1	–	ns

Host Port Interface Timing

The host processor interface (HPI) provides an asynchronous 16-bit parallel port for interfacing with off-chip devices. The HPI operates in either Intel or Motorola mode.

Figure 8 shows the timing relationships for a host processor read in Intel mode. Table 12 describes the annotations shown in Figure 8.

Figure 8 HPI Host Read, Intel Mode

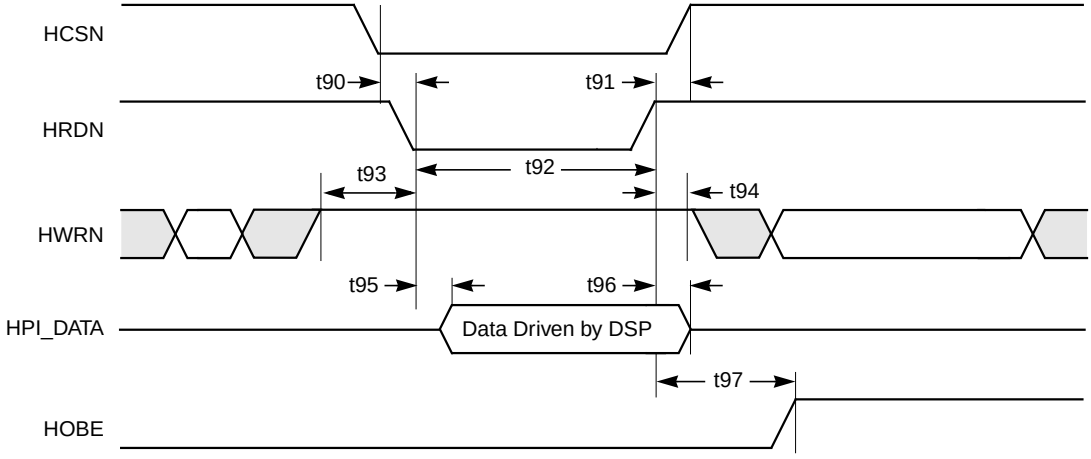


Table 12 HPI Host Read Timing, Intel Mode

Reference	Description	Min	Max	Units
t90	HCSN to HRDN Setup Time (LOW to LOW)	0.5	–	ns
t91	HRDN to HCSN Hold Time (HIGH to HIGH)	0	–	ns
t92	HRDN Pulse Width (LOW to HIGH)	3T	–	ns
t93	HWRN Setup Time (HIGH to LOW)	T	–	ns
t94	HWRN Hold Time	0	–	ns
t95	Data Delay (LOW to Valid)	–	T	ns
t96	Data Hold Time (HIGH to Invalid)	0	–	ns
t97	HOBE Delay Time (HIGH to HIGH)	–	T	ns

Figure 9 shows the timing relationships for a host processor write in Intel mode. Table 13 describes the annotations shown in Figure 9.

Figure 9 HPI Host Write, Intel Mode

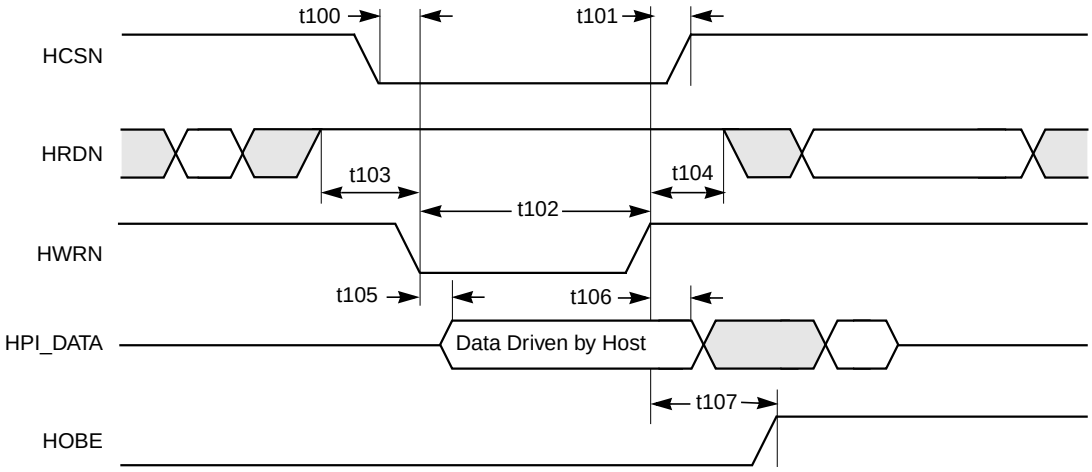


Table 13 HPI Host Write Timing, Intel Mode

Reference	Description	Min	Max	Units
t100	HCSN to HWRN Setup Time (LOW to LOW)	0.5	–	ns
t101	HWRN to HCSN Hold Time (HIGH to HIGH)	0	–	ns
t102	HWRN Pulse Width (LOW to HIGH)	3T	–	ns
t103	HRDN Setup Time (HIGH to LOW)	T	–	ns
t104	HRDN Hold Time	0	–	ns
t105	Data Delay (LOW to Valid)	–	T	ns
t106	Data Hold Time (HIGH to Invalid)	0	–	ns
t107	HOBIB Delay Time (HIGH to HIGH)	–	T	ns

Figure 10 shows the timing relationships for a host processor read in Motorola mode. Table 14 describes the annotations shown in Figure 10.

Figure 10 HPI Host Read, Motorola Mode

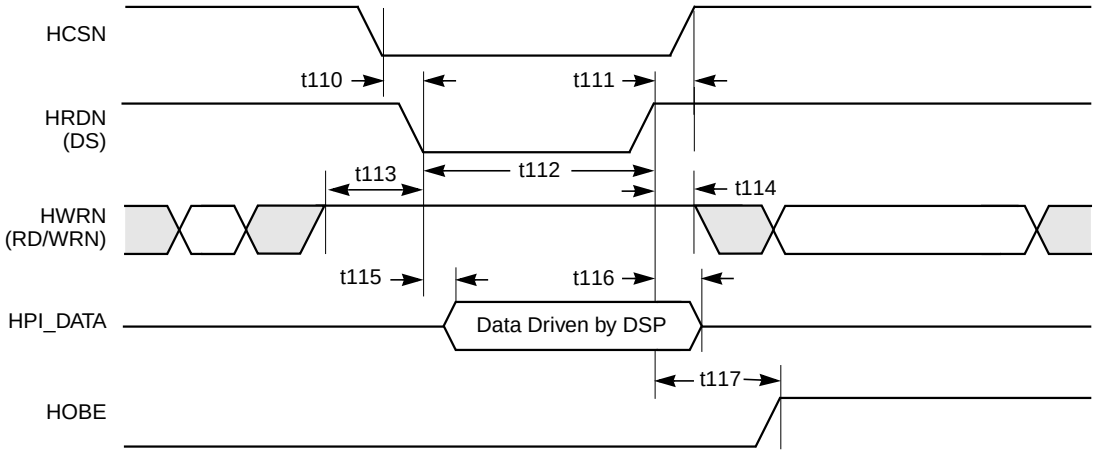


Table 14 HPI Host Read Timing, Motorola Mode

Reference	Description	Min	Max	Units
t110	HCSN to DS Setup Time (LOW to LOW)	0.5	–	ns
t111	DS to HCSN Hold Time (HIGH to HIGH)	0	–	ns
t112	DS Pulse Width (LOW to HIGH)	3T	–	ns
t113	RD/WRN to DS Setup Time (HIGH to LOW)	T	–	ns
t114	DS to RD/WRN Hold Time	0	–	ns
t115	Data Delay (LOW to Valid)	–	T	ns
t116	Data Hold Time (HIGH to Invalid)	0	–	ns
t117	HOBE Delay Time (HIGH to HIGH)	–	T	ns

Figure 11 shows the timing relationships for a host processor write in Motorola mode. Table 15 describes the annotations shown in Figure 11.

Figure 11 HPI Host Write, Motorola Mode

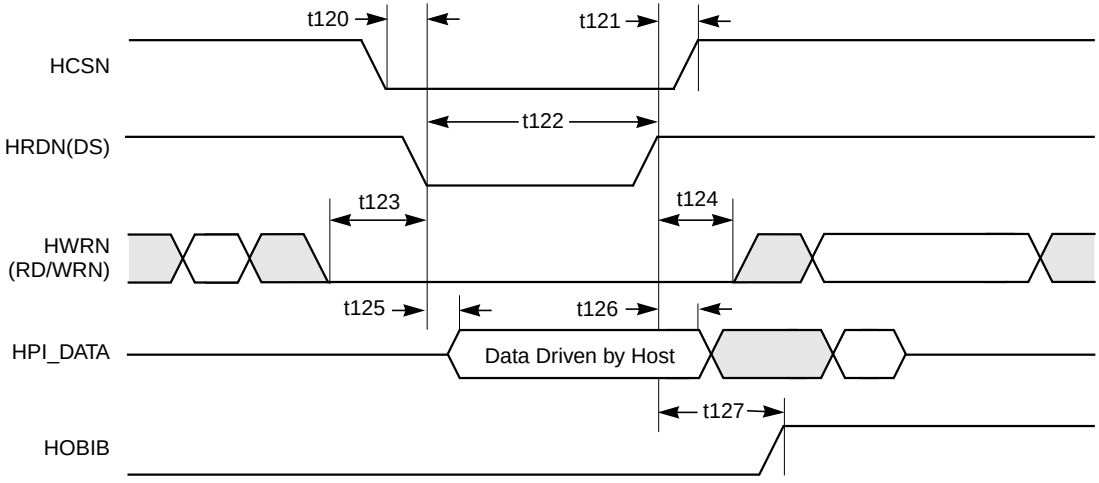


Table 15 HPI Host Write Timing, Motorola Mode

Reference	Description	Min	Max	Units
t120	HCSN to DS Setup Time (LOW to LOW)	0.5	–	ns
t121	DS to HCSN Hold Time (HIGH to HIGH)	0	–	ns
t122	DS Pulse Width (LOW to HIGH)	3T	–	ns
t123	RD / WRN to DS Setup Time (LOW to LOW)	T	–	ns
t124	DS to RD/WRN Hold Time	0	–	ns
t125	Data Delay (LOW to Valid)	–	T	ns
t126	Data Hold Time (HIGH to Invalid)	0	–	ns
t127	HOBIB Delay Time (HIGH to HIGH)	–	T	ns

Specifications

This section describes the electrical and mechanical specifications of the LSI402Z.

Electrical Characteristics

Table 16 lists the DC characteristics for the LSI402Z.

Table 16 Electrical Characteristics

Parameter	Symbol	V_{DD} = 1.8 V, V_{DDIO} = 3.3 V	
		Min	Max
Input Voltage Low High	 V_{IL} V_{IH}	 0 V 2.0 V	 0.8 V V_{DDIO} + 0.3 V
Input Current Low High	 I_{IL} I_{IH}	 –10 µA –	 – 10 µA
Output Low Voltage @ +4 mA (Low)	V_{OL}	–	0.4
Output High Voltage @ -4 mA (High)	V_{OH}	2.4	–
Output 3-State Current Low High	 I_{OZL} I_{OZH}	 –10 µA –	 – –10 µA
Input Capacitance	C_I	–	5.5 pF

Table 17 lists the power dissipation characteristics of the LSI402Z.

Table 17 LSI402Z Power Dissipation

Frequency	Voltage	Power Dissipation
200 MHz	1.8 V	1 W (typical)

Table 18 lists the recommended operating conditions for the LSI402Z.

Table 18 Recommended Operating Conditions

Parameter	Symbol	V_{DD} = 1.8 V, V_{DDIO} = 3.3 V	
		Min	Max
Core Operating Voltage	V_{DD}	1.65	1.95
I/O Operating Voltage	V_{DDIO}	3.0	3.6
Input Voltage	V_I	0	5.0
Output Voltage	V_O	0	V_{DDIO}
Ambient Temperature (Industrial Operating Conditions)	T_A	–10 °C	85 °C

Table 19 lists the absolute maximum ratings for the LSI402Z.

Table 19 Absolute Maximum Ratings

Property	Min	Max
Ambient Temperature Range (°C)	–40	125
Storage Temperature Range (°C)	–65	150
Voltage Range on any pin (V)	–0.5	V_{DDIO} + 0.5
Soldering Temperature for Package Leads (°C)	–	300

Mechanical Specifications

The LSI402Z is packaged in a 208-ball mini-BGA package (package code HG).

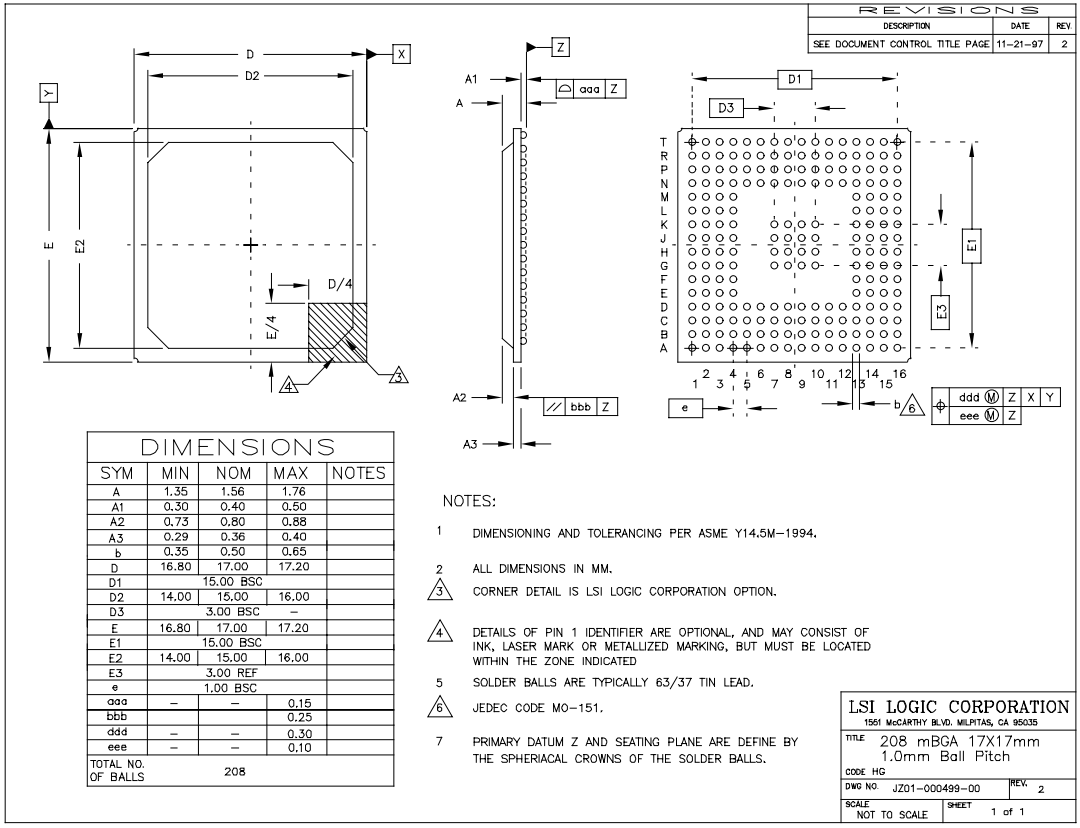
Table 20 Package Thermal Resistance

Package	Maximum Thermal Resistance (θ_{JA})[1]
208 mini-BGA	30 °C/W

1. Still-air ambient.

Figure 12 shows a mechanical drawing of the LSI402Z's package. Figure 13 shows a close-up of the package ball grid.

Figure 12 208 mini-BGA (HG) Mechanical Drawing



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code HG.**

Figure 13 LSI402Z Package (208 Mini-BGA, Bottom View)

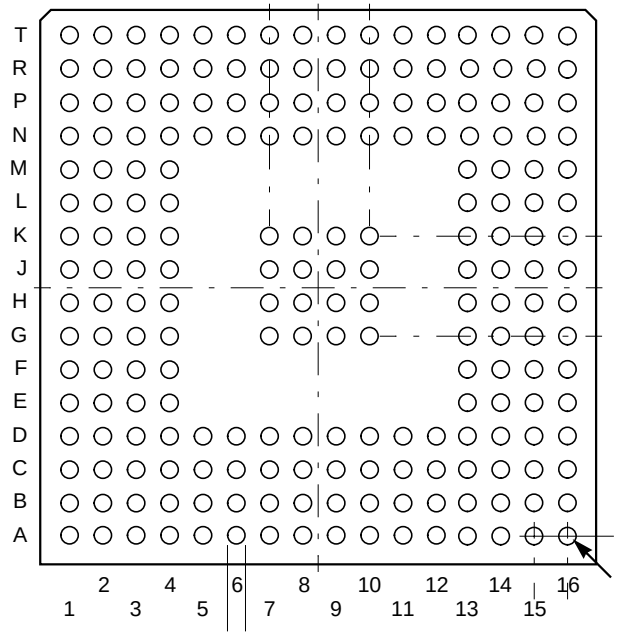


Table 21 lists the mapping of LSI402Z signals to balls on the package. Refer to Figure 13 for the package ball grid.

Table 21 208 Signal to Balls on the Package List

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
ADDR0	L15	DATA21	R4	ICS0N	K14	S1DI	J4	VDDIO	R3
ADDR1	M13	DATA22	T2	ICS1N	K16	S1DO	G1	VDDIO	T16
ADDR2	M14	DATA23	P3	ICS2N	K15	S1IBF	H1	VDDIO	T5
ADDR3	M16	DATA24	R2	ICS3N	L13	S1OBE	H2	VDDIO	T7
ADDR4	M15	DATA25	T1	INT0	B4	S1RCLK	H3	VSS	A6
ADDR5	N15	DATA26	R1	INT1	A4	S1RFS	H4	VSS	D12
ADDR6	P16	DATA27	N2	INT2	C4	S1XCLK	G4	VSS	D16
ADDR7	P15	DATA28	N1	INT3	B5	S1XFS	G3	VSS	F16
ADDR8	R16	DATA29	N3	INT4	A5	TCK	C5	VSS	F2
ADDR9	P14	DATA30	M2	MEMCLK	F15	TDI	C6	VSS	G14
ADDR10	T15	DATA31	M1	MEMTSTN	B1	TDO	D6	VSS	J1
ADDR11	R14	DCS0N	J14	NMI	A3	TMS	B7	VSS	L14
ADDR12	T14	DCS1N	J16	PCS0N	H16	TRSTN	A7	VSS	M3
ADDR13	T13	DCS2N	J15	PCS1N	H14	TSE	B8	VSS	N13
ADDR14	R13	DCS3N	K13	PCS2N	H13	VDD2	A16	VSS	N5
ADDR15	T12	GTN	D5	PCS3N	J13	VDD2	B6	VSS	P11
ADDR16	P12	HALT	C2	PIO0	G2	VDD2	B9	VSS	P13
ADDR17	N12	HCSN	C7	PIO1	F4	VDD2	C12	VSS	P7
ADSN	F14	HOBE	D9	PIO2	F3	VDD2	C3	VSS	P9
CLKIN	C16	HOBIB	D8	PIO3	F1	VDD2	E13	VSS	T3
CLKOUT	B15	HOLD	D3	PIO4	E1	VDD2	E4	VSS2	G10
DATA0	R11	HOLDA	D2	PIO5	E2	VDD2	G13	VSS2	G7
DATA1	T11	HPIDATA0	D10	PIO6	D4	VDD2	M4	VSS2	G8
DATA2	T10	HPIDATA1	C10	PIO7	D1	VDD2	N11	VSS2	G9
DATA3	P10	HPIDATA2	A10	PLLBYPASS	C14	VDD2	N16	VSS2	H10
DATA4	N10	HPIDATA3	B10	PLLSEL0	D15	VDD2	P2	VSS2	H7
DATA5	R9	HPIDATA4	D11	PLLSEL1	D14	VDD2	P5	VSS2	H8
DATA6	T9	HPIDATA5	C11	PLLSEL2	E15	VDD2	R15	VSS2	H9
DATA7	N8	HPIDATA6	A11	PLLSEL3	E16	VDDIO	A12	VSS2	J10
DATA8	P8	HPIDATA7	B11	PLLVDD	C15	VDDIO	A9	VSS2	J7
DATA9	T8	HPIDATA8	B12	PLLVSS	B16	VDDIO	B2	VSS2	J8
DATA10	R8	HPIDATA9	D13	RDN	G16	VDDIO	C9	VSS2	J9
DATA11	N7	HPIDATA10	A13	RDY	E14	VDDIO	E3	VSS2	K10
DATA12	R7	HPIDATA11	C13	RSTN	A1	VDDIO	H15	VSS2	K7
DATA13	N6	HPIDATA12	B13	S0DI	L1	VDDIO	J3	VSS2	K8
DATA14	P6	HPIDATA13	A14	S0DO	J2	VDDIO	L16	VSS2	K9
DATA15	T6	HPIDATA14	B14	S0IBF	K2	VDDIO	L2	WR0N	F13
DATA16	R6	HPIDATA15	A15	S0OBE	K1	VDDIO	N14	WR1N	G15
DATA17	R5	HRDN	A8	S0RCLK	L4	VDDIO	N9	XDMAEN0	A2
DATA18	N4	HSTS	C8	S0RFS	L3	VDDIO	P1	XDMAEN7	B3
DATA19	T4	HWRN	D7	S0XCLK	K3	VDDIO	R10		
DATA20	P4	IBOOT	C1	S0XFS	K4	VDDIO	R12		

Notes

Notes

Sales Offices and Design Resource Centers

LSI Logic Corporation
Corporate Headquarters
Tel: 408.433.8000
Fax: 408.433.8989

NORTH AMERICA

California
Irvine
♦ Tel: 949.553.5600
Fax: 949.474.8101

Pleasanton Design Center
Tel: 925.730.8800
Fax: 925.730.8700

San Diego
Tel: 619.613.8300
Fax: 619.613.8350

Wireless Design Center
Tel: 619.350.5560
Fax: 619.350.0171

Silicon Valley
♦ Tel: 408.433.8000
Fax: 408.954.3353

Colorado
Boulder
Tel: 303.447.3800
Fax: 303.541.0641

Florida
Boca Raton
Tel: 561.989.3236
Fax: 561.989.3237

Georgia
Roswell
Tel: 770.641.8001
Fax: 770.641.8005

Illinois
Schaumburg
♦ Tel: 847.995.1600
Fax: 847.995.1622

Kentucky
Bowling Green
Tel: 502.793.0010
Fax: 502.793.0040

Maryland
Bethesda
Tel: 301.897.5800
Fax: 301.897.8389

Massachusetts
Waltham
♦ Tel: 781.890.0180
Fax: 781.890.6158

Minnesota
Minneapolis
♦ Tel: 612.921.8300
Fax: 612.921.8399

New Jersey
Edison
♦ Tel: 732.549.4500
Fax: 732.549.4802

New York
Fairport
Tel: 716.218.0020
Fax: 716.218.9010

North Carolina
Raleigh
Tel: 919.785.4520
Fax: 919.783.8909

Oregon
Beaverton
Tel: 503.645.0589
Fax: 503.645.6612

Texas
Austin
Tel: 512.388.7294
Fax: 512.388.4171

Dallas
Tel: 972.503.3205
Fax: 972.503.2258

♦ Tel: 972.244.5000
Fax: 972.244.5001

Houston
Tel: 281.379.7800
Fax: 281.379.7818

Washington
Issaquah
Tel: 425.837.1733
Fax: 425.837.1734

Canada
Ontario
Ottawa
♦ Tel: 613.592.1263
Fax: 613.592.3253

Toronto
Tel: 416.620.7400
Fax: 416.620.5005

Quebec
Montreal
♦ Tel: 514.694.2417
Fax: 514.694.2699

INTERNATIONAL

Australia
New South Wales
Reptechnic Pty Ltd
♦ Tel: 612.9953.9844
Fax: 612.9953.9683

China
Beijing
LSI Logic International Services Inc
Tel: 86.10.6804.2534
Fax: 86.10.6804.2521

France
Paris
LSI Logic S.A.
Immeuble Europa
♦ Tel: 33.1.34.63.13.13
Fax: 33.1.34.63.13.19

Germany
Munich
LSI Logic GmbH
♦ Tel: 49.89.4.58.33.0
Fax: 49.89.4.58.33.108

Stuttgart
Tel: 49.711.13.96.90
Fax: 49.711.86.61.428

Hong Kong
Hong Kong
AVT Industrial Ltd
Tel: 852.2428.0008
Fax: 852.2401.2105

India
Bangalore
Spike Technologies India Private Ltd
♦ Tel: 91.80.664.5530
Fax: 91.80.664.9748

Israel
Ramat Hasharon
LSI Logic
♦ Tel: 972.3.5.480480
Fax: 972.3.5.403747

Netanya
VLSI Development Centre
Tel: 972.9.657190
Fax: 972.9.657194

Italy
Milano
LSI Logic S.P.A.
♦ Tel: 39.039.687371
Fax: 39.039.6057867

Japan
Tokyo
LSI Logic K.K.
♦ Tel: 81.3.5463.7821
Fax: 81.3.5463.7820

Osaka
♦ Tel: 81.6.947.5281
Fax: 81.6.947.5287

Korea
Seoul
LSI Logic Corporation of Korea Ltd
♦ Tel: 82.2.528.3400
Fax: 82.2.528.2250

The Netherlands
Eindhoven
LSI Logic Europe Ltd
Tel: 31.40.265.3580
Fax: 31.40.296.2109

Singapore
Singapore
LSI Logic Pte Ltd
♦ Tel: 65.334.9061
Fax: 65.334.4749

Tel: 65.835.5040
Fax: 65.732.5047

Sweden
Stockholm
LSI Logic AB
♦ Tel: 46.8.444.15.00
Fax: 46.8.750.66.47

Switzerland
Brugg/Biel
LSI Logic Sulzer AG
Tel: 41.32.536363
Fax: 41.32.536367

Taiwan
Taipei
LSI Logic Asia-Pacific
♦ Tel: 886.2.2718.7828
Fax: 886.2.2718.8869

Avnet-Mercuries Corporation, Ltd
Tel: 886.2.2503.1111
Fax: 886.2.2503.1449

Jeilin Technology Corporation, Ltd
Tel: 886.2.2248.4828
Fax: 886.2.2242.4397

Lumax International Corporation, Ltd
Tel: 886.2.2788.3656
Fax: 886.2.2788.3568

Prospect Technology Corporation, Ltd
Tel: 886.2.2721.9533
Fax: 886.2.2773.3756

United Kingdom
Bracknell
LSI Logic Europe Ltd
♦ Tel: 44.1344.426544
Fax: 44.1344.481039

♦ Sales Offices with Design Resource Centers

To receive product literature, visit us at http://www.lsilogic.com

ISO 9000 Certified

Printed on Recycled Paper

Printed in USA
Order No. C15033
Doc. No. DB08-000127-01