LSI/CSI

LS7362

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A3800

BRUSHLESS DC MOTOR COMMUTATOR/CONTROLLER

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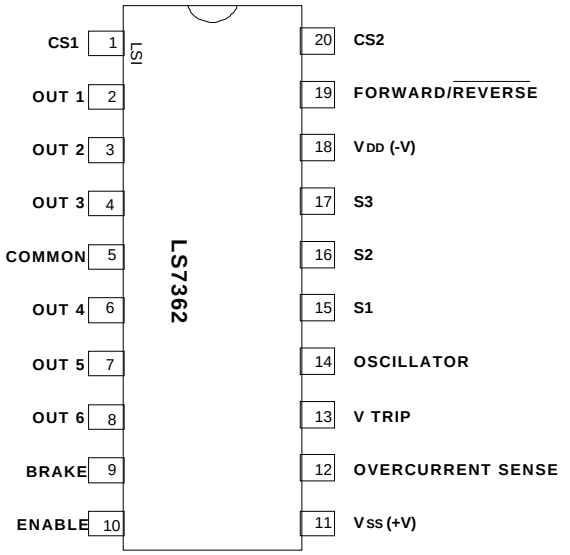
FEATURES:

- Speed Control by Pulse Width Modulation (PWM) of low-side drivers only.
- Open or closed loop motor speed control.
- +5 to +28 Volt operation (Vss - VDD).
- Externally selectable input to output code for 60°, 120°, 240°, or 300° electrical sensor spacing.
- Three or four phase operation.
- Analog Speed control.
- Forward/Reverse control.
- Output Enable control.
- Positive Static Braking.
- Overcurrent Sensing.
- Six outputs drive switching bridge directly.
- LS7362 (DIP), LS7362-S (SOIC)

CONNECTION DIAGRAM - TOP VIEW



DESCRIPTION:

The LS7362 is a monolithic, ion implanted MOS circuit designed to generate the signals necessary to control a three phase or four phase brushless DC motor. It is the basic building block of a brushless DC motor controller. The circuit responds to changes at the SENSE inputs, originating at the motor position sensors, to provide electronic commutation of the motor windings. Pulse width modulation (PWM) of low-side drivers for motor speed control is accomplished through either the ENABLE input or through the V TRIP input (Analog Speed control) in conjunction with the OSCILLATOR input. Overcurrent circuitry is provided to protect the windings, associated drivers and power supply. The LS7362 circuitry causes the external output drivers to switch off immediately upon sensing the overcurrent condition, and on again only when the overcurrent condition disappears and the positive edge of either the ENABLE input or the sawtooth OSCILLATOR occurs. This limits the overcurrent sense cycling to the chopping rate of the ENABLE input or the sawtooth OSCILLATOR. A positive braking feature is provided to effect rapid deceleration. The LS7362 is designed for driving Bipolar and Field Effect Transistors. Because only low-side drivers are pulse width modulated, the LS7362 is ideally suited in situations where the integrated circuit interfaces with level converters to drive high voltage brushless DC motors. By pulse width modulating the low-side drivers only, the switch losses in the level conversion circuitry for the high-side drivers is minimized. Figure 1 indicates how the level conversion is accomplished.

The COMMON, Pin 5, is tied to the positive supply rail and LS7362 Outputs 1, 2, and 3 are used to drive level converters Q101, Q102 and Q103 respectively. Only the motor top side drivers consisting of Q107, Q108 and Q109 which are connected to the motor power supply, V_M, will be subject to the high speed switching currents that flow through the motor. The level converters are turned on and off at the slower commutation rate.

INPUT/OUTPUT DESCRIPTION:

COMMUTATION SELECTS (Pins 1, 20)

These inputs are used to select the proper sequence of outputs based on the electrical separation of the motor position sensors. With both inputs low (logic zero), the sequence is adjusted for 60° electrical separation, with CS2 high and CS1 low 120° separation sequence is selected, with CS1 high and CS2 low 240° separation sequence is selected and with CS1 and CS2 high the 300° separation sequence is selected. Note that in all cases the external output drivers are disabled for invalid SENSE input codes. Internal pull down resistors are provided at Pins 1 and 20 causing a logic zero when these pins are left open.

FORWARD/$\overline{\text{REVERSE}}$ (Pin 19)
This pin acts to modify the input to output sequence such that when brought from high to low or low to high the direction of rotation will reverse. An internal pull up resistor is provided at Pin 19 causing a logic one when left open.

SENSE INPUTS (Pins 15, 16, 17)
These inputs provide control of the output commutation sequence as shown in Table III. S1, S2, S3 originate in the position sensors of the motor and must sequence in cycle code order. Hall switch "pull-up" resistors are provided at Pins 15, 16 and 17. The positive supply of the Hall devices should be common to the chip Vss.

BRAKE (Pin 9)
A high level applied to this input unconditionally turns off outputs 1, 2 and 3 and turns on outputs 4,5 and 6 (See Figure 1). Transistors Q101, Q102 and Q103 cut off causing Q107, Q108 and Q109 to cut off and transistors Q104, Q105 and Q106 turn on, shorting the windings together, The BRAKE has priority over all other inputs. An internal pull down resistor is provided at Pin 9 causing no braking when left open. (Center- tapped motor configuration requires a power supply disconnect transistor controlled by the BRAKE signal - See Figure 3.)

ENABLE (Pin 10)
A high level on this input permits the output to sequence as in Table III, while a low disables all external output drivers. An internal "pull up" resistor is provided at Pin 10, enabling when left open. Positive edges at this input will reset the overcurrent flip-flop.

OVERCURRENT SENSE (Pin 12)
This input provides the user a way of protecting the motor winding, drivers and power supply from an overload condition. The user provides a fractional ohm resistor between the negative supply and the common emitters of the NPN drivers. This point is connected to one end of a potentiometer (e.g. 100K ohms), the other end of which is connected to the positive supply. The wiper pickoff is adjusted so that all outputs are disabled for currents greater than the limit. The action of the input is to disable all external output drivers. When BRAKE exists, OVERCURRENT SENSE will be overridden. The overcurrent circuitry latches the overcurrent condition. The latch may be reset by the positive edge of either the sawtooth OSCILLATOR or the ENABLE input. When using the ENABLE input as a chopped input, the OSCILLATOR pin should be held at Vss. When the ENABLE input is held high, the OSCILLATOR must be used to reset the overcurrent latch.

V TRIP (Pin 13)
This pin is used in conjunction with the sawtooth oscillator provided on the circuit. When the voltage level applied to V TRIP is more negative than the waveform at the OSCILLATOR pin, the low-side drivers will be enabled. When V TRIP is more positive than the sawtooth OSCILLATOR waveform the low-side drivers are disabled.

The sawtooth waveform at the OSCILLATOR pin typically varies from .4 Vss to Vss-2 Volts (assuming V_{DD} is at ground potential). The purpose of the V TRIP input in conjunction with the OSCILLATOR is to provide variable speed adjustment for the motor by means of PWM of the low-side drivers.

OSCILLATOR (Pin 14)
A reisistor and capacitor connected to this pin (See Fig. 6) provide the timing components for a sawtooth OSCILLATOR. The signal generated is used in conjunction with V TRIP to provide PWM for variable speed applications and to reset the overcurrent condition.

OUTPUTS 1, 2, 3 (Pins 2, 3, 4)
These open drain outputs are enabled as shown in Table III and provide base current when the COMMON (Pin 5) is tied to Vss. These outputs provide commutation only for the high-side drivers. They are not pulse width modulated to control speed.

OUTPUT 4, 5, 6 (PINS 6, 7, 8)
These open drain outputs are enabled as in Table III and provide base current to NPN transistors when the COMMON is tied to Vss. They provide commutation and are pulse width modulated to provide speed control.

COMMON (Pin 5)
The COMMON is connected to Vss for driving low-side drivers and high-side level converters.

Vss (Pin 11) Supply voltage positive terminal.
V_{DD} (Pin 18) Supply voltage negative terminal.

TYPICAL CIRCUIT OPERATION:

Figure 1 indicates an application using bipolar power transistors. The oscillator is used for motor speed control as explained under VTRIP. Only low-side drive transistors are pulse width modulated during speed control. The outputs turn on in pairs (See Table III). For example, two separate paths are turned on when Q8 and Q4 are on. One path is from the positive supply through Q8, R1 and the base emitter junction of Q101. The second is from the positive supply through Q4, R14, the base emitter junction of Q105 and the fractional ohm resistor to ground. The current in the first path is determined by the power supply voltage, the impedance of Q8, the value of R1 and the voltage drop across the base-emitter junction of Q101 (0.7 Volts for a single transistor or 1.4 Volts for a Darlington Transistor). The current in the second path is determined by the power supply voltage, the impedance of Q4, the value of R14 and the voltage drop across the base-emitter junction of Q105. Table I provides the recommended value for R1; R2, R3, R13, R14, and R15 are the same value.
Figure 2 indicates an application where Power FETS are used. The nominal power supply for the LS7362 in this configuration is 15 Volts so that the low side N channel Power FET drivers will have 15 Volts of gate drive. Resistors R13, R14 and R15 serve to discharge the gate capacitance during FET turn-off. The high-side P-channel FET drivers use 15 Volt Zener diodes Z1, Z2 and Z3 to limit the gate drive. Resistors R8, R10 and R12 are the gate capacitance discharge resistors. Table II indicates the minimum value of R13 (=R14=R15) needed as a function of output drive voltage for the low-side drivers.

MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNIT
Storage Temperature	T_{STG}	-65 to +150	°C
Operating Temperature			
1. Plastic	T_A	-25 to +70	°C
2. Ceramic	T_A	-55 to +125	°C
Voltage (any pin to Vss)	V_{MAX}	-30 to +.5	Volts

DC ELECTRICAL CHARACTERISTICS:
(All Voltages Referenced to V_{DD})

	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{SS}	5	-	28	Volts
Supply Current					
(Excluding Outputs)	I_{DD}	-	4.5	6	mA
Input Specifications:					
BRAKE, ENABLE, CS1, CS2	R_{IN}	-	150	-	KΩ
S1, S2, S3, FORWARD/REVERSE					
Voltage (Logic "1")	V_{IH}	Vss-1.5	-	Vss	Volts
(Logic "0")	V_{IL}	0	-	Vss-4.0	Volts
OVERCURRENT SENSE (See Note)					
Voltage (Logic "1")	V_{IH}	(Vss/2)+.25	-	Vss	Volts
(Logic "0")	V_{IL}	0	-	(Vss/2)-.25	Volts
Oscillator:					
Frequency Range	Fosc	0	1/RC	100	KHz
External Resistor Range	Rosc	22	-	1000	KΩ

NOTE: Theoretical switching point of the OVERCURRENT SENSE input is one half of the power supply determined by an internal bias network in manufacturing. Tolerances cause the switching point to vary plus or minus .25 Volts. After manufacture, the switching point remains fixed within 10 mV over time and temperature. The input switching sensivity is a maximum of 50mV. There is no hysteresis on the OVERCURRENT SENSE input.

TABLE I
OUTPUT CURRENT LIMITING RESISTOR SELECTION TABLE

POWER SUPPLY (VOLTS)	OUTPUT CURRENT 20	15	10	7.5	5	2.5	mA
6	**	**	**	**	**	2.0	
9	**	**	**	.94	1.6	3.2	
12	.35	.53	.88	1.2	2.1	4.0	
15	.54	.76	1.2	1.7	2.6	5.3	Resistance
18	*	1.0	1.6	2.1	3.2	6.5	(KΩ)
21	*	*	1.9	2.5	3.8	7.7	
24	*	*	2.2	2.9	4.4	9.0	
28	*	*	*	3.5	5.3	10.3	

*causes excessive power dissipation
**exceeds max current possible for this voltage

TABLE II
For Power Supply 5-28 Volts

R13 (K ohms)	Output Voltage
10	Vss -0.5
5.1	Vss -1.0
2.7	Vss -2.0

TABLE III
OUTPUT COMMUTATION SEQUENCE
THREE PHASE OPERATION

SEQUENCE SELECT	CS1 CS2 = 0 0	CS1 CS2 = 0 1	CS1 CS2 = 1 0	CS1 CS2 = 1 1	FORWARD/REVERSE=1				FORWARD/REVERSE=0			
ELECTRICAL SEPARATION	(-60°-)	(-120°-)	(-240°-)	(-300°-)	OUTPUTS	DRIVERS			OUTPUTS	DRIVERS		
SENSE INPUTS	S1 S2 S3	S1 S2 S3	S1 S2 S3	S1 S2 S3	ENABLED	A	B	C	ENABLED	A	B	C
	0 0 0	0 0 1	0 1 0	0 1 1	O1, O5	+	-	Off	O2, O4	-	+	Off
	1 0 0	1 0 1	1 1 0	1 1 1	O3, O5	Off	-	+	O2, O6	Off	+	-
	1 1 0	1 0 0	1 0 0	1 1 0	O3, O4	-	Off	+	O1, O6	+	Off	-
	1 1 1	1 1 0	1 0 1	1 0 0	O2, O4	-	+	Off	O1, O5	+	-	Off
	0 1 1	0 1 0	0 0 1	0 0 0	O2, O6	Off	+	-	O3, O5	Off	-	+
	0 0 1	0 1 1	0 1 1	0 0 1	O1, O6	+	Off	-	O3, O4	-	Off	+
	0 1 0	0 0 0	0 0 0	0 1 0	ALL DISABLED				ALL DISABLED			
	1 0 1	1 1 1	1 1 1	1 0 1	ALL DISABLED				ALL DISABLED			

The OVERCURRENT input (BRAKE low) enables external output drivers in normal sequence when more negative than Vss/2 and disables all external output drivers when more positive than Vss/2. The OVERCURRENT is sensed continuously, and sets a flip flop which is reset by the rising edge of the ENABLE input or the sawtooth OSCILLATOR. (See description under OVERCURRENT SENSE.)

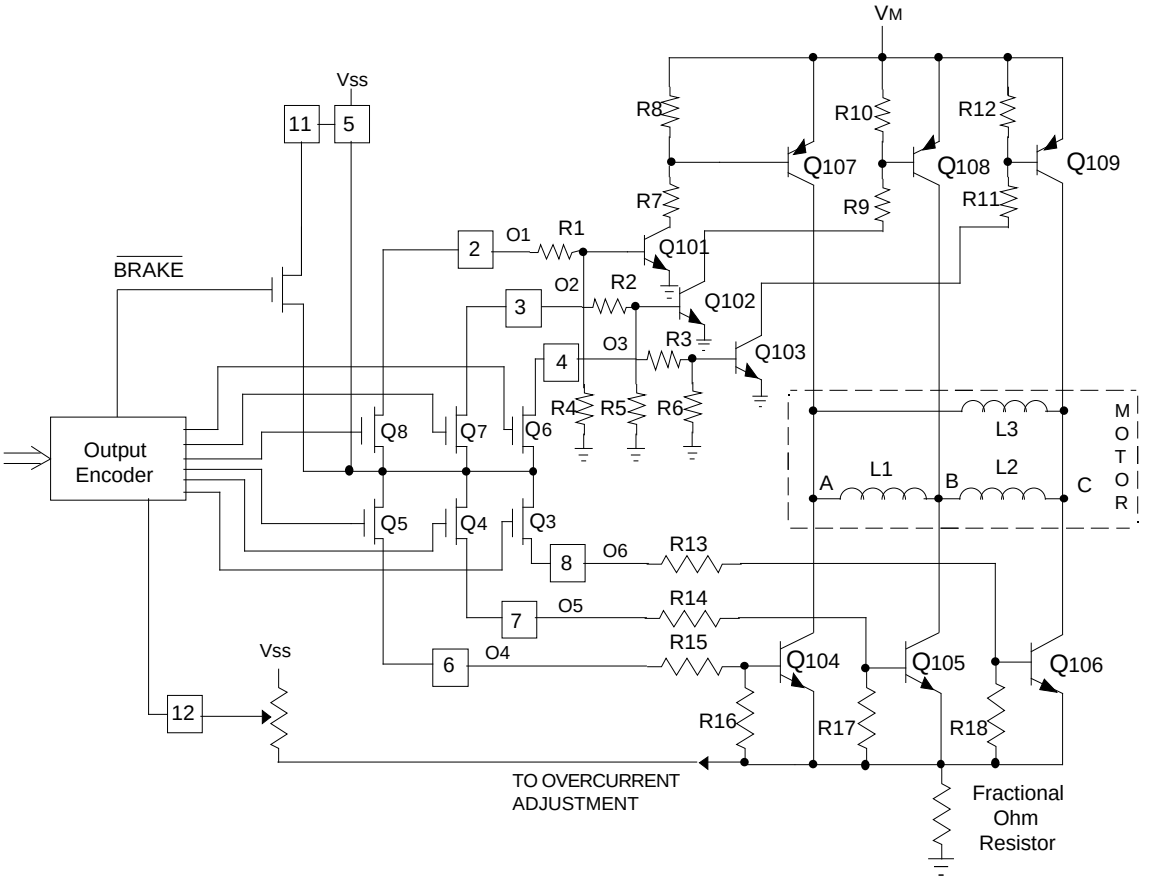


FIGURE 1. BIPOLAR THREE PHASE OUTPUT DRIVER CIRCUITRY

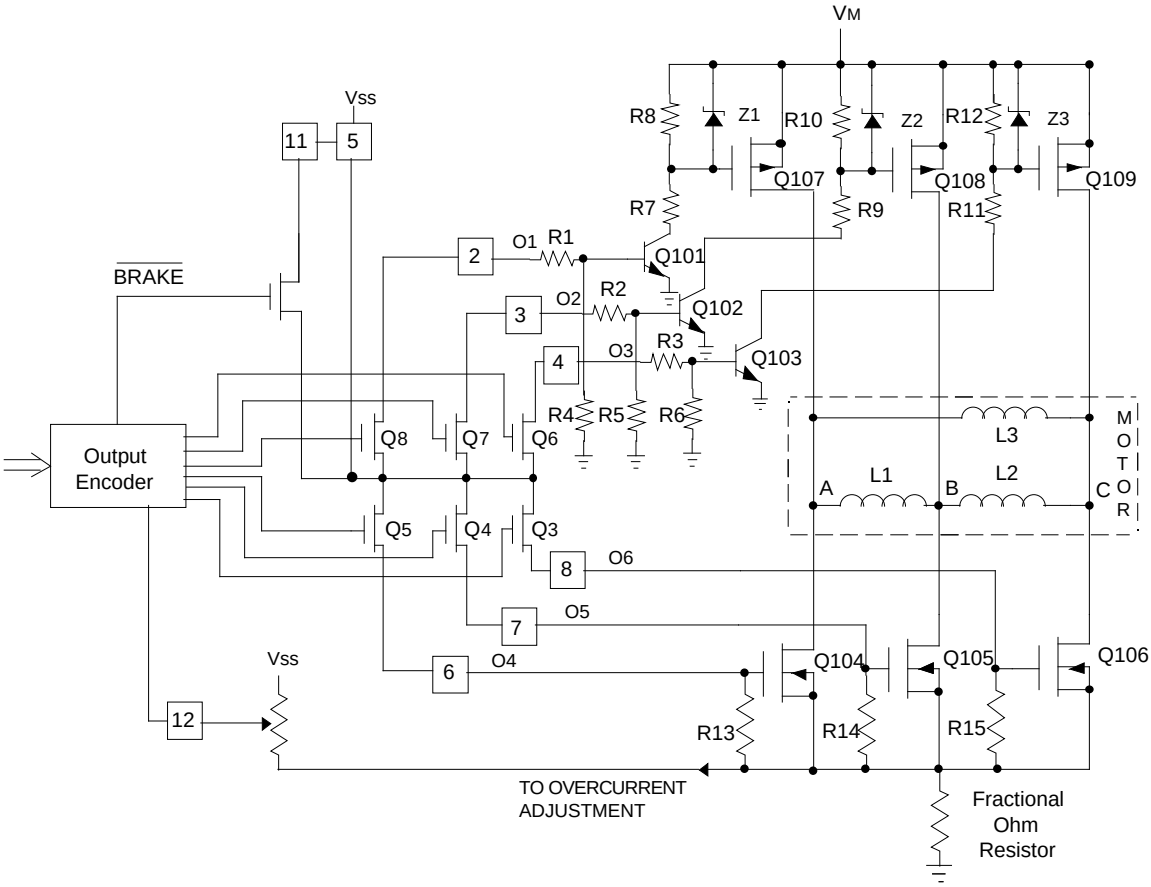


FIGURE 2. POWER FET THREE PHASE OUTPUT DRIVER CIRCUITRY

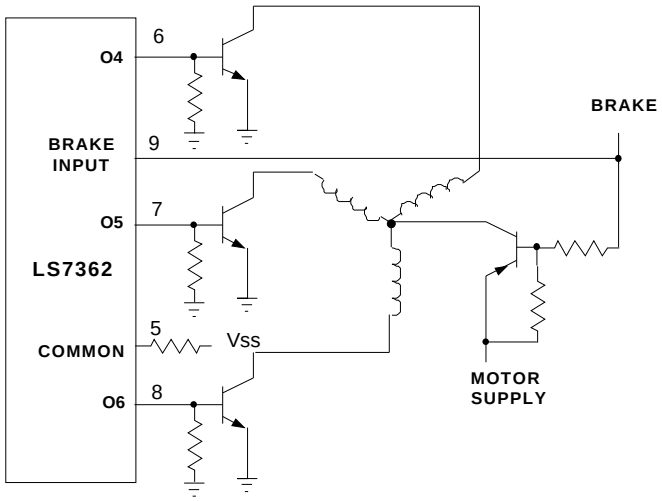


FIGURE 3. SINGLE-ENDED DRIVER CIRCUIT

This configuration requires only one base current limiting resistor connected from the COMMON pin to Vss.

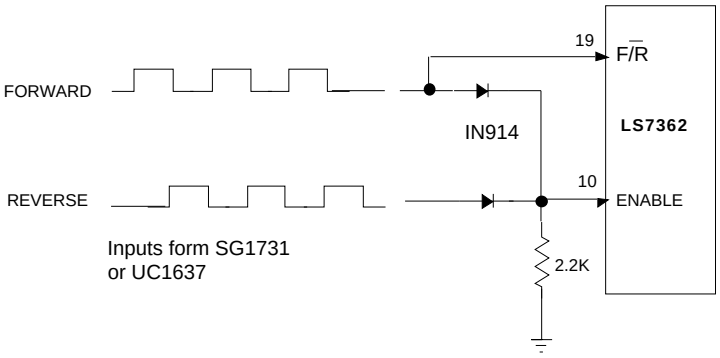


FIGURE 4. PRECISION CONTROL BRUSHLESS DC MOTOR DRIVE

For controlled acceleration and deceleration of motors in the forward or reverse directions, a motor control pulse width modulator circuit such as the SG1731 or UC1637 can be interfaced with the LS7362.
The logical OR gate made up of the resistor-diode network permits the LS7362 to be enabled when either the forward or reverse input is high. By applying the forward input directly to Pin 19, the motor can only operate in the forward direction when the forward input is high and only in the reverse direction when the reverse input is high. Motor direction is determined by relative pulse widths of the forward and reverse inputs while acceleration or deceleration is determined by variations of these widths.

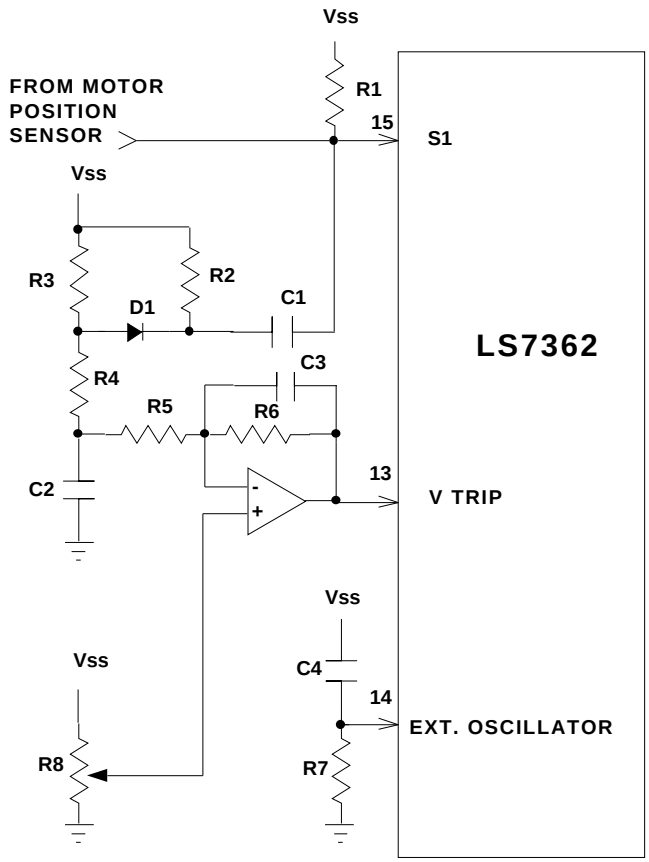


FIGURE 5 CLOSED-LOOP SPEED CONTROLLER

A closed loop system can be configured by differentiating one of the motor position sense inputs and integrating only the negative pulses to form a DC voltage that is applied to the inverting input of an op-amp. The non-inverting input voltage is adjusted with a potentiometer until the resultant voltage at V TRIP causes the motor to run at desired speed. The R2-C1 differentiator, the R3-D1 negative pulse transmitter and the R4-C2 integrator form a frequency to voltage converter. An increase in motor speed above the desired speed causes V TRIP to increase which lowers the duty cycle modulation of the oscillator and the resultant motor speed. A decrease in speed lowers V TRIP and raises the duty cycle modulation and the resultant motor speed. For proper operation, both R5 and R6 should be greater than R4, and R4 in turn should be greater than both R2 and R3. Also the R4-C2 time constant should be greater than the R2-C1 time constant. C3 may be added across R6 for additional V TRIP smoothing.

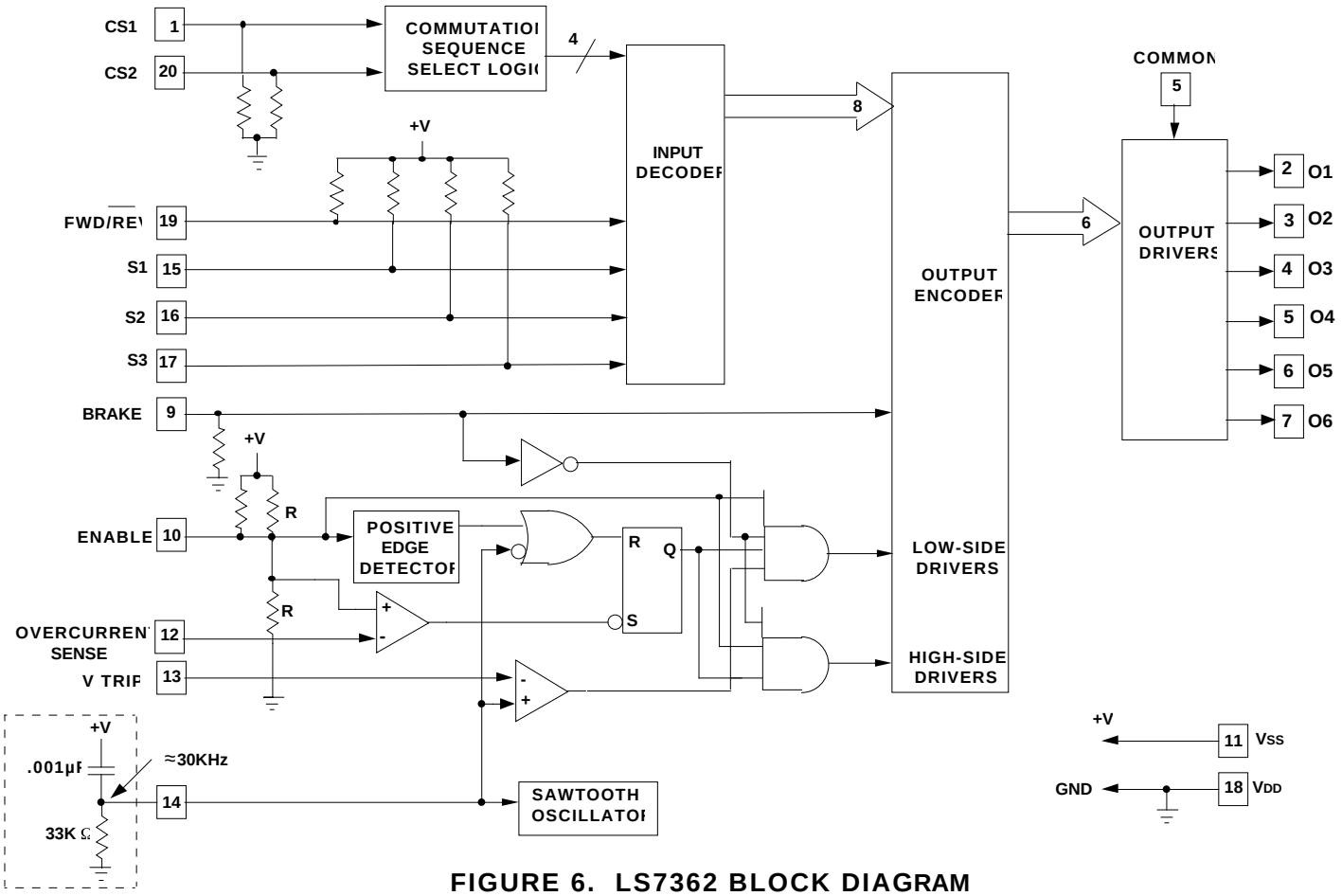


FIGURE 6. LS7362 BLOCK DIAGRAM