LSI/CSI
Manufacturers of Custom and Standard LSI Circuits

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LS7040

Revised July 1989

DUAL 3 DECADE UP/DOWN COUNTER

FEATURES:

- DC to 350 KHz Count Frequency at +5V Operation
- Fully Synchronous Operation
- Cascadable
- Inputs CMOS, TTL, and DTL Compatible at +5V Operation
- Separate Low Current Drain Power Supply for Counter Stages Permits Battery Stand-by Operation
- Reset
- Count Enable
- Parallel BCD Output Data
- Power-on-Reset
- Count Input Applied to a Regenerative Circuit which Permits Infinite Rise and Fall Times
- Selectable as 6 Decade or Dual 3 Decade Up or Down Counter
- CMOS Type Noise Immunity on all Inputs
- Output Latches
- Single Power Supply Operation +4.75VDC to +15VDC

DESCRIPTION:

The LS7040 is a monolithic ion implanted MOS synchronous Dual 3 Decade or 6 Decade Up/Down Counter including latches and parallel BCD data outputs.

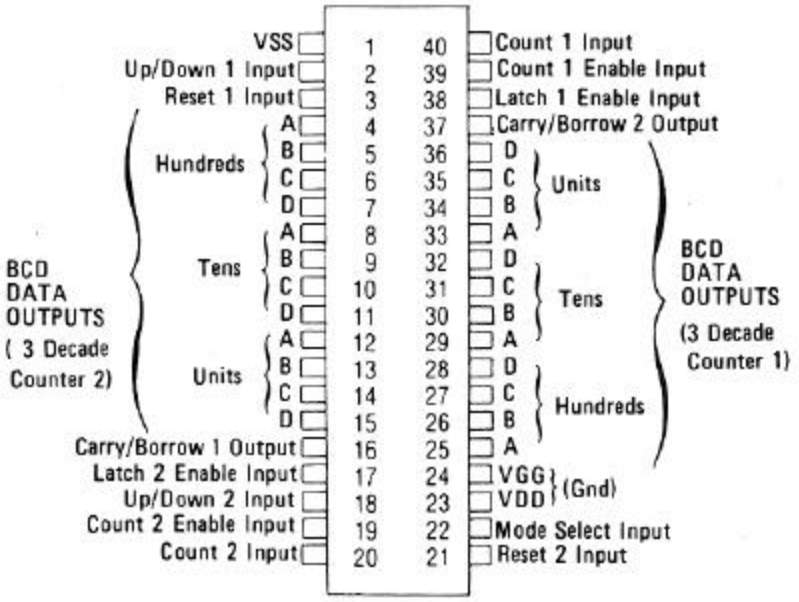
DESCRIPTION OF OPERATION:

UP/DOWN Circuit can be operated as a 6 decade Up or Down counter, a dual 3 decade Up or Down counter, or in a mode where one 3 decade counter counts up and the other counts down. A high input causes counter to operate in the Up mode. A low input (or N/C) causes the counter to operate in the Down mode.

COUNT Counter will operate at speeds up to 350kHz and advances on the negative edge of the input count pulse. When using as a synchronous 6 decade counter, Count 1 and Count 2 must be tied together and must have fast rise and fall times, i.e. 50 μsec max. When using as an asynchronous counter, the input count pulse is applied to the Count 1 Input and the Carry/Borrow 1 output is applied to the Count 2 Input. In this mode, the input count pulse can have an infinite rise and fall time. Refer to Figures 2 through 4 for synchronous and asynchronous counter operation.

RESET A high input will hold all counter stages at zero. When using as a 6 decade counter, Reset 1 and Reset 2 must be tied together.

CONNECTION DIAGRAM: TOP VIEW
STANDARD 40 PIN PLASTIC DIP



TOP VIEW

COUNT ENABLE A high input will permit counting. A low input will inhibit counting and the counter will remain at its last count. When using as a 6 decade counter, Count 1 Enable and Count 2 Enable must be tied together. See Figures 2 through 4.

LATCH ENABLE A high input will cause information present in the counter to be transmitted through the latch. A low input prevents updating of the latches as the counter advances. When using as a 6 decade counter, Latch 1 Enable and Latch 2 Enable must be tied together.

MODE SELECT When input is low (or N/C), the counter becomes a dual 3 decade counter. In this mode of operation the counter can be hooked up as an asynchronous 6 decade counter. A high input causes the counter to operate as a synchronous 6 decade counter.

BCD DATA All 24 BCD data bits stored in the latches are brought out in parallel.

CARRY/BORROW As a Dual 3 Decade Up Counter, Carry signals are positive outputs lasting for one clock period that occur when a count of 999 is reached. Each output is capable of driving another 7040 counter directly. When used as a synchronous 6 decade Up Counter, Carry 2 will be the output Carry and will occur when a count of 999999 is reached while Carry 1 is internally routed into decade 4. As a Dual 3 Decade Down Counter, Borrow Outputs occur when a count of 000 is reached. As a synchronous 6 Decade Down Counter, Borrow 2 will occur when a count of 000000 is reached. When cascading synchronous 6 Decade Counters, Carry/Borrow 2 of the first counter is applied to the Count 1 Enable and Count 2 Enable of the second counter . In this case the count inputs of both counters must be tied together. This arrangement enables fully synchronous operation.

When cascading asynchronous counters, Carry/Borrow 2 of the first counter is applied to Count 1 of the second counter. To Enable counting, Count 1 Enable and Count 2 Enable must be high (VSS).

POWER SUPPLIES The circuit will operate over the range of 4.75V to +15V. VGG is the supply for all the peripheral circuitry VDD is the supply for the low current drain counter chain. This is done to facilitate battery stand-by for VDD during a power supply outage condition. (See Figures 5 and 6). During this condition the circuit will continue to count and generate output carry signals. The BCD outputs will not be available and the latch will be inoperative.

POWER-ON-RESET A Power-On-Reset circuit enables the counter to initialize at a count of 000000 when power is first applied.

NOTE: The following inputs have internal pull down resistors to VDD with maximum sink current of 20 μA at VSS input.

Up/Down 1
Up/Down 2
Mode Select

TECHNICAL DATA

Input Specification-With VSS=+15V and VDD=VGG=0V inputs will be High Threshold Logic and CMOS compatible. With VSS=+5V inputs will be TTL, DTL, and CMOS compatible. (TTL and DTL inputs require +3.5 volts logic 1 input).

Outputs - Will be CMOS compatible over entire range of power supply voltage limits.

Logic - Positive true.

Package - 40 pin Dual-In-Line.

MAXIMUM RATINGS:

Parameter	Symbol	Value	Units
Storage Temperature	Tstg	-65 to +150	°C
Operating Temperature	Ta	-25 to +70	°C
Voltage (any pin to VSS)	Vmax	-30 to +.5	V

DC ELECTRICAL CHARACTERISTICS

(VDD = *VGG* = 0V, VSS = +4.75V to +15V,-25°C Ta ±70C°
Unless otherwise specified.

Parameter	Symbol	Min.	Max.	Units
Quiescent Supply Current (VSS = +5V)	Idd		2.5	mA
	Igg		4.5	mA
Quiescent Supply Current (VSS = +9V)	Idd		3.0	mA
	Igg		7.0	mA
Quiescent Supply Current (VSS = +15V)	Idd		4.0	mA
	Igg		11.0	mA
Input Capacitance All Inputs	Cin		10	pf
Noise Immunity All Inputs	Vnl	30%(VSS-VDD)		Volts
	Vnh	30%(VSS-VDD)		Volts
Output Levels All Outputs	Vol		+0.5	Volts
	Voh	VSS-1		Volts

AC ELECTRICAL CHARACTERISTICS

(VDD = *VGG* = 0V, VSS = +4.75V to +15V,-25°C Ta ±70C°
Unless otherwise specified.

Parameter	Symbol	Min.	Max.	Units
Count Input Frequency (For Data Outputs) VSS = +5V, 3 Decade	Fc	DC	350	kHz
VSS = +5V, Synchronous 6 Decade	Fc	DC	250	kHz
VSS = +15V, 3 Decade	Fc	DC	250	kHz
VSS= +15V,Synchronous 6 Decade	Fc	DC	175	kHz
Count Input Pulse width (negative Pulse) VSS = +5V	Tcpw	1.5		μs
VSS = +15V	Tcpw	2.5		μs
Count Input Rise and Fall Fall Time				
Asynchronous Counting			No Limit	
Synchronous Counting			50	μs

AC ELECTRICAL CHARACTERISTICS (Cont'd)

Parameter	Symbol	Min.	Max.	Units
Reset Pulse Width	Trpw	4.0		μs
Count Enable Set Up Time	Tces*	2.0		μs
Count Enable Hold Time	Tceh*	2.5		μs
Count Input to Latch Enable Set Up Time	Tcls	4.0		μs
Latch Enable Pulse Width	Tlpw	2.0		μs
Up/Down Set Up Time	Tuds*	2.0		μs
Up/Down Hold Time (See Note 1)	Tudhl*	7.0		μs
	Tudht**	2.5		μs
Propagation Delay (CL = 15 pF)				
Data Output	Tdd*		4.5	μs
Carry Output	Tcd*		5.5	μs

* With respect to count input leading negative edge.

** With respect to count input trailing positive edge.

Note 1: Tudht may be used instead of Tudhl at high frequencies where the Count Input negative pulse width is less than 4.5 μsec. If the pulse width is greater than 4.5 μsec., Tudhl must be used.

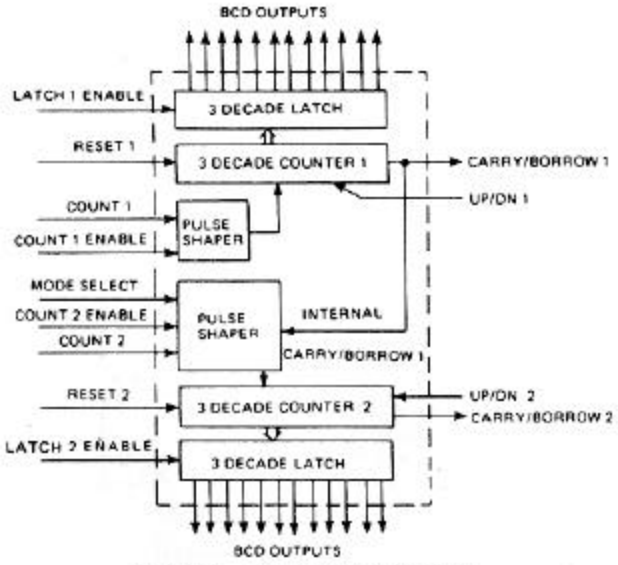


FIGURE 1 – LS7040 BLOCK DIAGRAM

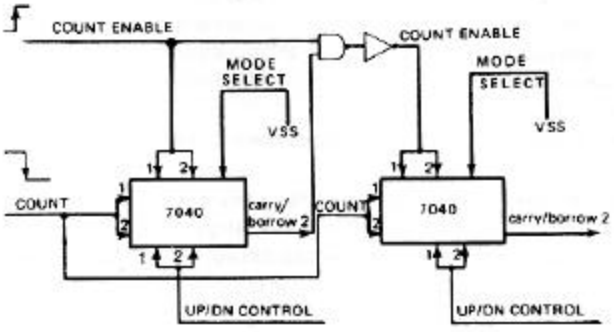


FIGURE 2 – SYNCHRONOUS 12 DECADE COUNTER

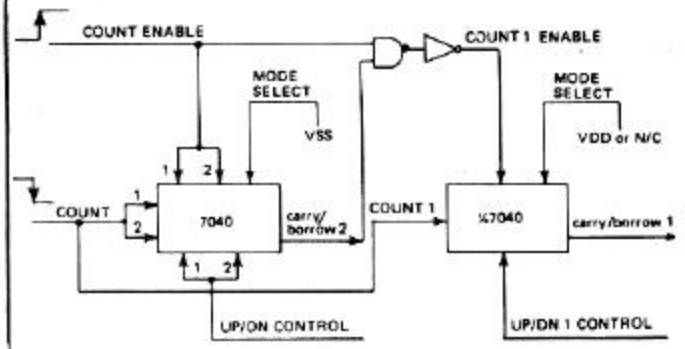


FIGURE 3 – SYNCHRONOUS 9 DECADE COUNTER

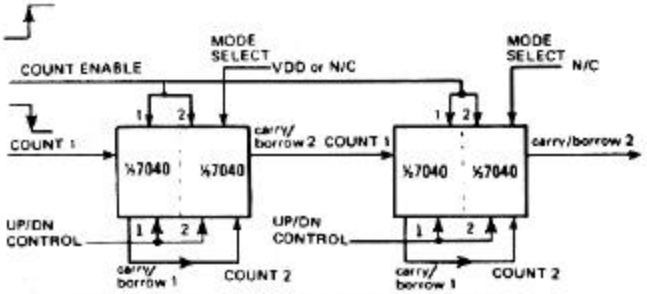
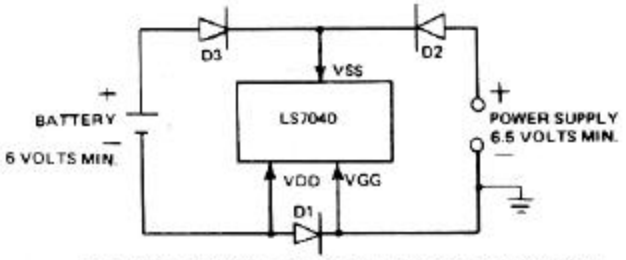


FIGURE 4 – ASYNCHRONOUS 12 DECADE COUNTER

BATTERY STAND-BY SCHEMATICS



Positive Supply System The battery voltage is lower than the supply voltage and is used only in the Power Outage Condition for counting. When the power supply is shut off, the battery supplies current only through VDD. Diode D1 is used to isolate VDD and VGG. Diode D2 is used to prevent VSS from going to ground potential when the power supply shuts off. Diode D3 is used to isolate the battery and the power supply.

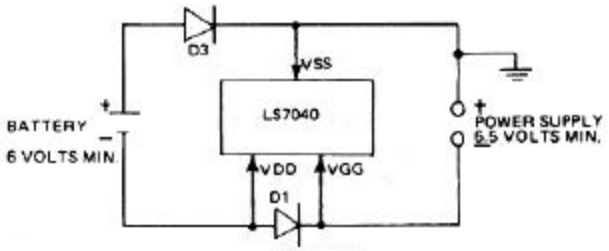


FIGURE 6

Negative Supply System Diode D2 is not needed since VGG going to ground potential will not affect standby operation.

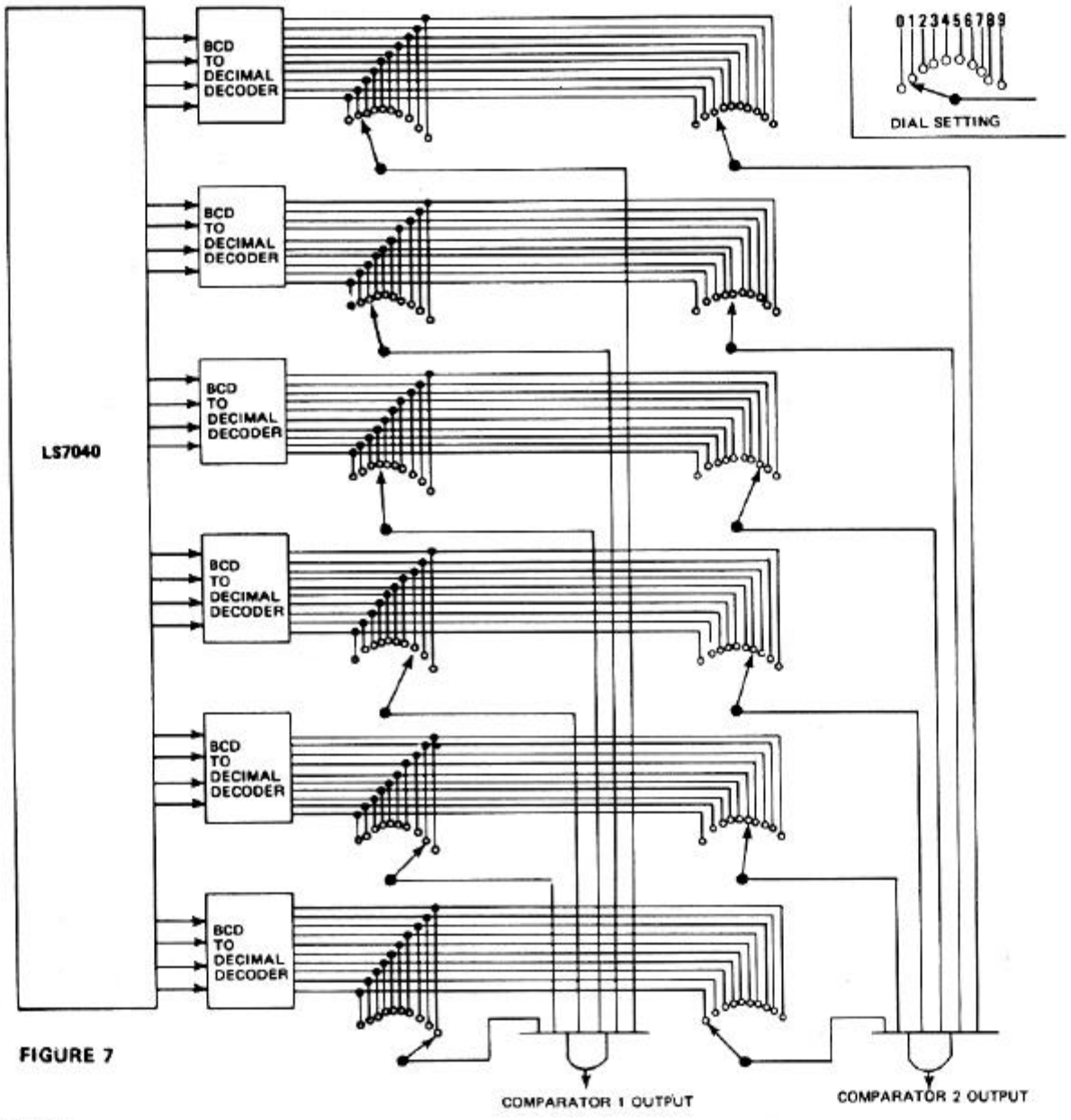


FIGURE 7

APPLICATION NOTE:

The unique feature of the LS7040, and its main advantage over multiplexed counters, is its parallel BCD outputs. These outputs can be applied to as many external preset comparators as desired with a minimum of hardware. Figure 7 illustrates the circuitry for two 6 digit comparators. A BCD to Decimal decoder and a 10 position switch is used for each of the decade outputs. The arms of the 6 switches are combined in an And gate to provide the comparison output. The desired decimal number is selected and the And gate produces a Logic 1 output when the LS7040 reaches that number. For each additional comparator, six 10 position switches and one And gate are added. There is no limit to the number of comparators that can be used with one LS7040 and 6 BCD to decimal decoders. Counter outputs can be displayed by applying the BCD outputs to a 7 segment decoder to drive LED displays.

Because of the cascadability of the LS7040, a 12 digit comparator scheme would use 2 LS7040's and 12 BCD to decade decoders. This scheme can be extended to as many digits as desired.

Figure 7 depicts an output occuring at comparator 1 when the LS7040 reaches a count of 123789. Comparator 2 will produce an output at a count of 247650

An additional advantage of the LS7040 over multiplexed counter outputs occurs when analog circuits and counter circuits are being used together. The demultiplexing signals and associated hardware that are used by a multiplex counter can cause noise to interfere with analog signals. The use of the LS7040 in an analog application will negate the possibility of any noise generation.