SATURN-II

L9002DX2

***CD/SS™* Wireless packet and voice communication processor**

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1. GENERAL DESCRIPTION

The L9002DX2 is a second generation digital wireless communication chip using the Lanwave Code Division Spread Spectrum (CD/SS™) DSP architecture. It is backward compatible with prior Lanwave SATURN devices, with a improved internal DSP engine to support higher coding density using a proprietary fractional chip rate scheme, in additional to several functional enhancements for diversity control and packet data protocols.

L9002DX2 fractional chip mode employs the logarithmic sub band phase encoding technique, a variation of the VPSK scheme (Very Small Phase Shift Keying). Using this scheme a fractional one-half and one-third chip rate CD/SS™ codes can be employed to reduce IF bandwidth requirement on the RF circuit while keeping at least 10dB processing gain to meeting FCC Part15.247(e) requirements.

The L9002DX2 is a superset of the L9002VX2 and remains backward compatible to all SATURN-classic series devices. In addition, a diversity control register (DCR) is implemented to assist in dual antenna selection using a Fuzzy Logic technique. This register also provide an orthogonal hop set generator for hybrid CD/SS frequency hopping systems in the 2.4GHz RF band. A burst transfer mode is added for carrying an additional 12-bytes of data in each acquistion burst frames (abf), expanding the packet data rate by 500%. This feature is used for low bit rate signalling at sub-sensitivity RF levels using time diversity ability built into the packet frames.

Application of the L9002DX2 ranges from very low cost digital cordless telephones using 500KHz IF bandwidth, to the very high performance wireless PABX and wireless local loop systems in any open frequency bands. The added coding efficiency in baseband DSP allows for more room to reduce cost either in a simplified RF filter circuit, or by replacing the ADPCM chip with software direct voice sampling (PCM codec). In addition, sub band phase encoding will allow one-quarter to one-fifth chip rate CD/SS codes for digital narrow band and hybrid frequency hopping phones to be implemented in a uniform architecture with the basic CD/SS digital spread spectrum model in the same family, simplifying engineering and product change costs. Other system enhancements of the L9002DX2 lies in the continued improvement of the software to be made available by customers in-house development and from future Lanwave products.

Implemented in a low power 3V CMOS process technology, the L9002DX2 is compatible electrically, functionally and in identical pin out to all SATURN family of products. A complete reference design is available for telephone manufacturers for quick turn development.

2. FEATURES

- Single 2.7 to 3.6 volt power supply
- Master clock rate: 20MHz (DX2-20), 33MHz (DX2-33) and 40MHz (DX2-40) with external crystal
- Typical power consumption of 30 mA active mode at 33MHz; power down to 0.5 mA
- Advanced CD/SS™, 1-bit CDMA, digital signal processing architecture with VPSK encoding

- Integrated dual antenna design with support for space and frequency diversity. Fuzzy logic based space and frequency Diversity Control Register (DCR).
- Preamble search and locking mechanism allowing for time diversity design in sub-sensitivity RF channels. Burst transfer mode increased data bandwidth by 500% to 15bytes per packet.
- Compliant with FCC Part 15.247(e) in 2.4GHz & 900MHz operations using full rate to 1/3 rate codes. Supporting narrow band digital encoding and hybrid frequency hopping with less than 1/3 rate codes.
- Information encoded with 8x32-bit user selectable modulation code, 22-bit ID, 8x11 bit encryption seed for maximum information security
- Advanced Noise Reduction for voice transmission
- 24-bit command field per frame with Forward Error Protection (FEP)
- Direct interface to ADPCM codec and 4-bit / 8-bit microcontrollers
- Integrated power management
- 32 General Purpose I/O expansion pins
- Programmable CPU Clock Generation
- Programmable General Purpose Timer
- Low power, STATIC CMOS circuit design
- 100-pin, 0.65mm pitch, PQFP package for easy assembly
- 100-pin, 0.50mm pitch, low profile TQFP for tight packaging

3. SUMMARY OF NEW FUNCTIONS

The following new functions described from section 3.1 to 3.3 are implemented in the SATURN-II DX family only. Sections 3.4 to 3.5 are implemented in both the SATURN-II VX and DX2 families.

3.1 Fractional Chip Rate mode

Fractional Chip Rate employs logarithmic sub band VPSK technique to CD/SS encoding, reducting IF frequency bandwidth to one-half and one-third while keeping over +10dB processing gain for FCC Part 15.247(e) requirements, and one-quarter to one-sixth for narrowly spreaded bandwidth systems.

To derive higher signal resolution from the 1-bit ADC quantizer in the SATURN architecture, phase quantization is used in the sub band frequencies to improve signal accuracy. The maximum phase resolution allowed in the L9002DX2 DSP engine is 6-levels per chip, or 12-phase symbols per cycle, making for a maximum coding density of 1.778 chips per bit compared to the current 10.667 chips per bit. Practical usage is recommended to higher than 1/3 rate encoding for FCC compliant systems.

SATURN-classic family: 32 (chips/symbol) / 3 (bits/symbol) = 10.667 chips per bit.

SATURN-II DX family: 32 /3 (chips per bit) * (1/6) = 1.778 chips per bit.

This is summarized in the following table:

Fractional Code Rate (Lanwave Semantics)	**VPSK Phase Resolution** (symbol / cycle)	**8-level CD/SS™** average chips per bit	**IF Frequency bandwidth** (at 19.2MHz Master Clock)	**Channel spacing** GFSK /w Bt=0.5	**Channel efficiency** (1) (Hz per bit per second)
Full Rate (PN_X)	2	**10.667**	682 Khz	2.048 Mhz	25.5
Half Rate (PN_H)	4	**5.33**	341 Khz	1.024 Mhz	12.8
One Third Rate (PN_T)	6	**3.56**	228 Khz	683 Khz	8.5
One Fourth Rate (PN_U)	8	**2.67**	171 Khz	512 Khz	6.4
One Fifth Rate (PN_V)	10	**2.13**	137 Khz	410 Khz	5.1
One Sixth Rate (PN_W)	12	**1.78** (2)	113 Khz	341 Khz	4.3

(1) Calculated based on full duplex data rate on standard SATURN-II TDD frame architecture, without subframe error correction word bandwidth(6bits per subframe), before CD/SS despreading gain.

(2) Fractional rate CD/SS codes eventually approach TDMA ratio of 1chip per bit, with a gradual change in error correction ability (jamming margin, or processing gain.)

A higher coding density improves IF bandwidth utilization at the tradeoff of jamming margin. RF sensitivity, however, improves upto 5dB. To satisfy FCC Part 15.247(e) requirement the minimum fractional rate is one-third. At this code rate the IF chip band width is 228KHz. If the FCC measurement tolerance is included (which is 2dB) the absolute minimum is one-fifth. At fractional rates, however, the RF bandwidth is less than 500KHz under nominal SATURN Mclk operation and the technique is applicable to hybrid hopping or narrow band digital systems only.

Using the fractional chip rate requires special CD/SS codes and re-programming of the DX2 internal DSP registers. These information are obtainable directly from Lanwave Technology, Inc. Since the

RF signal is phase quantized at a higher resolution there is restriction on phase noise and jitter specifications using the L9002DX2 under the fractional chip rate mode. These requirements are described in the Lanwave Technical Note AN-10.

CD/SS code compression achieves the same IF bandwidth reduction as 32kbps, 24kbps and 16kbps ADPCM compression. By using a doubled master clock (between 32Mhz to 38.4MHz) and fractional chip rate mode, the uncompressed PCM samples at 8Kx8bit can be sent through the same IF frequency bandwidth, or slightly less than the VX2 bandwidth.

For detail please contact Lanwave Technical Support (email: techsupport@lanwave.com).

3.2 Diversity Control Register (DCR)

These new registers in the L9002DX2 implement a dual antenna switching gate and an orthogonal hybrid hop set generator. Details of the antenna switch gates and its application is described in Lanwave Technical Note AN-9.

The internal antenna switching decision circuit is based on a frame based SNR evaluation. The diversity optimization algorithms based on this strategy is detailed in Lanwave Technical Note AN-13. The logic circuit implemented in the L9002DX2 is designed to assist this software algorithm but can be bypassed in the control software for other diversity strategies.

The internal hop set generator is aimed at assisting frequency hopping and rendevous algorithms implementable in a low cost MCU. The hop set generator is designed to be used in conjunction with the CD/SS spread spectrum engine to meet FCC hybrid hopping requirements and is not recommended for non-hybrid applications. Detail of this register and usage is described in Lanwave Technical Note AN-15.

3.3 Burst Packet Transfer mode

Burst Packet Transfer mode expands the data transfer rate allowed in the current SATURN-classic family by 500% to 15-bytes per acquistion (abf) packet. The abf packet currently allows time diversity implementation of 3-byte data transfer in the ID&ST field subject to a 2-stage Markov chain control of preamble acquisition. This preamble search and locking mechanism allows a limited data transfer capability in a highly noisy environment by packet retransmission (time diversity) and signal detection in an exceptionally high error rate. Typically this mechanism would provide a non-isochronous communication channel at 8 to 10dB below the receivers RF sensitivity limit in a FSK modulation scheme. Detail application of this mechanism for data and protocol communication below the sensitivity edge is explained in Lanwave Technical Note AN-16 obtainable from Lanwave Technical Support.

Data communication of an extra 12-bytes of full duplex data comes from the data stored in the transmit FIFO before abf transmission, and the received 12-byte of packet data is deposited without error correction into the receive FIFO after a valid abf preamble has been declared received. The SATURN-II DX family preserves backward compatibility with prior SATURN-classic by shortening the quad IDx2 checking fields to ID+3-bytes of transmit data in each abf sub frames. The TDD link between a SATURN L9002DX2 with a prior generation SATURN can hencefore be preserved using software. Future TDD amongst DX2 devices can take advantage of the new packet bandwidth in the protocol software upon announcing and sensing the capability of its partners. Gradually and over time, this new DX2 frame structure can over take the old SATURN-classic framing architecture as the new software data transfer scheme.

The following functions are present in both the SATURN-II VX family and the DX family:

3.4 Slave Clock Correction mode

Slave Clock Correction Mode facilitates chip rate scaling.

Data flow in a SATURN Master-Slave communication link inherently follows the timing of the on board 19.2MHz master crystal, which is inevitably different to the slave side crystal and could change over time and temperature. The slave ADPCM coding and decoding rate (8KHz) follows the timing of the COD_SYNC signal from the base band SATURN processor. To enable identical voice sampling rate the slave COD_SYNC is designed to phase locked to the master SATURN timing. This internal digital phase locked loop has been extended 25% in locking range in the L9002VX2 and L9002DX2, thereby allowing a Mclk range down to 14.4MHz. This feature allow system designers to use a lower chipping rate (down to 1.02Mcps) to derive cost and range improvements in a consumer electronic system. (The Nyquist voice channel reduction is proportional. A 14.4MHz Mclk will allow a 0 - 3KHz voice path bandwidth.)

Asserting the Slave Clock Correction Mode can be done through connecting pin 26 of the L9002VX2 or L9002DX2 to HIGH (Vcc) before a hardware Reset. This pin is currently a No Connection (NC) pin in the prior SATURN devices thereby preserving backward compatiblity.

For detail system design see Lanwave Technical Note AN-2.

3.5 Command Field Eavesdropping mode

This feature enables command broadcasting from an active Master-Slave Time Division Duplex (TDD) link during conversation.

Any listening L9002VX2 and L9002DX2 within the radio radius in the same frequency, can pick up (evardrop) on the active Master's Command field (24-bit UST) in TDD with its active Slave if its 22-bit UID is known. This is performed by programming the listening Slaves with a "Mirror_ID" in the Receive_Only mode. The Mirror_ID is a 24-bit binary number related by a binary function from the 22-bit master group ID (UID) and the 8-bit encryption seed vector. This function implemented in the existing SATURN family has been simplified to enable real time derivation in a 4-bit MCU processor in the new SATURN-II without compromising security. For details see Lanwave Technical Note AN-3.

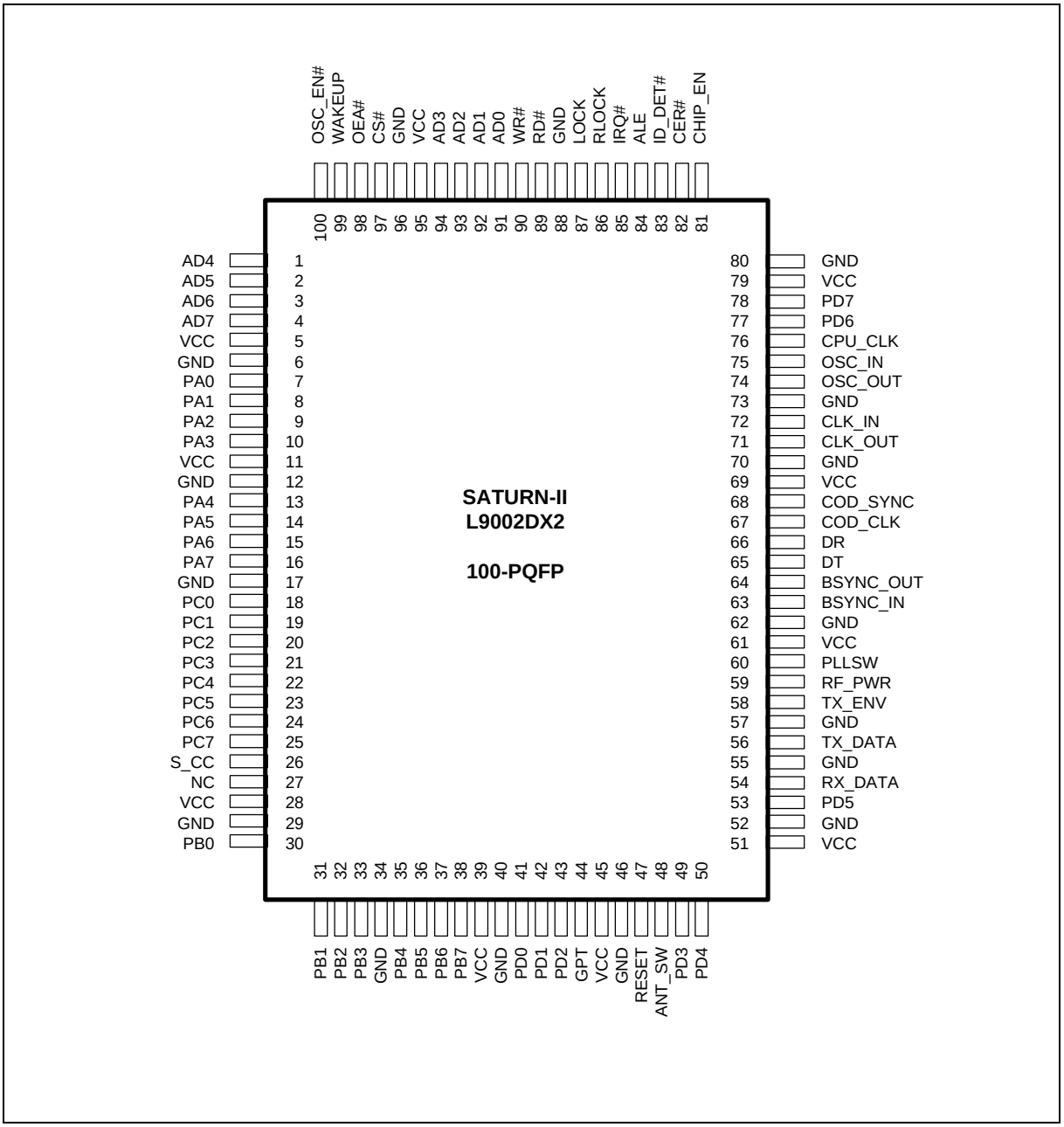
Active evasdropping allows TDD link break-in using simple algorithms. Link break-in is used to implementing SOHO PABX features such as Ring-on-Intercom, or Caller-ID notification to an active conversation pair. It also allows more complex software be used for multiple base, multiple domain synchronization.

To implement the new elliptic function the entire 24-bit UID field has to be programmed completely and beginning with "10" follow by.. 22-bit User Selectable ID. Backward compatibility is preserved with the old SATURN family members since the first two bits were hard wired to "10".

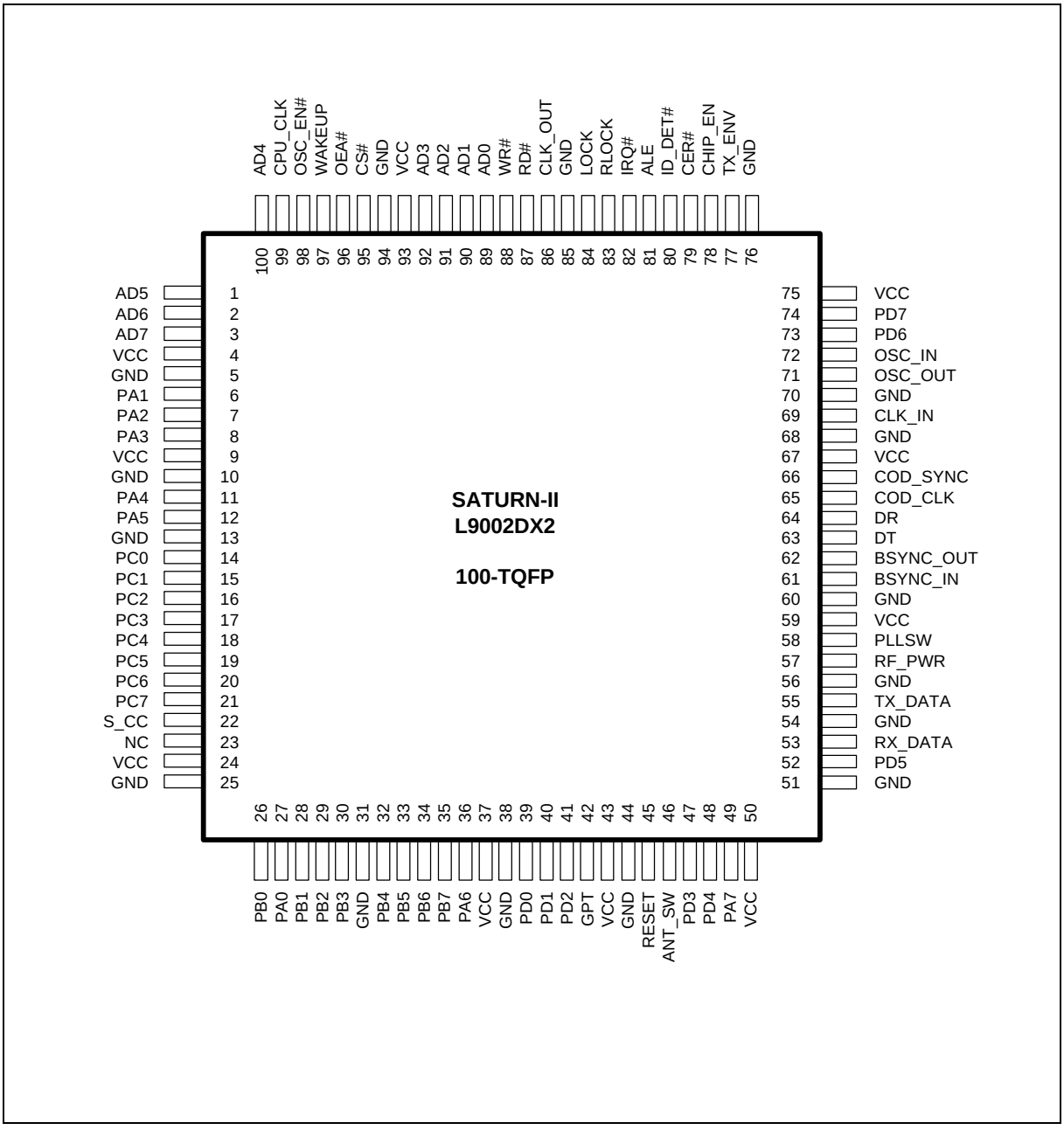
4. PIN AND BLOCK DIAGRAM

4.1 Pin Configuration

4.1.1 100-pin PQFP package



4.1.2 100-pin TQFP package



4.2. Functional Block Diagram

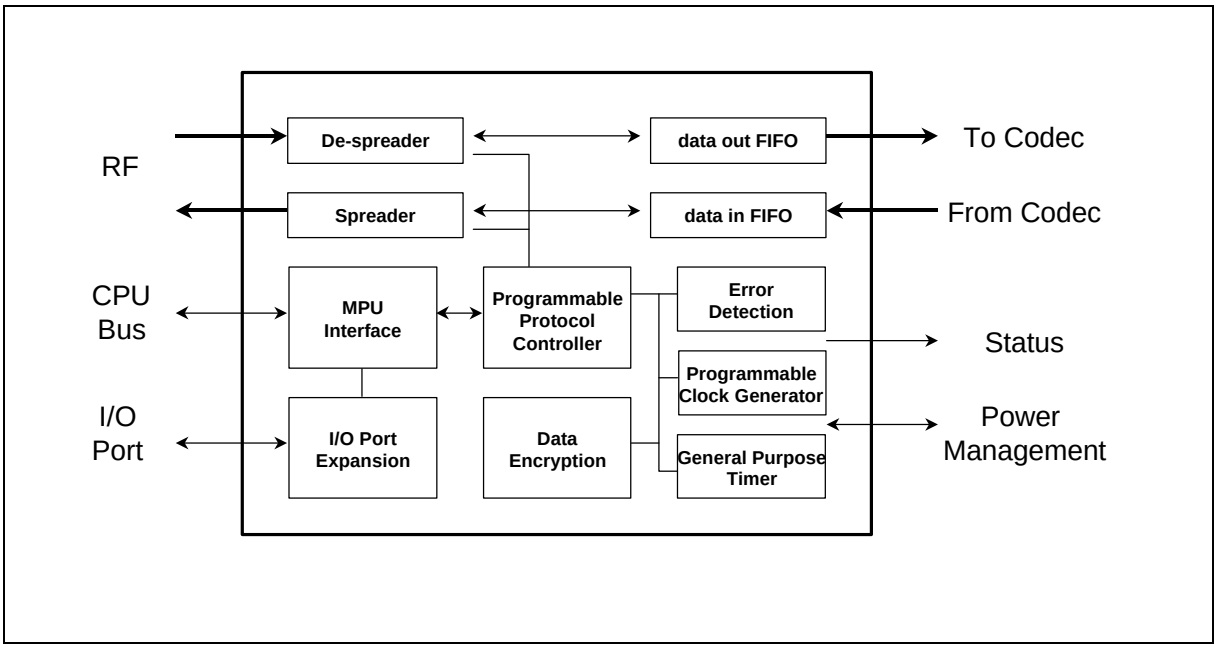
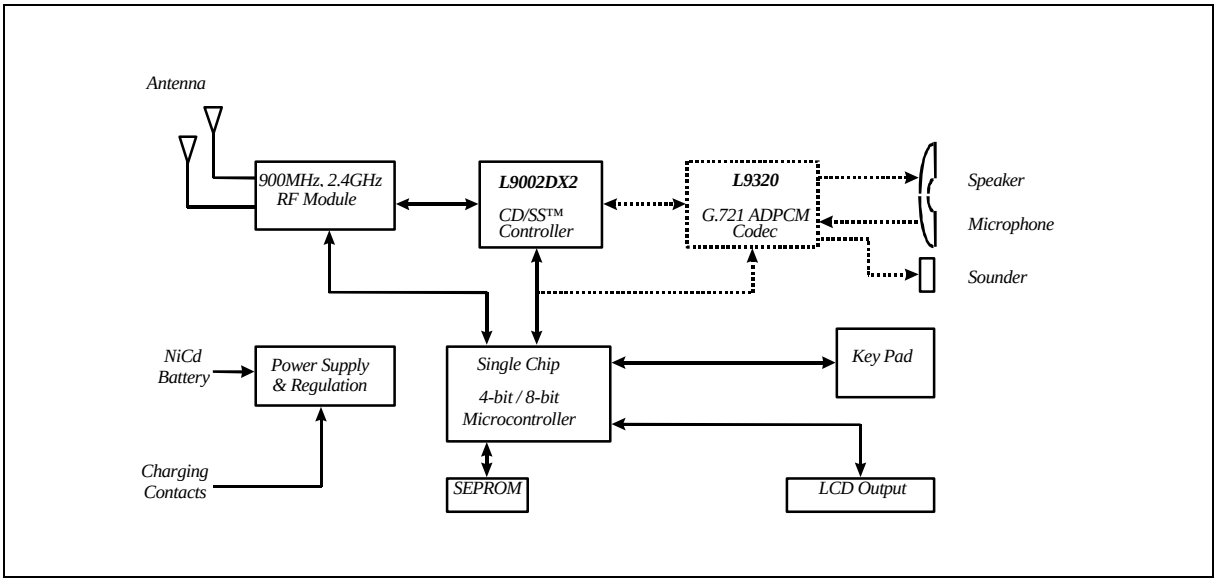


Figure 4.2.1. L9002DX2 SATURN-II internal block diagram

And simple cordless phone design (below).



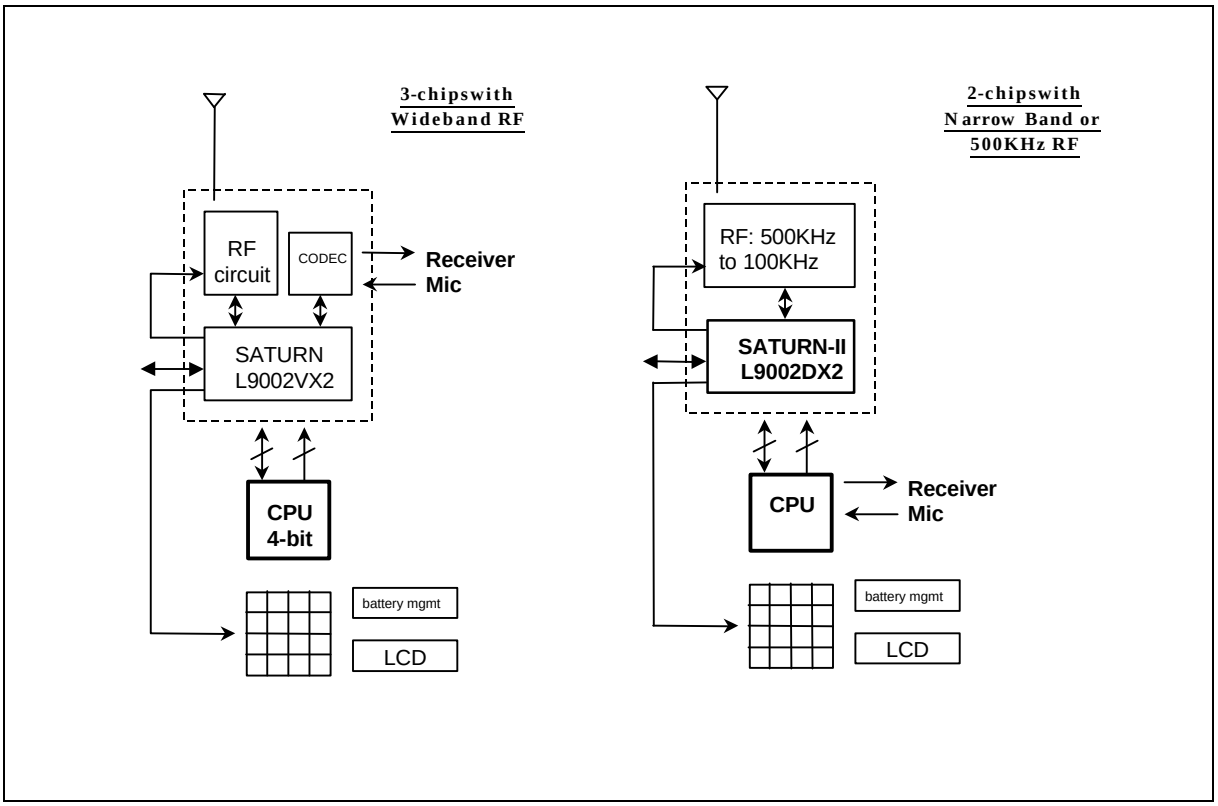


Figure 4.2.2. Cost reduced L9002DX2 cordless telephone design

5. PIN DESCRIPTION

The following table describes the external pins of the L9002DX2 in PQFP package. Due to differing package the TQFP device has a slightly different pin assignment. The following conventions and abbreviations are used in the signal descriptions:

Signal Name: All active low signals has "#" suffix; otherwise the signal is active high.

Signal Type: IN = 3V TTL input

IN_D = 3V TTL input with build-in pull down resistor

IN_U = 3V TTL input with built-in pull up resistor

OUT = 3V TTL output

OD = Open-drain 3V TTL output

IO = Bi-directional 3V TTL signal

5.1. MCU Interface

TABLE 1: Micro-controller access signals

PIN NAME	PIN NO.	I/O	DESCRIPTION
AD[7:0]	4,3,2,1, 94,93, 92,91	IO	Address and data bus. This is the multiplexed address and data bus used for micro-controller interface
ALE	84	IN	Address Latch Enable. Access address is latched at the falling edge of the ALE. The address specifies the on-chip register being accessed by the micro-controller
CS#	97	IN	Chip Select. This signal is asserted during a micro-controller access cycle.
IRQ#	85	OUT	Interrupt Request. It is asserted by the L9002DX2 to interrupt the system micro-controller at certain operation points. Interrupt is generated at the end of each transmit frame, the end of each receive frame, and when frame error is detected.
RD#	89	IN	Read Control. When RD# is asserted, read data is driven on to the AD[7:0] bus by the L9002DX2
WR#	90	IN	Write Control. When WR# is asserted, write data on the AD[7:0] bus is sampled by the L9002DX2

5.2. Codec Interface

TABLE 2: Codec Interface

PIN NAME	PIN NO.	I/O	FUNCTION
COD_CLK	67	OUT	Codec transmit and receive clock. It is used by the Codec chip to sample received data and generate transmit data. This signal is derived from the main operating frequency and is 600KHz from a nominally generated 19.2MHz Mclk (CLK_IN)
COD_SYNC	68	OUT	Codec Synchronization signal. This is an 8KHz framing clock signal used by the Codec to synchronize transmit and receive data. COD_SYNC is synchronous with COD_CLK and is generated from the main operating frequency
DR	66	OUT	Received Data. Voice data to be sampled by the Codec. It is sampled by the Codec chip at the falling edge of COD_CLK at the beginning of each frame.
DT	65	IN	Transmit Data. Voice data generated by the Codec for transmission. It is generated by the Codec at the rising edge of COD_CLK

5.3. RF Subsection Interface

TABLE 3: RF Module Interface

PIN NAME	PIN NO.	I/O	FUNCTION
PLLSW	60	OUT	Phase Lock Loop Switch. This signal switches the transceiver phase lock loop between transmit and receive mode. PLLSW is high druing transmission and the preceding gap time. It is low during receiving
RF_PWR	59	OUT	RF Power. This signal switches the transmitter and Power Amplifier on and off during full duplex operation. It is high when transmitting and low when receiving. It is enveloped by TX_ENV to ensure the proper timing sequence when the RF module switches direction
RX_DATA	54	IN	Received Data. PN data recovered from the RF module. Input to the SATURN decoder circuitry
TX_DATA	56	OUT	Transmit Data. Output of the spreader circuitry to be transmitted by the RF module. TX_DATA is a high drive output designed for analog interface but is not 5V tolerant. All other external pins are 5V tolerant.
TX_ENV	58	OUT	Transmitter Power. Switches the direction of the RF module. It is high when transmitting and low when receiving. It envelope RF_PWR by 5.5 chip time in both edges to allow PA settling

ANT_SW	48	OUT	Antenna Switch. This signal can be used to switch between two available antenna in the system. The ANT_SW signal changes state only at the beginning of the gap time between frames.

5.4 System Interface

TABLE 4: System Interface

PIN NAME	PIN NO.	I/O	FUNCTION
BSYNC_IN	63	IN_D	Burst Synchronization Input. This signal is designed to use in a PABX setup where multiple master SATURN RF is co-located together. All the BSYNC_IN signals should be connected together so that all masters starts transmission at the same time
BSYNC_OUT	64	OUT	Burst Synchronization Output. This signal is designed to use in a PABX setup where multiple master is located together. The BSYNC_OUT of the one master should be connected to the BSYNC_IN to all masters to synchronize transmission. If only one master is used, the BSYNC_OUT should be connected to the BSYNC_IN of the same device
CHIP_EN	81	IN	Chip Enable. This signal controls the internal clocks of the device. When it is de-asserted, the internal clocks remain unchanged (time freeze). The device is in operation mode only when CHIP_EN is asserted.
CLK_IN	72	IN	System Clock Input (also called Mclk)
CLK_OUT	71	OUT	System Clock Output. This signal is generated by the oscillator circuit and should be connected to the CLK_IN input
CPU_CLK	76	OUT	CPU Clock. This is the clock input to the system micro-controller. After power up, this is the main operating clock divided by 8. It can be programmed to divided by 2 or by 4
CER#	82	OUT	Check Sum Error. This signal is asserted at the end of each receive subframe to indicate that at least one single parity error has been detected. It is cleared when the control and status register is read
GPT	44	OUT	General Purpose Timer. This signal is the output of the programmable general purpose timer. The cycle time of this output is programmable between 125usec to 8.192sec with 50% duty cycle, when operating from the nominal 19.2MHz master clock
ID_DET#	83	OUT	ID Detect. This signal is set during each receive frame after a valid UID is detected in the ID field. It is clear at the end of the receive frame if the ID is not found.
LOCK	87	OUT	Lock. Indicates that the L9002DX2 is in the LOCK state with the remote device. See functional description section for more detail
RLOCK	86	OUT	Remote Lock. Indicates that the L9002DX2 is in the RLOCK state. See functional description section for more detail

S_CC	26	IN_D	Slave Clock Correction. When asserted on the slave side the system clock (Mclk) is frequency and phased locked to the TDD master. It does not affect the master side timing
NC	27		No Connect. This signal must be left unconnected in the system
OEA#	98	IN_U	Output enable for port A output pins
OSC_EN#	100	IN	Crystal Oscillator Enable. The oscillator circuit is off when this signal is de-asserted
OSC_IN	75	IN	Crystal input.
OSC_OUT	74	OUT	Crystal output.
PA[7:0]	16,15,14 ,13,10,9 ,8,7	OUT	General Purpose output port A
PB[7:4] PB[3:0]	38,37, 36,35 33,32, 31,30	OD OUT	General Purpose output port B. High nibble is Open drain.
PC[7:4] PC[3:0]	25,24, 23,22 21,20, 19,18	IN_U IN_D	General Purpose input port C. High nibble is internally pull up. Low nibble is internally pull down.
PD[7:0]	78,77, 53,50, 49,43, 42,41	IO	General Purpose I/O port D.
RESET	47	IN	System Reset. This is a synchronous reset signal. RESET must be asserted for at least ten clock cycles after initial power up
WAKEUP	99	OUT	Combinatorial output of Port C input pins. WAKEUP = PC0 | PC1 | PC2 | PC3 | ~PC4 | ~PC5 | ~PC6 | ~PC7

* All pin numbers are referenced to the 100-pin PQFP package.

6. FUNCTIONAL DESCRIPTION

The L9002DX2 is an integrated wireless baseband DSP chip. Unlike its precessors in the original SATURN family this is designed and optimized for multiple handset digital cordless telephones, multi-way family radio, packet data and wireless PABX systems such as those found in a typical small office, home office (SOHO) environment. It employs Code Division Spread Spectrum (CD/SS) technology for secure and superior voice data transmission. The additional fractional chip rate mode improves IF bandwidth coding efficiency and reduces system and RF cost. All the telephone controller functions are provided including: time division duplex control, CD/SS code spreading and despreading, direct codec and RF module interface and a general purpose I/O expansion ports.

6.1. Code Division Spreader and De-spreader

The CD/SS technique of spectrum spreading employs a high number of orthogonal frequency codes (nicknamed Color Codes) preprogrammed into the DSP processor. User data is group together to form a symbol array in the 2**N binary signal space. During transmission these symbols are subsitituted with each of the assigned Color Codes sequences, now called chips, for baseband transmission. The reception process reverses the encoding operation, but decoding decision is made according to the least mean square distance from the nearest preprogrammed Color Code to decide and return the proper symbol. As a result, channel noise impacting the received chips can be corrected to yield undistorted user data. This ability to recover the correct data under random channel noise is Processing Gain (PG). When the Color Code patterns are carefully selected to exhibit maximal binary mean square distance amongst themselves, and therefore do not self interfere (orthogonal), the Processing Gain of the CD/SS Color Coding communication system is given by the following equation:

$$PG = 10 * \text{Log}_{10}(\text{ Color Code Binary Chip Length }), \quad J/S \leq 6dB.$$

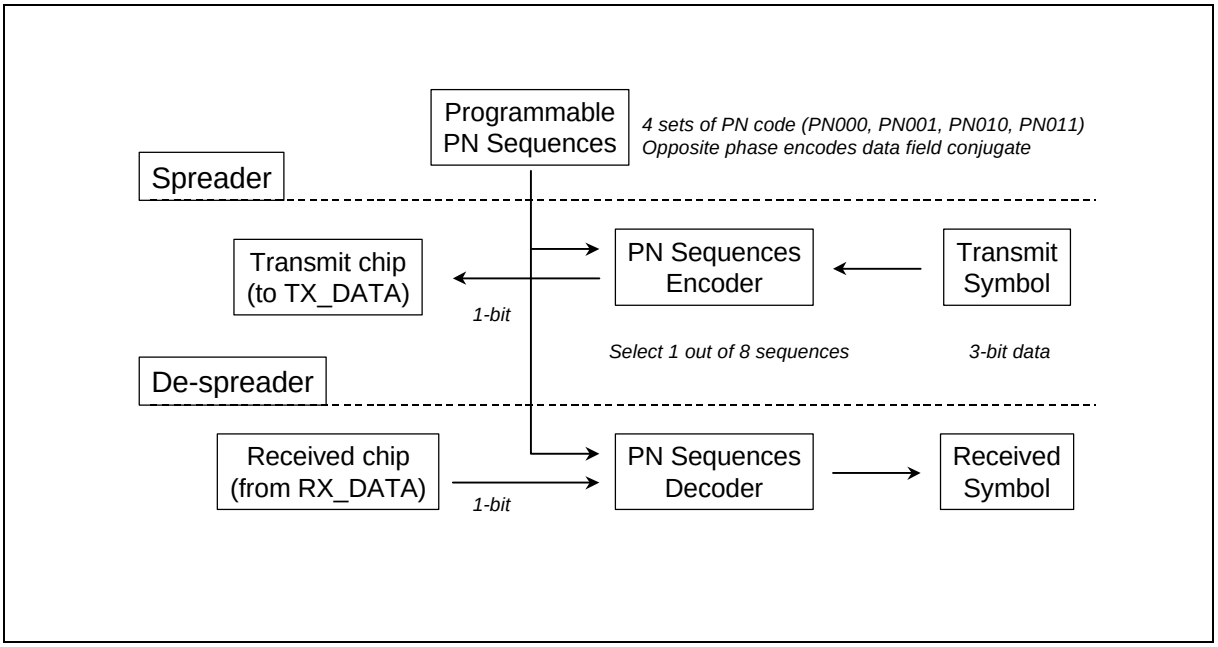
The SATURN and the SATURN-II family of CD/SS processors use 32-chips long Color Codes and the maximum processing gain is therefore 15.1dB (when the jammer to signal ratio (J/S) is less than the error margin of the 1-bit quantizer.) This Gain calculation is not affected by the number of Color Codes used to encode the user symbols provided sufficient orthogonal codes can be found. In the SATURN family the number of Color Codes used is 8, and the maximum user bits per symbol is 3 bits. Therefore the channel efficiency of the SATURN CD/SS processor is 300% of comparable Direct Sequence Spreading, under properly chosen Color Codes and when the J/S ratio margin is gauranteed in the power control of the RF circuit.

The received signal is sampled by the de-spreader in a 1-bit phase detecting quantizer at multiple times of the chip rate. This front end interface unit reduces the complexity of linear RF design and the oversampling gaurantee correct phase recovery under differential group delay, or modulation phase jitter distortions to a wide tolerance. This phase error allowance makes possible for low cost RF designs.

In the L9002DX2 fractional chip rate DSP engine, the sub band frequencies are sampled at a higher rate than the high frequency components, allowing for an increased signal resolution derived from phase quantization while keeping a uniform time delay variation on the RF circuit. This new DSP engine is optimized to yield the best performance at the one-third rate level and to yield over 10dB of

processing gain compliant to FCC Part 15.247(e) measurement criteria. The exact processing gain of the system is dependent on the CD/SS codes used and the phase jitter and distortions in the RF module which is subject to continuous improvements over time.

The following diagram shows the principal functins of the Code Division Spread and De-spreader:

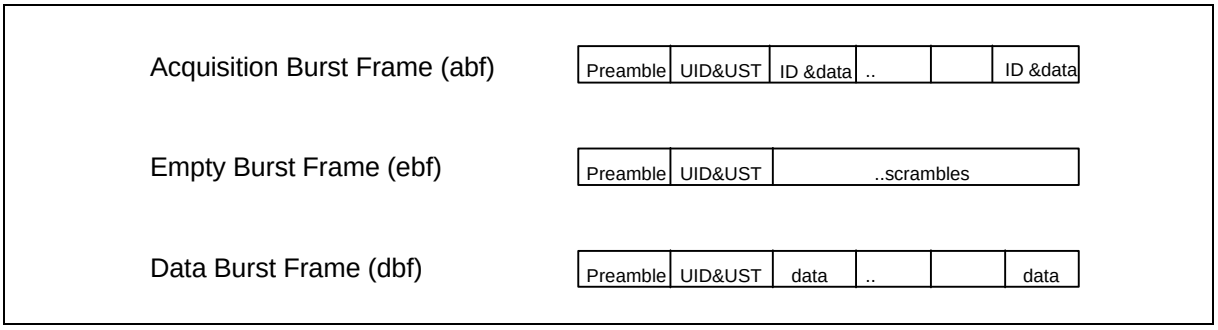


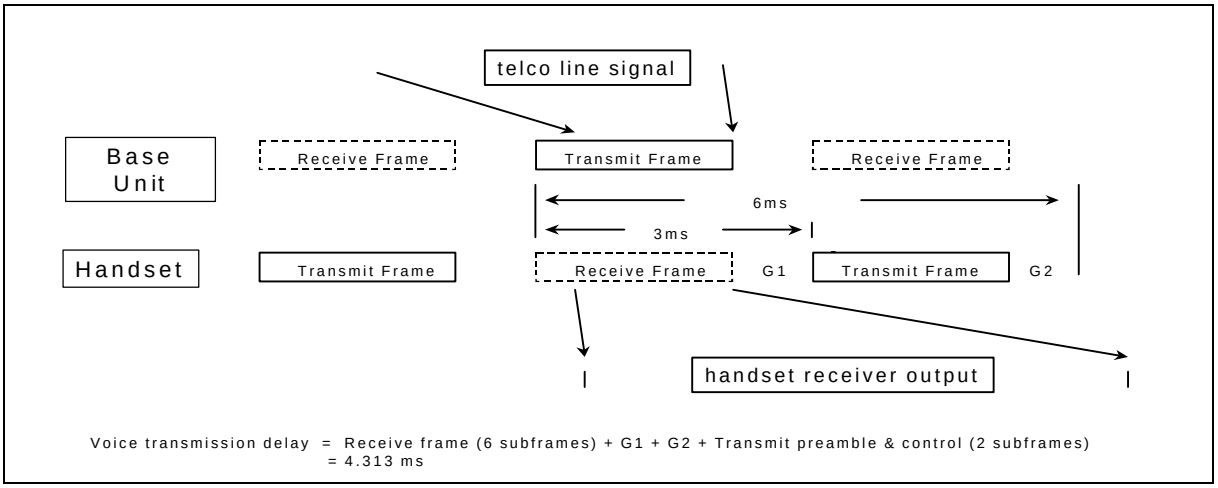
6.2. Time Division Duplex

The L9002DX2 emulates full duplex communication on a half duplex link by using time division duplex (TDD). The two communication units, one designated as master and the other designated as slave, communicate with each other by using the TDD protocol.

Within each time slot, only one device is transmitting and the other is either in idle or receiving mode. Three types of communication frames are used by the master and slave to establish communication link and transmission of data. The frame structures and the TDD timing are illustrated in the following diagram.

Protocol & Data Frames





Each frame consists of 324 bits. It includes a 54-bit preamble and five sub-frames. Each sub-frame contains 48 bits of data and 6 bits of parity. The first subframe contains 24 bits of User ID field which uniquely identifies the master-slave pair. Between transmitting and receiving of each frame, idle time equal to the transmission time of 60 bits is added for RF module switching and phase lock loop settling. At the Mclk of 19.200MHz the chipping rate is 1.365M chips per second. The transmission time of one frame including the idle time is exactly 3.000 ms. With 192 bits of user data transmitted per frame, the full duplex data field carries 32Kbps in each direction. These rates are scalable with Mclk.

Communication is initiated in the master by sending the acquisition frame (abf). When the slave acquires the acquisition frame and correctly matches all the UID fields to less than 2 symbol errors, it declares a valid abf frame is found and responds by sending another acquisition frame to the master. The abf subframe is modified in the L9002DX2 under data mode from prior SATURN generations to carry an addition 12-bytes of data equally embedded in each subframes.

When the master receives the return abf with the correct UID, it responds by sending the empty frame (ebf) to the slave. The slave responds by sending another empty frame and the communication link is thereafter established.

Once the TDD link is established, the master and the slave take turns in sending data frames. Each

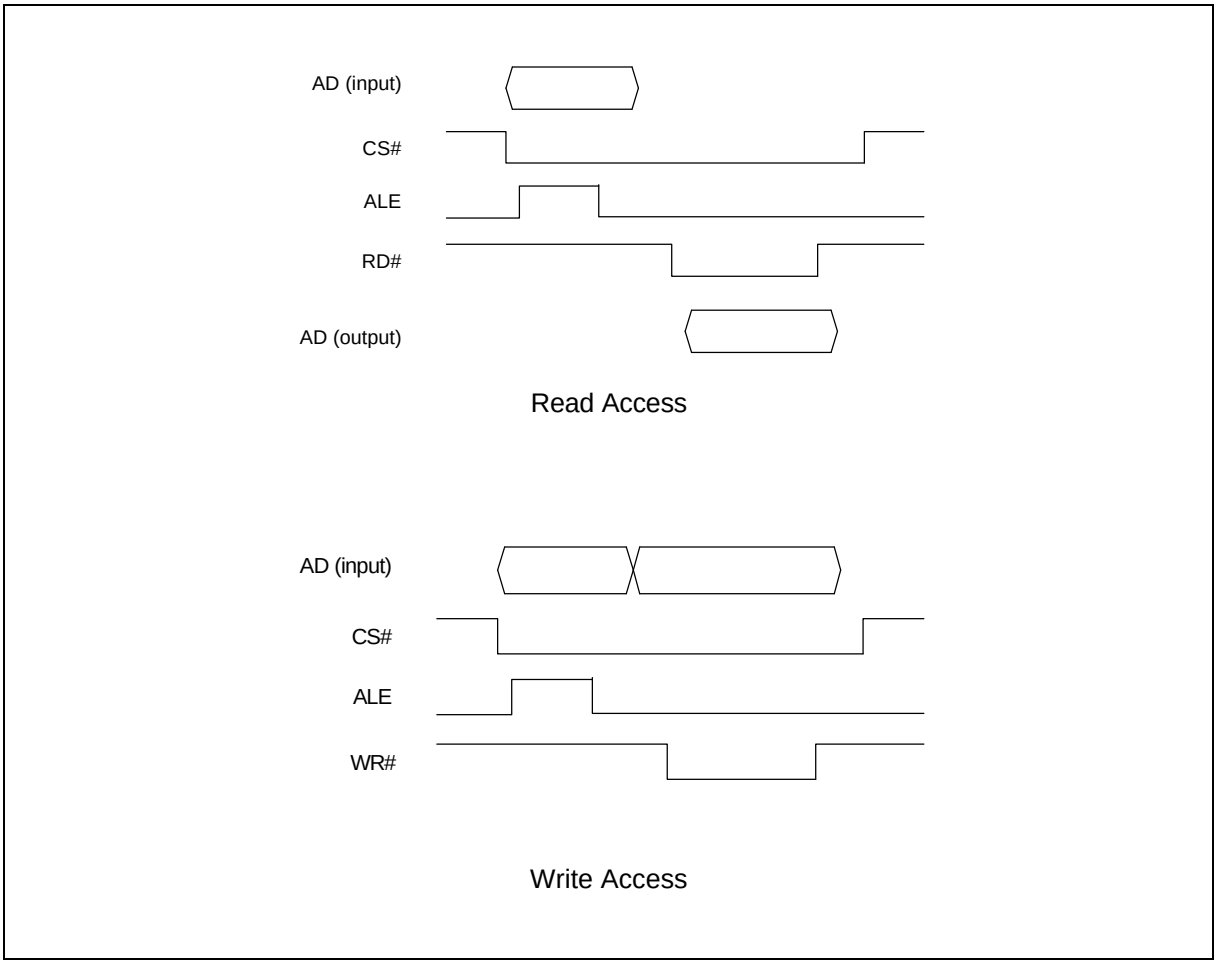
data frame contains the UID and status subframe to identify the intended receiver and the command/status information in addition to user data.

6.3. System Controller Interface

Interface to the system controller is through the on-chip registers, the interrupt pin and a group of auxilliary status signals.

6.3.1 Control Register Access

The control registers of the L9002DX2 can be accessed by the system controller through a simple bus interface. The registers and the I/O expansion ports are uniquely identified by an 8-bit address. The following diagram illustrates the read and write access timing to the on-chip registers.



Each access must be enclosed by the assertion of CS#. As soon as CS# is asserted, the access address can be specified at the AD bus with ALE asserted. The access address is latched by the

falling edge of ALE. Once the address is latched, the access command can be specified by asserting the RD# or WR# signals. If RD# is asserted, the read data is driven by the L9002DX2 on to the AD bus. The system controller must tri-state the AD bus before asserting RD# to avoid data contention.

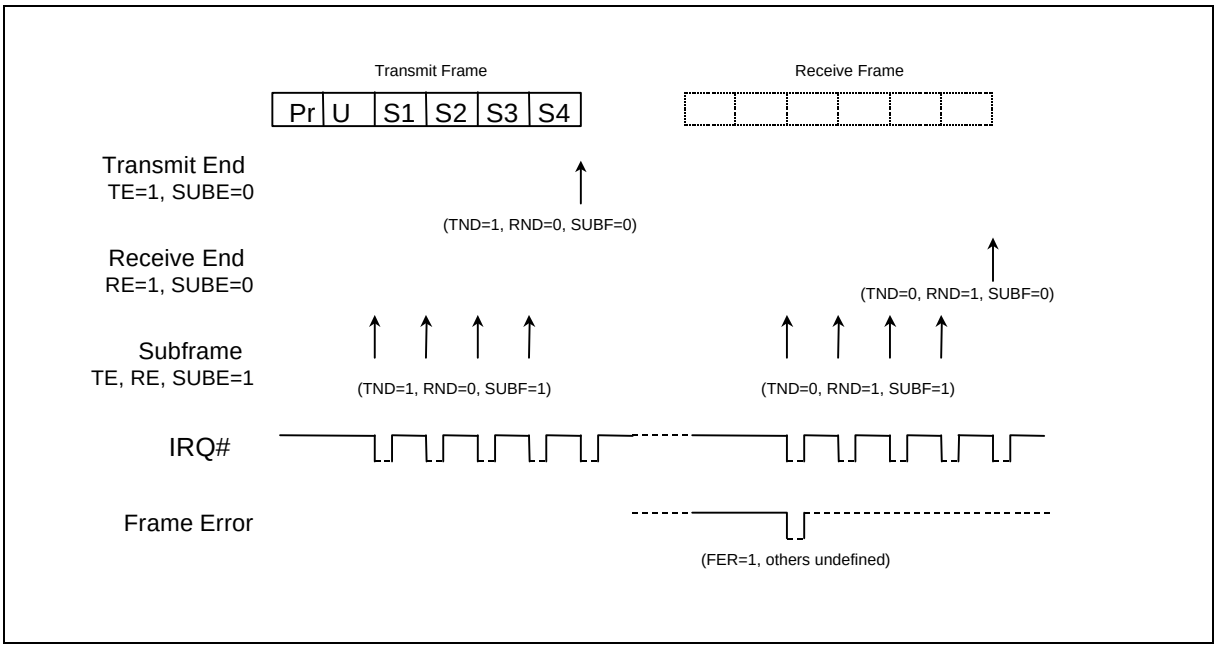
If WR# is asserted, the data on the AD bus is written into the register specified during ALE. The valid data must be driven on the AD cus before WR# is asserted.

6.3.2. Interrupt

The L9002DX2 can be programmed to generate system interrupt at the end of each transmit or receive frames or subframes.

If the TE bit in the command register is set, an interrupt is generated at the end of each transmit frame. If the SUBE bit in the command register is also set, interrupt is generated at the end of each transmit subframes in addition to the end of frame. The RE bit in the command register has similar function but is applied to receive frame and subframes.

When an interrupt, IRQ#, is asserted, it remains asserted until the status register is read by the controller. When the status register is read, some status bits and the IRQ# pin are cleared at the same time. If the status register is not read before the next interrupt arrives, the second interrupt may not be detected since IRQ# remains asserted starting from the first interrupt. Below is a diagram on the interrupt generation and control.



6.3.3. Auxiliary status signals

The L9002DX2 provides additional status signals to assist system design.

The LOCK signal is asserted after the device successfully receive an acquisition frame (abf). It remains asserted until the communication link is declared broken.

The RLOCK signal is asserted after the device successfully receive an empty frame (ebf). It remains asserted until the communication link is declared broken.

The communication link is declared broken whenever the Sticky Counter expires. The Sticky Counter, if enabled and programmed to a positive value, will be decremented by one whenever a frame error (FER) is detected in the middle of TDD communication. It is restored to its original value at the end of a valid received frame that satisfies the UID detection criteria. It expires when it reaches a zero value.

ID_DET# is asserted when the receiving device detects the correct User ID in the receive frame. It is asserted around the middle of the first subframe of the receive frame. Once asserted, it remains asserted until the end of the frame. The L9002DX2 allows up to two symbol errors within the UID field. That is, ID_DET# is asserted if two or less symbol error is detected in the ID field.

CER# is asserted when the parity error is detected in any subframe. It is cleared when the status register is read by the system controller.

6.3.4. Data Transfer

When the L9002DX2 operates at data mode, the transmit and received data are buffered internally in the L9002DX2 through two FIFO. Control register 16 (hex) is the input port to the transmit data FIFO. Up to three subframe of data can be buffered in this FIFO before starting transmission. The system controller must deposit at least one sub-frame worth of data into this FIFO before the beginning of a transmit frame.

Control register 17 (hex) is the output port of the receive data FIFO. Data received by the L9002DX2 are deposited here and must be read at the end of each receive sub-frame. When the received FIFO is empty the value read by the system controller will be the value stored in the Quiet code register at location 03 (hex.)

When parity mode is enabled, each sub-frame carries 48 bits of user data. Since the transmit FIFO is byte-wide, 6 bytes should be written into this FIFO for each sub-frame of data. When parity mode is disabled, the user can transmit 6 extra bits of data with each sub-frame. The 6 extra bit must be written into the FIFO through control register 13 (hex). Before each 6 byte of data is written, the 6 bits of extra data must first written into control register 13. Immediately afterwards, the 6 bytes of user data is written into register 16 (hex). Together they form 54 bits of user data for the sub-frame.

To receive 54 bits of data for each subframe, the system controller must first read out 6 bytes of data from control register 17 (hex) and then read control register 13 (hex) for the 6 extra bits.

6.3.5. Burst Transfer Mode

The L9002DX2 acquisition burst frames now carries 12-bytes of data in the subframes. In addition to sending the 24-bit UST field in the abf, 3-bytes of user data each alongside with one UID is sent in every subframe field. These transmit data are taken from the transmit FIFO during abf transmission. To use this feature the transmit FIFO shall be filled with the entire 12-bytes before the acquisition frame is sent.

The received acquisition frame carries an extra 12-bytes of data. Whenever a valid preamble is declared received alongside with the validation of the first UID field to less than 3 symbol difference from the receiver's own UID, these data will be deposited into the receive FIFO.

The use of the abf burst transfer mode allows sub-sensitivity level packet communication between 2 SATURN units under a highly noisy environment.

6.4. Clock Generator

The L9002DX2 nominally operates with the system crystal or oscillator at 19.200MHz.

The CLK_IN signal is the system clock input pin. All internal timing signals, including the chip rate and sampling rate, are generated from this main clock. The system clock can be supplied by an external source or can be generated through the on-chip oscillator circuit.

The on-chip oscillator circuit consists of four pins, OSC_IN, OSC_OUT, OSC_EN# and CLK_OUT. The OSC_IN and OSC_OUT pins are connected to an external crystal. OSC_EN# should be asserted (low) to enable the oscillator circuit. CLK_OUT is the buffered output of the oscillator which is capable of driving multiple external devices. If the on-chip oscillator is to be used to generate the system clock input, CLK_OUT and CLK_IN should be connected together externally. If the system clock is provided by another external source different from the on-chip oscillator, the oscillator circuit can be turned off by de-asserting OSC_EN#. The external clock source should drive the CLK_IN input directly. In power down mode the OSC_EN# signal can be de-asserted to stop the oscillator and the system clock to conserve power.

The L9002DX2 contains a programmable clock generator to generate a divided-down CPU clock to the system controller. The CPU clock output from the L9002DX2 can be programmed to run at 9.6MHz, 4.8MHz, 2.4MHz (CLK_IN divided by 2, 4 or 8) or off. After system reset, the CPU clock runs at 2.4MHz (divided by 8).

6.5. Codec Interface Bus

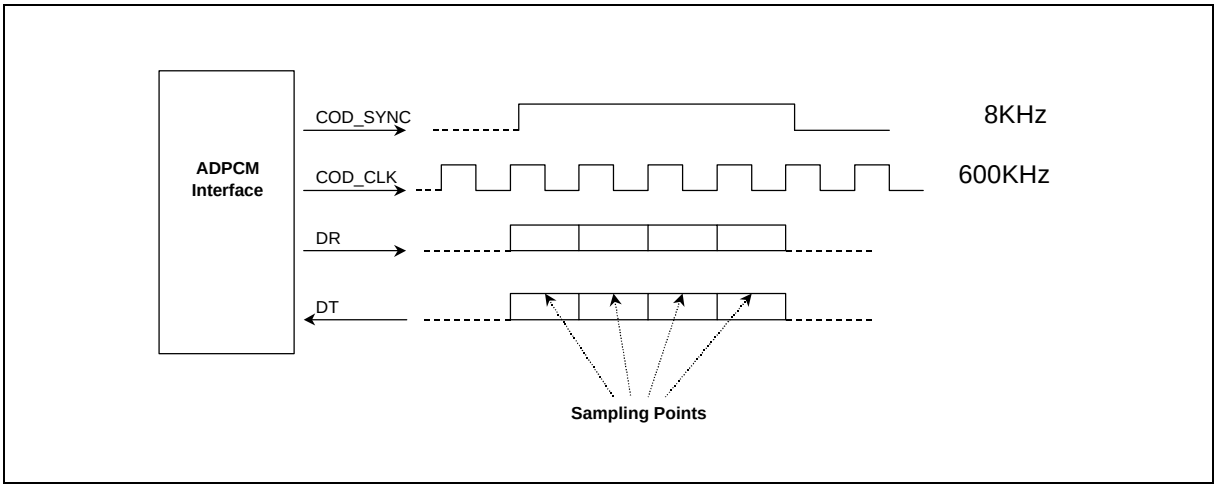
The L9002DX2 supports all ADPCM Codec chips that are compatible with the CCITT G.721 recommendation and ANSI T1.301. Once the communication is established between the master and slave, the L9002DX2 interfaces directly with the codec to retrieve transmit data and send out received data. It generates codec framing signal COD_SYNC and clocking signal COD_CLK.

The COD_SYNC signal is a 8KHz signal nominally generated from the system clock. The COD_CLK signal is 600KHz, equivalent to 75X of COD_SYNC.

The rising edge of COD_SYNC defines a data frame for the codec chip. The COD_SYNC signal remains high for four COD_CLK cycles. The codec chip samples four bits of data at the falling edge of COD_CLK while COD_SYNC is high. User data recovered by the despreader of L9002DX2 is stored in on-chip FIFO and then output on DR to be sampled by the codec, synchronized with COD_SYNC and COD_CLK signals.

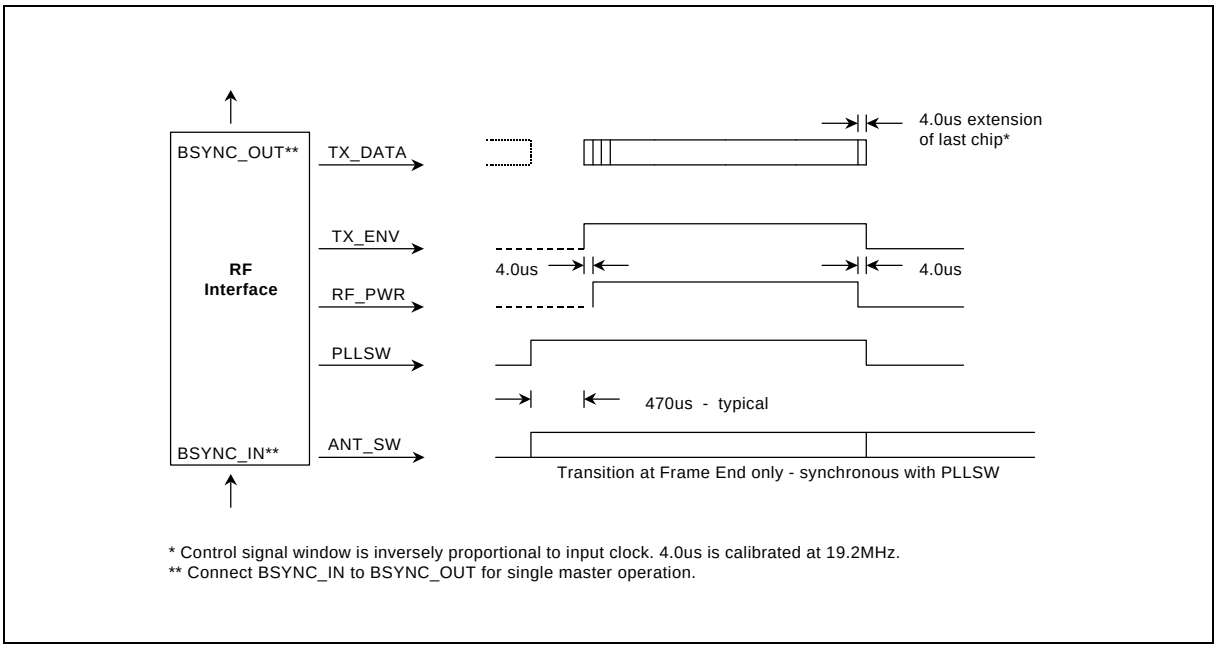
Data to be transmitted by the L9002DX2 is generated by the codec at the first four rising edges of COD_CLK of each data frame. The transmit data, DT, is sampled by the L9002DX2 at the falling edge of COD_CLK and stored in on-chip FIFO. During transmission time, data is read from the FIFO and send out to the RF module through the spreader.

The following timing diagram illustrate the timing of the codec interfaces.



6.6. RF Interface

The RF subsystem interface consists of the PLLSW, RF_PWR, TX_ENV, TX_DATA, RX_DATA and ANT_SW signals. The PLLSW, RF_PWR and TX_ENV signals control the RF module to be in receive and transmit state. The ANT_SW pin is used only in dual antenna design to select one of the two available antenna. The value of ANT_SW pin follows the ANTSW bit in the control register. At the end of a transmit frame or receive frame, the value stored in the ANTSW bit is latched to the ANT_SW output. During transmit or receive frame, ANT_SW output remains unchanged. The following timing diagram illustrates the RF control signals when switching between transmitting and receiving.



* Control signal window is inversely proportional to input clock. 4.0us is calibrated at 19.2MHz.
** Connect BSYNC_IN to BSYNC_OUT for single master operation.

6.7. Reset

The L9002DX2 can be reset through hardware or software. Hardware reset is when the RESET input is asserted with the system clock running. Software reset is done by writing a “one” to the RST bit in the command register. Hardware reset and software reset are very similar except that some control registers return to their default values through hardware reset while some other control registers return to default value through either reset. The register description section of this data sheet describes the conditions when each register returns to default value. It should be noted that some register values such as IO expansion ports are not affected by either reset. After system power-up, the RESET signal must be asserted for at least ten cycles before the system can function properly.

When the RESET signal is de-asserted, the L9002DX2 enters the standby mode. During standby, all the control registers holds its current value and the system controller interface and I/O expansion blocks are fully functional. All control registers, including the command registers, should be programmed by the controller during standby mode. Once programming is completed, the STRT bit in the command register can be set to start operation.

6.8. Advanced Power Management

The L9002DX2 has three power down modes: sleep, freeze and standby.

Sleep mode has the lowest level of power consumption. The device enters sleep mode when OSC_EN# is de-asserted. If the system clock, CLK_IN, is supplied by an external source, it should also stop toggling. Most of the function of the L9002DX2, including CPU_CLK, general purpose timer, Codec interface, are stopped in sleep mode. The controller interface and I/O ports are still operational. All control registers and IO ports retain their values and control register can still be accessed through the controller interface. However, reading the status register would not clear the IRQ# signal. In order to conserve power, controller bus activity and register access should be kept to the minimum.

To exit from sleep mode, the device must go throught the standby mode. The device must first be reset throught hardware reset or software reset. While reset is on, OSC_EN# or external clock can be re-asserted. The hardware or software reset can then be removed and the device is now in standby mode.

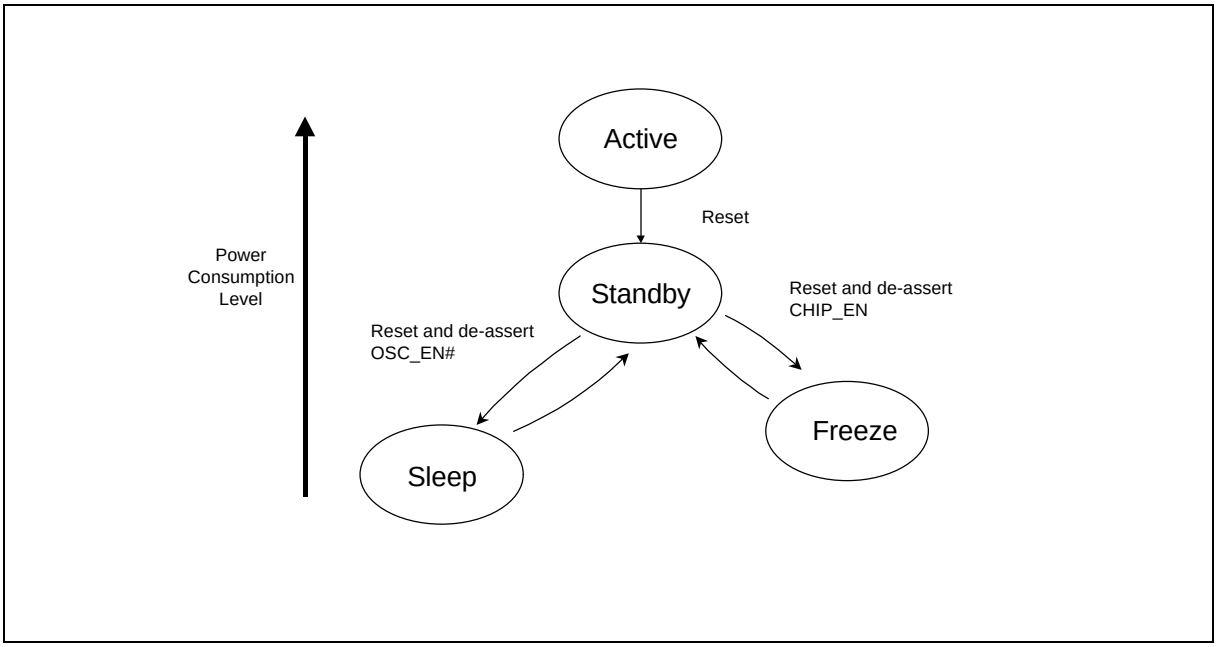
Freeze mode is the second lowest level of power saving. The device enters freeze mode when the CHIP_EN input is de-asserted. It is similar to sleep mode except that since the system clock is still toggling, the CPU_CLK and general purpose timer functions are still operational. Exit from freeze mode is similar to exit from sleep mode.

Standby mode is entered by executing a hardware or softwae reset while system clock is running. In standby mode, the device is operational except that communication protocol is not running. When the STRT bit in the command register is set, the device exit standby mode and becomes fully operational.

In order to ensure that the device enters sleep or freeze mode with all output pins at the proper setting, the device must be first reset through hardware or software before entering either sleep or freeze modes.

If the on-chip oscillator is not used and the system clock is supplied by an external source, the OSC_EN# pin must be de-asserted at all time to avoid any device switching noise and to minimize power consumption.

The diagram below represents various power management states:



6.9. Advance Noise Reduction

During voice communication, audible noise can occur in the system through two mechanisms: (1) random bit error or (2) communication link broken from receive frame error. A third mechanism that could exist in systems with ADPCM codecs running from different crystal frequencies other than Mclk, thereby causing FIFO over and underflow. This third noise causing mechanism can be fully avoided using the Slave Correction Mode in the L9002DX2 by asserting the S_CC control at pin 26. Therefore it is not described here.

The first error is generated from wireless bit error resulting from excess channel noise, causing the CD/SS engine to make wrong symbol decisions. This generally occur when the chip error rate is higher than 10E2, or 1 to 10 random error in every 100 received chips. This is notified to the controlling software by the CER# pin and the CER bit. Proper software muting can be applied to the ADPCM Codec if desired. However, the ADPCM voice coding algorithm is inherently robust against single, random bit noise without much artifact so the extra muting is generally not need, and are not recommended. A better mechanism is to take link layer actions before bit error occurs. The Signal to Noise Indicator (SNR register value) degrades before the error rate reaches 10E3, or 1 to 10 error in every 10,000 chips. It should be used as early warnings to the link layer to take proper action on RF power level, or to make a hopping decision before actual symbol error occurs would occur.

The second mechanism is generated when the SATURN-II receiver cannot acquire the receive data frame. This event is signaled to the controller as frame error and the communication link must be reestablished. The L9002DX2 is programmable in handling of frame error. If the STKY bit in the command register is cleared, the L9002DX2 will immediately declare lose lock on frame error. The LOCK and RLOCK signals, along with LK and RLK bits will be dropped and it will try to re-establish the link by sending and receiving acquisition frames. If the STKY bit in the command register is set, the L9002DX2 continues to transmit its data frame on frame error for a few times. If it receive a correct data frame during this time, the communication link remains intact. It declares lock lost only when it cannot receive the correct data frame after several attempts. The number of attempts it

continues to transmit on frame error is also programmable by the user through a the control register.

During the time when no data is received, the L9002DX2 sends the quiet code to the ADPCM Codec which is the value stored the Quietcode register. This eliminates the need for audio signal muting by software during frame errors.

6.10. Data and Voice Encryption

Data transmission using Code Division Spread Spectrum technology is inherently secure due to the use of user selectable pseudo random Color Codes. The L9002DX2 adds another level of data security by allowing the user to encrypt the transmit data on a frame-by-frame basis. The transmit data can be encoded by a random sequence generated on-chip. Only receivers programmed with the same seed can decipher the received frame correctly.

The random sequence is generated by the following polynomial f(X):

$$f(X) = 1 + X^2 + X^3 + X^5 + X^{11}$$

Unique random sequence is defined by the user by initializing the value of X^0 to X^7 through one of the control registers. If this seed vector is set to value of 0x00(hex), the encryption function is turn off.

6.11. Error Protection

Error detection is built-in to the L9002DX2. Every 8 bits of transmitted data is accompanied by a parity bit. Parity generation and detection is automatically performed. The CER bit in the status register and CER# output pin signals when parity error is detected. They are set within each subframe when parity is detected and are cleared when the status register is read.

6.12. Signal to Noise Indicator

Code Division Spread Spectrum algorithm recovers the correct symbol by making decision based on a least mean square algorithm. The total sum of the error magnitude is accumulated inside the Signal to Noise Indicator (SNR) register, which stores the accumulative value of the error factor on each received data frame starting from the beginning of the preamble lock phase. If the subframe interrupt bit, SUBE, is turned on and the signal strength indicator is read on each subframe and received frame end, the value is always increasing from the first interrupt until the last interrupt of the receive frame. This value provides a very good indication of how clean the communication link is as seen by the L9002DX2.

The signal strength indicator is a relative value. Higher value indicates stronger signal with relatively few chip mismatches. A value of 0x5F(hex) can be expected at frame end when strong signal is received. When frame error is detected on the received frame, the signal strength indicator does not carry any meaningful value.

6.13. General Purpose I/O Expansion Ports

The L9002DX2 contains four I/O expansion ports to facilitate system design. Port A and port B are

output ports with PA[7:0] and PB[7:0] as the corresponding output pins. Port A can be tri-stated by de-asserting the OEA# input pin. Port B is divided into two halves. The lower half, PB[3:0], has regular output buffers and is always enabled. The upper half, PB[7:4], has open drain outputs. Both port A and port B are bit address-able as well as byte address-able.

Port C is an input port with pins PC[7:0]. It can be read through the control register and also feeds to a combinational output signal. The output signal, WAKEUP, is defined with the following boolean logic equation:

WAKEUP = PC0 | PC1 | PC2 | PC3 | ~PC4 | ~PC5 | ~PC6 | ~PC7

Port D is a general purpose I/O port. It functions as an output port when the IO control bit in register 0x44(hex) is cleared. If the IO control bit is set, the output buffers on pins PD[7:0] are tri-stated and the input value can be read.

The internal registers holding the value of all ports are static registers and are not affected by software reset or power management functions. All ports can be written or read from when the system clock is turn off. Upon hardware reset, port D becomes an input port and the registers holding the output values are set. Port B is also set by hardware reset.

6.14. General Purpose Timer

A general purpose timer is included in the L9002DX2. It can be used by the system designer for various functions such as watch dog timer or tune generator. The output signal GPT is a 50% duty cycle signal and the cycle time is programmable between 125us (8KHz under nominal master clock) to 8.2 seconds. The cycle time is controlled by the two 8-bit registers at 0x46(hex) and 0x47(hex) with 47 being the upper byte and 46 being the lower byte. Together they form a 16-bit value which becomes the multiplying factor for the cycle time with 125us being the basic time unit. When the CLK_IN is deviated from the nominal 19.200MHz the basic time factor scales linearly. When both GPT control registers are cleared, the GPT output stops toggle.

6.15. Slave Clock Correction Mode

This is a new function implemented in the L9002DX2. Asserting this mode by connecting the S_CC signal (pin 26) to high before a hardware reset. The function of this mode only affects the SATURN controller operating in the slave mode. It will digitally phase and frequency lock the internal slave processor clock to the master SATURN after TDD has been established. This will ensure multiple clocking systems used either in conjunction with or independently in the ADPCM Codec to operate from the same master frequency, session by session. The gauranteed locking range between the two crystals is 210ppm deviation.

7. REGISTER DESCRIPTION

7.1. Introduction

The control registers of the L9002DX2 can be accessed through the system controller interfaces. This section describes each control register in detail.

The following table lists all the control registers. The register types are: R/W = Reand and Write-able, W = Write only register, R = Read only register

REGISTER	TYPE	ADDRESS (HEX)	HARDWARE RESET VALUE
Command 1 / Status	R/W	00	00000000
Command 2	R	01	00000000
Quiet Code	W	03	10000000
Transmit ST fields (UST)	W	04 – 06	-
Received ST fields (UST)	W	08 – 0A	-
System ID (UID)	W	0C – 0E	-
CPU Clock Divider	W	10	00000011
Preamble Search threshold	W	12	00001000
Extra Data	R/W	13	00000000
Signal Strength Indicator	R	14	-
Preamble Search & Lock count	W	15	00110111
Transmit Data FIFO	W	16	-
Receive Data FIFO	R	17	QUIETCODE ON EMPTY
Scrambler	W	1E	00000000
Sticky Count	W	1F	00000011
PN code, symbol zero	W	20 – 23	-
PN code, symbol one	W	24 – 27	-
PN code, symbol two	W	28 – 2B	-
PN code, symbol three	W	2C – 2F	-

I/O expansion port, PA, bit wise	W	30 – 37	-
I/O expansion port, PB, bit wise	W	38 – 3F	-
I/O expansion port, PA, byte wise	W	40	-
I/O expansion port, PB, byte wise	W	41	11111111
I/O expansion port, PC	R	42	-
I/O expansion port, PD	R/W	43	11111111
PD I/O direction control	W	44	11111111
GPT Timer, lower byte	W	46	00000000
GPT Timer, upper byte	W	47	00000000
Diversity Control Register	R	71	-
Diversity Control Setup	W	72 - 73	-
Reserved		ALL OTHERS	-

Table 7-1 Read/Write Status Description and Reset values in L9002DX2 Control Registers

7.2. Byte Register Description

7.2.1. Address 00: Command 1 / Status, Read/write, default = 00000000

Both the Command 1 register and Status register are maped to address 0x00. When this address is written, the input data is written into Command ! register in the following format.

	B7	B6	B5	B4	B3	B2	B1	B0
CSR1	0	D/P	REC	DATA	ANTSW	RST	STRT	STKY

Bit 7:

Must be written as 0.

Bit 6:

Select between parity and user data mode. If this bit is 0, parity generation is enabled. If it is 1, parity is not enabled and each sub-frame carries 6 extra bits of user data. When the device operates in voice mode, parity is always enabled and this bit is ignored.

Bit 5: Receive Only bit

If this bit is set and the device is operating in slave mode, it does not transmit any response frame even when a valid acquistion frame (abf) is detected.

Bit 4:

Voice/Data mode select. If this bit is 0, the device operates in voice mode. If this bit is 1, the device operates in data mode.

Bit 3: Antenna Switch bit

The output signal ANT_SW reflects the value of ANTSW bit. When the value of ANTSW bit changes, the output signal ANT_SW will change state only when the PLLSW output change state.

Bit 2: Software Reset bit

Setting this bit would have similar effect as asserting the RESET external input pin (hardware reset). The RST bit is cleared when the external RESET pin is asserted. Write one to this bit to enter soft reset state and write zero to exit soft reset.

Bit 1: Start bit

The device enter and starts normal operation when this bit is set.

Bit 0: STICKY bit

This bit enables the sticky count register (0x1F) when it is set. See description of the sticky count register for more detail.

When register location 0x00 is read, the status register value are outputted with the following format.

	B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
CSR1	LK	RLK	ANTST	SUBF	FER	CER	TND	RND

This register should be read by the system controller at each interrupt. Bit 4 to 0 and the interrupt request pin, IRQ#, are deasserted after each read.

Bit 7: Lock bit

This bit is set whenever an acquisition frame (abf) has been received by the device. Once set, this bit remains set unless the communication link is declared broken.

Bit 6: Rlock bit

This bit is set whenever an empty frame (ebf) has been received by the device. Once set, this bit remains set unless the communication link is declared broken

Bit 5: Antenna State bit

This bit has the same value as the prior state of the ANT_SW output pin.

Bit 4: Subframe End

The bit is set whenever an interrupt is generated at the end of a subframe. When interrupt is generated at the end of a complete data frame, this bit is cleared. This bit has valid information only when FER bit is cleared.

Bit 3: Frame Error

The bit is set when the device fail to detect the frame preamble or when system ID mismatch

condition occur. When this bit is set, bit 4, 2, 1 and 0 does not hold valid information.

Bit 2: Checksum Error

The bit is set if parity error is detected in any subframe. This bit is cleared every time this register is read.

Bit 1: Transmit End

The bit is set at the end of a transmit frame or subframe.

Bit 0: Receive End

This bit is set at the end of a received frame or subframe.

7.2.2. Address 01: Command 2, write only, default = 00000000

	B7	B6	B5	B4	B3	B2	B1	B0
CSR2	0	FLIP_TX	FLIP_RX	SUBE	TE	RE	M/S	T/N

Bit 7: Reserved

This bit is reserved.

Bit 6: FLIP TX

When this bit is set, the TX_DATA output pin has reversed polarity.

Bit 5: FLIP RX

When this bit is set, the RX_DATA input pin is interpreted with reversed polarity.

Bit 4: Subframe Interrupt Enable

If SUBE and either TE or RE is set, an interrupt is generated at the end of each transmit or receive subframe, depending on TE and RE. If SUBE is clear while either TE or RE is set, an interrupt is generated only at the end of each full data frame.

Bit 3: Transmit End Interrupt Enable

Setting this bit would enable an interrupt to be generated at the end of each transmit frame or subframe.

Bit 2: Receive End Interrupt Enable

Setting this bit would enable an interrupt to be generated at the end of each receive frame or subframe.

Bit 1: Master / Slave mode select bit

The device functions as a master when this bit is set. It functions as a slave if this bit is cleared.

Bit 0: Test / Normal mode select bit

This bit must be cleared for normal operation.

Bit 7 to 0 are cleared on hardware or software reset.

7.2.3. Address 03: Quiet Code, write only, default = 10000000

	B7	B6	B5	B4	B3	B2	B1	B0
	1	0	0	0	0	0	0	0

This register controls the output value of the receive data FIFO when data underflow occurs. The value equal to the quiet code of the CODEC should be written into this register. When data underflow occurs, value of this register is outputted to the CODEC.

This register is set to the default value on hardware reset and it is unaffected by software reset.

7.2.4. Address 04 – 06: Transmit Status, write only, no default value.

	B7	B6	B5	B4	B3	B2	B1	B0
STO	7	6	5	4	3	2	1	0
	15	14	13	12	11	10	9	8
	23	22	21	20	19	18	17	16

The transmit status field (UST) is sent by the L9002DX2 during all transmission frame. Value of the STO field is defined by the system controller and is not interpreted by the L9002DX2.

7.2.5. Address 08 – 0A: Received Status, read only.

	B7	B6	B5	B4	B3	B2	B1	B0
STI	7	6	5	4	3	2	1	0
	15	14	13	12	11	10	9	8
	23	22	21	20	19	18	17	16

The received status field stores the status value received from each receive frame. These registers are updated at the beginning of each receive frame after the status are received. Value of the STI field is defined by the system controller and is not interpreted by the L9002DX2.

7.2.6. Address 0C – 0E: System User ID, write only, no default value

	B7	B6	B5	B4	B3	B2	B1	B0
UID	7	6	5	4	3	2	1	0
	15	14	13	12	11	10	9	8
	23	22	21	20	19	18	17	16

These registers contain the system User ID. Address 0C contains the least significant bits and 0E contains the most significant bits. The first two bits of register 0E, UID[23:22], MUST BE programmed with “10”. Both the master and the slave should be programmed to the same UID value.

The L9002DX2 contains the new Mirror ID support mode. When mirror ID (MID) is used the first 2 bits of register 0E, MID[23:22], should be programmed with “01” to represent the mirror mode operation. For more details about the Mirror UID mode operation please consult Lanwave Technical Support.

The value of these registers are unaffected by hardware and software reset. They are undefined after system power up.

7.2.7 Address 10: CPU CLK, write only, default 00000011

	B7	B6	B5	B4	B3	B2	B1	B0
	0	0	0	0	0	0	CU1	CU0

Bit 1 to 0 defines the CPU clock divider. If bit[1:0] = 11, CPU_CLK output equivalent to CLK_IN divided by 8. If bit[1:0] = 10, CPU_CLK is divided by 4. If bit[1:0] = 01, CPU_CLK is divided by 2. IF bit[1:0] = 00, CPU_CLK output is always low.

This register is set to the default value at hardware reset. It is not affected by software reset.

7.2.8. Address 12: Preamble Search Threshold, write only, default = 00001000

	B7	B6	B5	B4	B3	B2	B1	B0
PSTH	0	0	0	0	1	0	0	0

The 4 least significant bits of this register defines the threshold value of the de-spreader in recognizing preamble symbol. Each acquired symbol has a signal strength value between 0 to 15. A preamble symbol must have signal strength above PSTH in order for it to be recognized.

PSTH is set to “1000” at hardware reset and it is not affected by software reset.

7.2.9. Address 13: Extra data, read and write, default = 00000000

	B7	B6	B5	B4	B3	B2	B1	B0
Extra Data	0	0	ED5	ED4	ED3	ED2	ED1	ED0

This register is used in data mode with parity disabled. It is the input and output port for transferring 6 extra bits of user data for each data mode sub-frame.

ED is set to “00 000000” at hardware reset or software reset.

7.2.10. Address 14: Signal Strength (SNR) Indicator, read only.

	B7	B6	B5	B4	B3	B2	B1	B0
SNR	MSB							LSB

This register is a relative measurement of native signal strength that is encoded with the same Color Code (“In band, native signal”). 0xFF indicates the strongest signal and 0x00 indicates the weakest signal. This register should be read at the end of each receive frame to determine the In band, native signal energy. For the normal L9002DX2 operation, a value of 0x5F is considered to be the strongest level.

When SNR is used in conjunction with the RSSI value from the RF module (which measures “In band RF energy”), a proper diversity decision can be made to space (antenna), frequency (RF hopping) changes for the best reception under a multipath dominant environment.

7.2.11. Address 15: Preamble Search & Lock Counter, write only, default: 00110111

	B7	B6	B5	B4	B3	B2	B1	B0
	PSL[3]	PSL[2]	PSL[1]	PSL[0]	DLL[3]	DLL[3]	DLL[1]	DLL[0]

This register contains the preamble symbol count during the Search and Locking phases. Preamble acquisition is divided into two stages. The first stage is completed when the number of preamble symbol equal to PSL is acquired. The second stage is completed when the number of preamble symbol equals to DLL is acquired. DLL must always be larger than PSL.

7.2.12. Address 16: Transmit data, write only.

	B7	B6	B5	B4	B3	B2	B1	B0

This register is the input port of the transmit data FIFO. One sub-frame worth of data must be first written into the FIFO through this port before starting transmission.

This register is not affected by reset but the transmit FIFO is cleared on hardware or software reset, and after the transmission of the empty burst frame.

7.2.13. Address 17: Receive data, read only.

	B7	B6	B5	B4	B3	B2	B1	B0

This register is the output port of the receive data FIFO. Data received by the L9002DX2 is deposited into the FIFO. They must be read by the system controller at each sub-frame interrupt.

This register is not affected by reset but the receive FIFO is cleared on hardware or software reset. When the FIFO under flow occurs the default output is the value stored at the Quietcode register.

7.2.14. Address 1E: Encryption register, write only, default: 00000000

	B7	B6	B5	B4	B3	B2	B1	B0
	0	0	0	0	0	0	0	0

This register contains the encryption key (seed vector) used for all transmit and receive data. Both the master and the slave must be programmed to the same value in order to communicate.

This register is set to the default value during hardware reset and is not affected by software reset.

7.2.15. Address 1F: Sticky count, write only, default: 00000011

	B7	B6	B5	B4	B3	B2	B1	B0
	0	0	0	0	0	0	1	1

The 4 least significant bits of this register determine the sticky count. The sticky count is the number of error data frame the device allows before it would attempt to re-establish communication link through the acquisition burst protocol. If the STKY bit of the CSR1 register is cleared, the sticky count register is ignored and the communication link must be re-established on every data frame error.

This register is set to the default value during hardware reset and it is not affected by software reset.

7.2.16. Address 20 – 23: PN code zero, write only, no default value.

	B7	B6	B5	B4	B3	B2	B1	B0
PN0	7	6	5	4	3	2	1	0
	15	14	13	12	11	10	9	8
	23	22	21	20	19	18	17	16
	31	30	29	28	27	26	25	24

This registers contain the PN sequence for symbol “000” and “111”. PN code registers are not affected by hardware or software reset.

7.2.17. Address 24 – 27: PN code one, write only, no default value.

	B7	B6	B5	B4	B3	B2	B1	B0
PN1	7	6	5	4	3	2	1	0
	15	14	13	12	11	10	9	8
	23	22	21	20	19	18	17	16
	31	30	29	28	27	26	25	24

This registers contain the PN sequence for symbol “001” and “110”. PN code registers are not affected by hardware or software reset.

7.2.18. Address 28 – 2B: PN code two, write only, no default value.

	B7	B6	B5	B4	B3	B2	B1	B0
PN3	7	6	5	4	3	2	1	0
	15	14	13	12	11	10	9	8

	23	22	21	20	19	18	17	16
	31	30	29	28	27	26	25	24

This registers contain the PN sequence for symbol “010” and “101”. PN code registers are not affected by hardware or software reset.

7.2.19. Address 2C – 2F: PN code three, write only, no default value.

	B7	B6	B5	B4	B3	B2	B1	B0
PN3	7	6	5	4	3	2	1	0
	15	14	13	12	11	10	9	8
	23	22	21	20	19	18	17	16
	31	30	29	28	27	26	25	24

This registers contain the PN sequence for symbol “011” and “100”. PN code registers are not affected by hardware or software reset.

7.2.20. Address 30 – 37: I/O expansion port A, write only.

Address 30 to 37 are the bit-wise address of bit 0 to 7 of I/O expansion port A. The data bit position of each bit in the AD bus is the same as if the bit is address through the byte wise-address, i.e. bit 7 is access through AD7 and bit 0 is through AD0.

7.2.21. Address 38 – 3F: I/O expansion port B, write only.

Bit-wise address of port B. Access method is the same as port A.

7.2.22. Address 40: I/O expansion port A, write only.

This is the byte-wise address of port A. When address 40 is written, all 7 bits of port A are updated at the same time. This port is not affected by hardware or software reset.

7.2.23. Address 41: I/O expansion port B, write only, default = 11111111

This is the byte-wise address of port B. When address 41 is written, all 7 bits of port B are updated at the same time. This port is set by hardware reset and is not affected by software reset.

7.2.24. Address 42: I/O expansion port C, read only.

Bit 7 to 0 of this register is mapped to the input port PC[7:0]. This port is not affected by hardware or software reset.

7.2.25. Address 43: I/O expansion port D, read and write, default = 11111111

Bit 7 to 0 of this register is mapped to the I/O port PD[7:0]. When this port is in output mode, write to this register sets the value of PD pins. When this port is in input mode, the value of PD pins are read from this location. This port is set by hardware reset and is not affected by software reset.

7.2.26. Address 44: I/O direction control of port D, write only, default = 11111111

Bit 1 (the second last bit) of this register is the I/O control of port D. When it is one, port D is an input port. When it is zero, port D is an output port and the PD pins are driven by the device. Other bits of this register are reserved. This register is set by hardware reset and it is not affected by software reset.

7.2.27. Address 46 and 47: General purpose timer, write only, default = 00000000

Register 46 and 47 together forms a 16-bit number, GPT_CNT. Register 47 is the upper byte and register 46 is the lower byte. GPT_CNT determines the cycle time of the GPT output pin in units of 2400 CLK_IN cycle time. If the device operates at 19.2MHz, GPT cycle time range from 125us to 8.192 second. GPT always have 50% duty cycle. When GPT_CNT is zero, the GPT output does not toggle. These registers are cleared by hardware reset and are not affected by software reset.

8. ELECTRICAL SPECIFICATIONS

8.1. Absolute Maximum Ratings

(Voltage Referenced to V_{SS} pin)

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	-0.3 to 4.30	V
Voltage to 5V Tolerant Pins (1)	---	-0.3 to 5.5	V
Voltage to Non-5V Tolerant Pins (1)	---	-0.3 to V_{CC} + 0.3	V
Operating Temperature	T_{OP}	0 to +85	^{o}C
Storage Temperature	T_{STG}	-40 to +125	^{o}C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

8.2. DC Characteristics

(V_{SS} = 0 volt T_{OP} = 0 to +85° C)

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V_{CC}	-----	2.7	3.0	3.6	V
Operating Current	I_{CC4}	CLK_IN = 19.200 MHz, Active Mode.	---	18	30	mA
Standby Current	I_{CC3}	CLK_IN = 19.200 MHz, Standby Mode. RESET=1. PA[7:0], PB[3:0] = 0. PD[7:0] = 0 or INPUT mode. PC[7:4]=1.	---	2	5	mA
Freeze Mode Current	I_{CC2}	CLK_IN = 19.200 MHz, Freeze Mode, CHIP_EN=0. PA[7:0], PB[3:0] = 0. PD[7:0] = 0 or INPUT mode. PC[7:4]=1.	---	1	2	mA
Sleep Mode Current	I_{CC1}	CLK_IN = 19.200 MHz, Sleep Mode, CLK_IN inactive, OSC_EN# = 1. PA[7:0], PB[3:0] = 0. PD[7:0] = 0 or INPUT mode. PC[7:4]=1.	---	0.1	0.5	mA
Input High Voltage	V_{IH}	All digital input pins	2.0	---	-----	V
Input Low Voltage	V_{IL}	All digital input pins	0	----	0.8	V

8.2. DC Characteristics, continued

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
Output High Voltage (2)	V_{OH1}	I_{OH} = -2mA	2.4	----	-----	V
Output Low Voltage (2)	V_{OL1}	I_{OL} = 2mA	0	---	0.4	V
Output High Voltage (2,3)	V_{OH2}	I_{OH} = -3mA	2.4	----	-----	V
Output Low Voltage (2)	V_{OL2}	I_{OL} = 2mA	0	---	0.4	V
Output High Voltage (2)	V_{OH3}	I_{OH} = -8mA	2.4	----	-----	V
Output Low Voltage (2)	V_{OL3}	I_{OL} = 8mA	0	---	0.4	V
Input Current, normal buffer	I_{I1}		-10	---	+10	uA
Input Current, buffer with pull-up	I_{I2}		-200	---	+10	uA
Input Current, buffer with pull-down	I_{I3}		-10	---	+200	uA
Tri-state leakage current	I_{OZ}		-10	---	+10	uA
Input Capacitance	C_{IN}	All digital input pins to V_{SS}	---	---	10	pF

Notes:

1. TX_DATA is not 5V tolerant.
2. V_{OL1}, V_{OH1} = BSYNC_OUT, CER#, COD_CLK, COD_SYNC, CPU_CLK, DR, ID_DET#, IRQ#, LOCK, PA, PD, PLLSW, RF_PWR, RLOCK, TX_ENV, WAKEUP
   V_{OL2}, V_{OH2} = AD, ANT_SW, CLK_OUT, GPT, PB
   V_{OL3}, V_{OH3} = TX_DATA
3. PB[7:4] are open-drain outputs.

8.3. AC Switching Characteristics

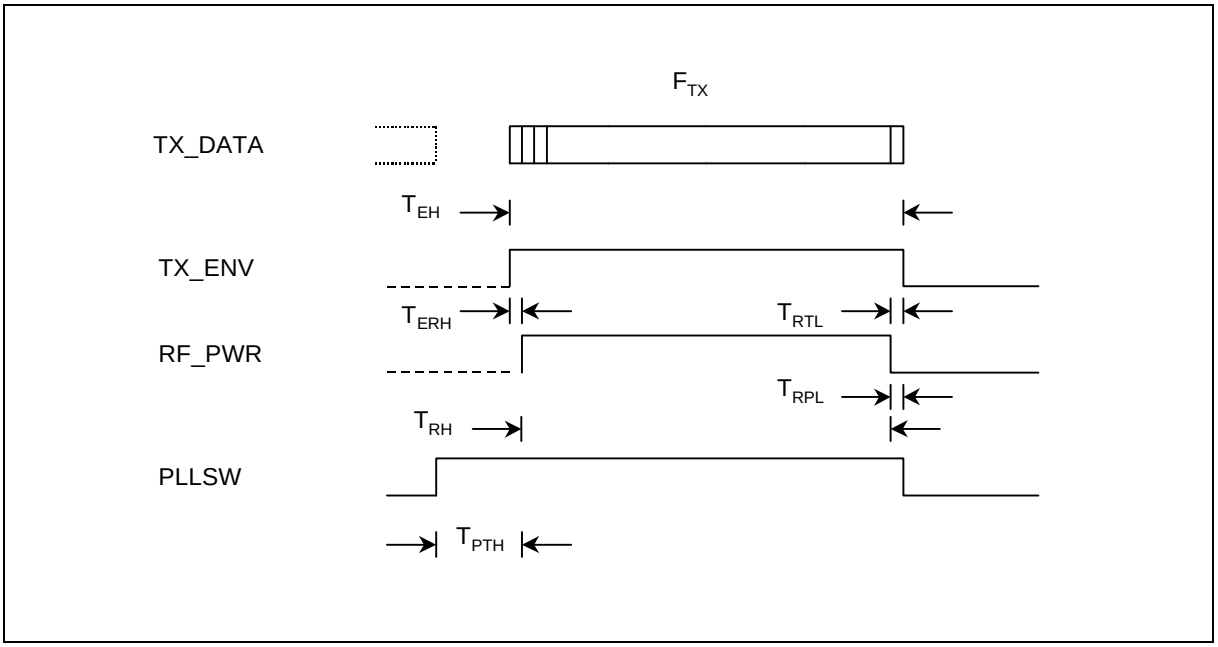
8.3.1. Characteristic of RF Module Interface Bus

(V_{EXT} = +2.7 to 3.3V ; Vss = 0V; all digital circuit referenced to V_{SS} ; T_{OP} = 0 to +85° C, C_L = 150 pF)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TX_ENV High Time	T_{EH}	(1)	---	2532	---	uS
TX_ENV High to RF_PWR High	T_{ERH}	(1)	---	4	---	uS
PLLSW High to TX_ENV High	T_{PTH}	(1)	---	470	---	uS
RF_PWR High Time	T_{RH}	(1)	---	2524	---	uS
RF_PWR Low to TX_ENV Low	T_{RTL}	(1)	---	4	---	uS
RF_PWR Low to PLLSW Low	T_{RTL}	(1)	---	4	---	uS
TX_DATA Rate	F_{TX}	(1)	---	1.365	---	Mbps

Note:

1. All RF timing values are linearly proportional to CLK_IN frequency. Value assumes master clock Mclk, or CLK_IN, at 19.200MHz



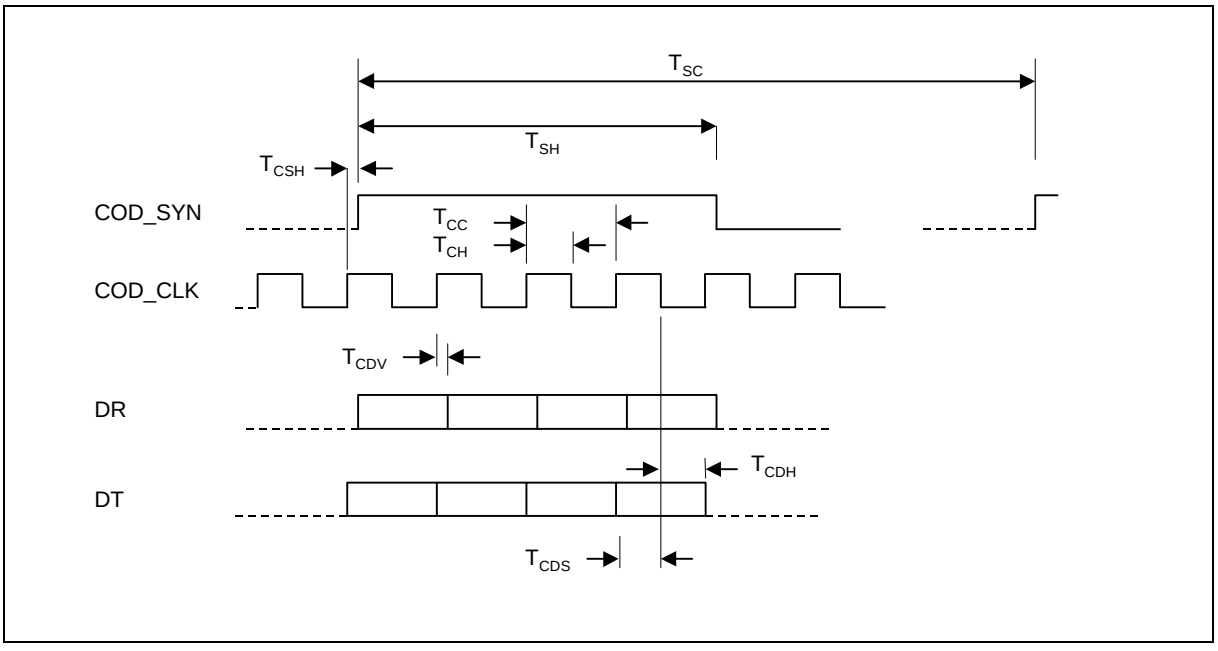
8.5.2. Characteristic of Codec Interface Bus

(V_{EXT} = +2.7 to 3.3V ; Vss = 0V; all digital circuit referenced to V_{SS} ; T_{OP} = 0 to +85° C, C_L = 150 pF)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CLK_IN Frequency (L9002DX2-20)	M_{CLK}		12.000	19.200	20.00	MHz
CLK_IN Frequency (L9002DX2-33)	M_{CLK}		12.000	32.768	33.00	MHz
CLK_IN Frequency (L9002DX2-40)	M_{CLK}		12.000	38.400	*TBD*	MHz
COD_SYNC High Time	T_{SH}	(2)	---	6.71	---	uS
COD_SYNC Cycle Time	T_{SC}	(2)	---	125	---	uS
COD_CLK High Time	T_{CH}	(2)	---	0.83	---	uS
COD_CLK Cycle Time	T_{CC}	(2)	---	1.67	---	uS
COD_CLK High to COD_SYNC High	T_{CSH}	(2)	---	0.05	---	uS
COD_CLK High to DR Valid	T_{CDV}		---	0.05	---	uS
DT to COD_CLK Low Setup Time	T_{CDS}		---	0.05	---	uS
DT to COD_CLK Low Hold Time	T_{CDH}		---	0.05	---	uS

Note:

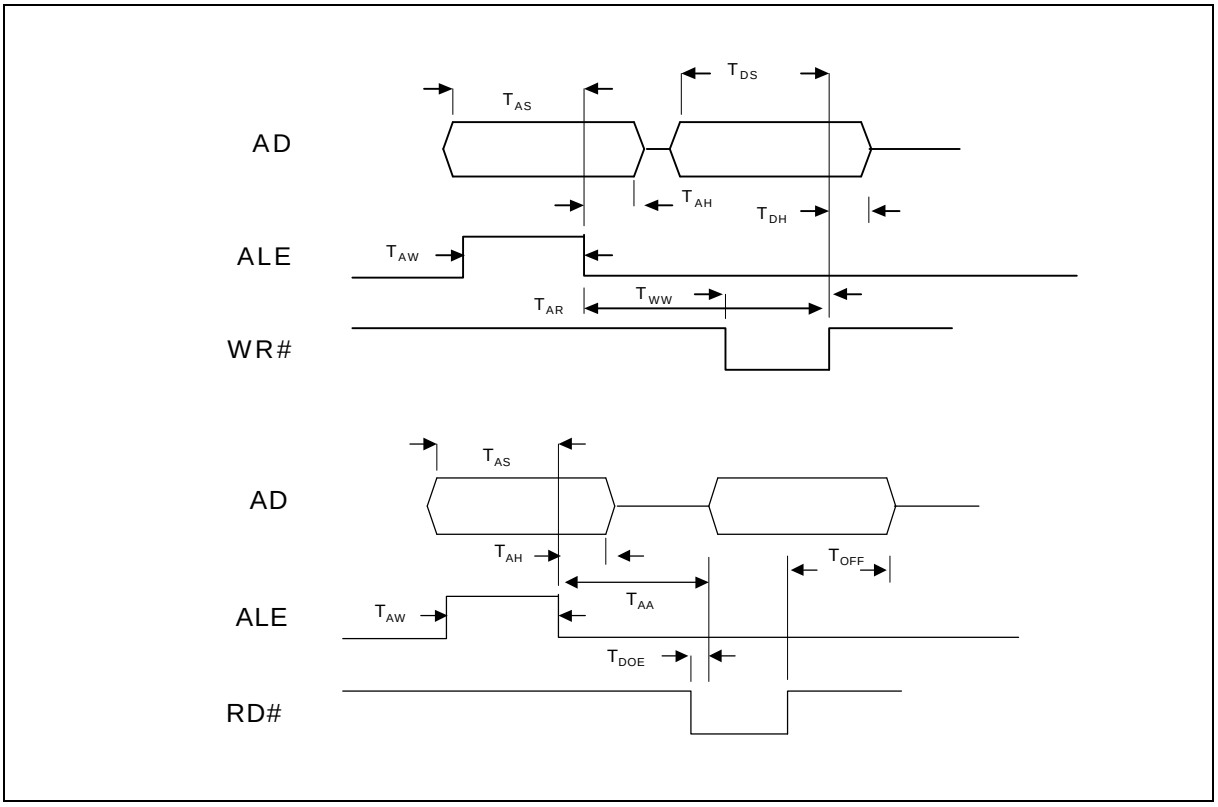
2. All Codec bus timing values are linearly proportional to CLK_IN frequency. Value assumes Mclk, or CLK_IN, at 19.200MHz



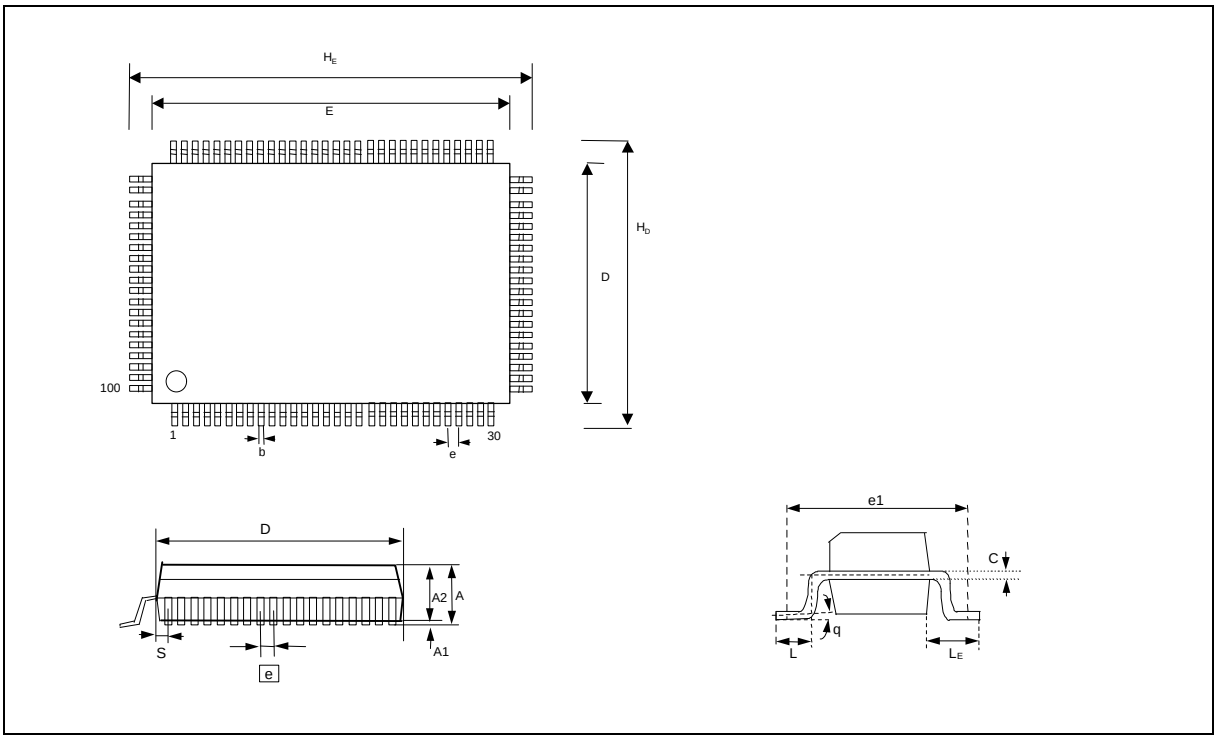
8.5.3. Characteristic of CPU Interface Bus

(V_{EXT} = +2.7 to 3.3V ; Vss = 0V; all digital circuit referenced to V_{SS} ; T_{OP} = 0 to +85° C, C_L = 150 pF)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Address to ALE Setup Time	T_{AS}		30			ns
Address to ALE Hold Time	T_{AH}		10			ns
Data to WR# Setup Time	T_{DS}		30			ns
Data to WR# Hold Time	T_{DH}		10			ns
RD# to Data Output Enable	T_{DOE}				20	ns
RD# to Data Output Disable	T_{OFF}				15	ns
ALE Pulse Width	T_{AW}		40			ns
WR# Pulse Width	T_{WW}		40			ns
ALE Low to Data Output valid	T_{AA}				45	ns
ALE Low to WR# High	T_{AR}		40			ns

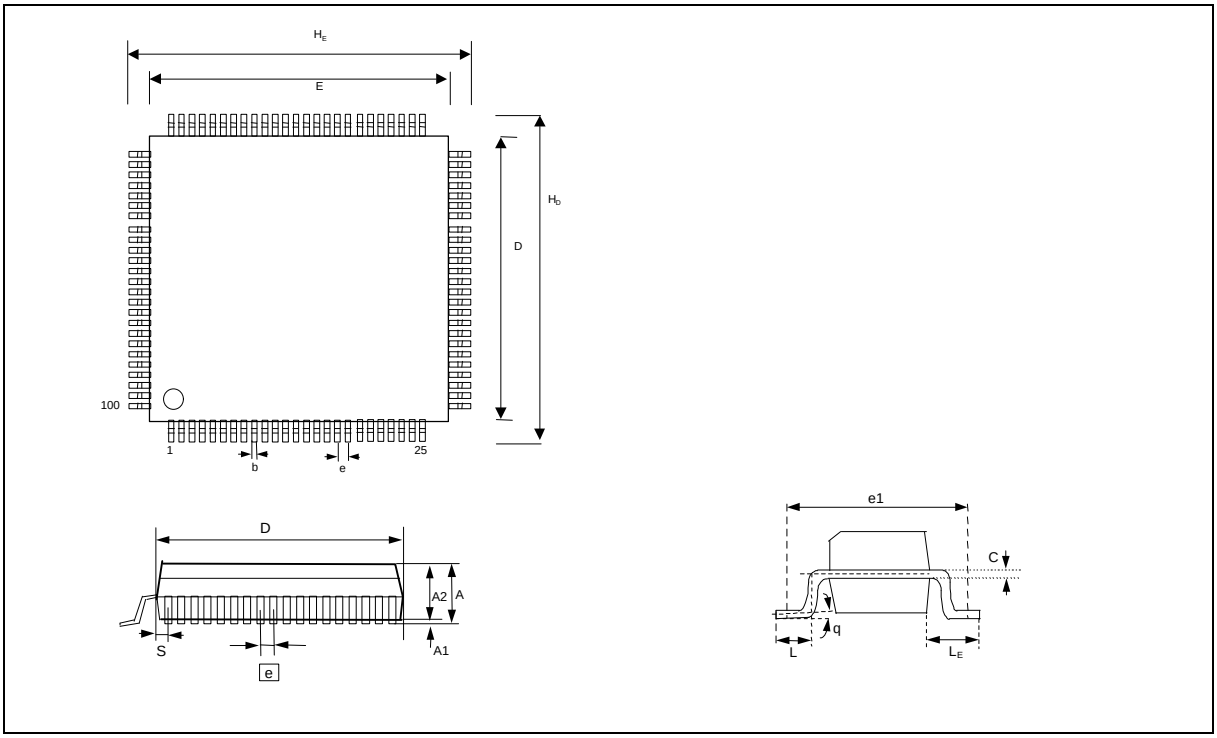


9. PACKAGE DIMENSION



100-pin Plastic PQFP Package

SYMBOL	DIMENSION IN INCH	DIMENSION IN MM
A	---	---
A1	0.014 ±0.004	0.35 ±0.10
A2	0.107 ±0.006	2.72 ±0.15
b	0.012 ±0.004	0.30 ±0.10
c	0.006 ±0.002	0.15 ±0.05
D	0.551 TYP. (0.555 Max.)	14.00 TYP. (14.10 Max.)
E	0.787 ±0.006	20.00 ±0.10
e	0.026 ±0.006	0.65 ±0.152
HD	0.677 ±0.008	17.20 ±0.20
HE	0.913 ±0.008	23.20 ±0.20
L	0.031 ±0.006	0.80 ±0.15
LE	0.063	1.60
S	---	---
θ	0–7 degree	0–7 degree



100-pin Plastic TQFP Package

SYMBOL	DIMENSION IN INCH	DIMENSION IN MM
A	---	1.2 (max)
A1	---	0 ~ 0.25
A2	---	1.0 ± 0.5
b	---	0.22 (+0.08, -0.07)
c	---	0.17 ± 0.05
D	---	14.0 ± 0.1
E	---	14.0 ± 0.1
e	---	0.5 (typical)
HD	---	16.0 ± 0.2
HE	---	16.0 ± 0.2
L	---	0.5 ± 0.2
LE	---	1.0 ± 0.2
S	---	1.0 (typical)
θ	---	0 ~ 10^{o} (degree)

Lanwave Technology Inc

Headquarter
20111 Stevens Creek Blvd., Suite 260,
Cupertino, California 95014.
U.S.A.
TEL: (408)-253-3883
FAX: (408)-253-6630
http://www.lanwave.com/

Please visit the Lanwave web site for the latest information and to contact our international sales representative near you:

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