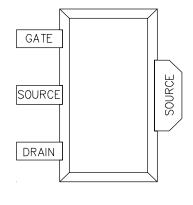
Solid State

LOW-NOISE, HIGH LINEARITY PACKAGED PHEMT

FEATURES

- +30 dBm Typical Power at 1800 MHz
- 15 dB Typical Power Gain at 1800 MHz
- 1.3 dB Typical Noise Figure
- +46 dBm Typical Intercept Point
- 50% Power-Added-Efficiency
- Color-coded by I_{DSS} range



TOP VIEW

DESCRIPTION AND APPLICATIONS

The LP3000SOT89 is a packaged Aluminum Gallium Arsenide / Indium Gallium Arsenide (AlGaAs/InGaAs) Pseudomorphic High Electron Mobility Transistor (PHEMT), utilizing an Electron-Beam direct-write 0.25 μm by 3000 μm Schottky barrier gate. The recessed "mushroom" gate structure minimizes parasitic gate-source and gate resistances. The epitaxial structure and processing have been optimized for reliable high-power applications. The LP3000 also features Si₃N₄ passivation and is available in a die form or in a flanged ceramic package (P100) for high-power applications. Packages are color-coded by the I_{DSS} range (see below).

Typical applications include PCS/Cellular low-voltage high-efficiency output amplifiers, and general purpose power amplifiers. Standard lot screening is patterned after MIL-STD-19500, JANC grade.

PERFORMANCE SPECIFICATIONS ($T_A = 25^{\circ}C$)

SYMBOLS	PARAMETERS		MIN	TYP	MAX	UNITS
I _{DSS}	Saturated Drain-Source Current	LP3000-SOT89 BLUE	800	860	924	
	$V_{DS} = +2V V_{GS} = 0V$	LP3000-SOT89 GREEN	925	975	1024	mA
		LP3000-SOT89 RED	1025	1060	1100	
P _{1dB}	P _{1dB} Output Power at 1dB Gain Compression					
	$V_{DS} = 5.0V, I_{DS} = 50\% I_{DSS}$	f = 1800 Mhz	29.0	30.0		dBm
G _{1dB}	Power Gain at 1dB Gain Compression					
	$V_{DS} = 5.0V, I_{DS} = 50\% I_{DSS}$	f = 1800 MHz	13.0	15.0		dB
η_{ADD}	Power-Added Efficiency (5V/50%)			50		%
NF	Noise Figure $V_{DS} = 5V$, $I_{DS} = 50\%$ I_{DSS} , $f = 1800$ MHz			1.3		dB
IP3	Output Intercept Point $V_{DS} = 5V$, $I_{DS} = 50\%$ I_{DSS} , $f = 1800$ MHz			46		dBm
I _{MAX}	Maximum Drain-Source Current	$V_{DS} = 2V V_{GS} = +1V$		925		mA
G _M	Transconductance	$V_{DS} = 2V V_{GS} = 0V$	300	400		mS
V _P	Pinch-Off Voltage	$V_{DS} = 2V I_{DS} = 5mA$	-0.25	-1.2	-2.0	V
I _{GSO}	Gate-Source Leakage Current	$V_{GS} = -3V$		10	100	μΑ
BV _{GS}	Gate-Source Breakdown Voltage	$I_{GS} = 8mA$	-10	-12		V
BV _{GD}	Gate-Drain Breakdown Voltage	$I_{GD} = 8mA$	-10	-13	_	V

DSS-021 WH

Phone: (408) 988-1845 **Internet:** http://www.Filtronicsolidstate.com **FAX:** (408) 970-9950

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ABSOLUTE MAXIMUM RATINGS (25°C)					
SYMBOL	PARAMETER	RATING ¹			
V_{DS}	Drain-Source Voltage	6V			
V_{GS}	Gate-Source Voltage	-4V			
I _{DS}	Drain-Source Current	I _{DSS}			
lg	Gate Current	100 mA			
P _{IN}	RF Input Power	1 W			
T _{CH}	Channel	175°C			
	Temperature				
T _{STG}	Storage Temperature	-65/175°C			
PT	Power Dissipation	4.0W ^{3,4}			

RECOMMENDED CONTINUOUS							
OPERATING LIMITS							
SYMBOL	PARAMETER	RATING ²					
V_{DS}	Drain-Source Voltage	5V					
V_{GS}	Gate-Source Voltage	-1V					
I _{DS}	Drain-Source Current	0.5 x I _{DSS}					
IG	Gate Current	30 mA					
P _{IN}	RF Input Power	0.75 W					
T _{CH}	Channel	150°C					
	Temperature						
T _{STG}	Storage Temperature	-20/50°C					
P _T	Power Dissipation	3.0 W ^{3,4}					
G_{XdB}	Gain Compression	8 dB					

NOTES:

- 1. Operating conditions that exceed the Absolute Maximum Ratings could result in permanent damage to the device.
- 2. Recommended Continuous Operating Limits should be observed for reliable device operation.
- 3. Power Dissipation defined as: $P_T = (P_{DC} + P_{IN}) P_{OUT}$, where: $P_{DC} = DC$ bias power, $P_{OUT} = RF$ output power, and P_{IN} = RF input power. *Note: Provide for adequate thermal heatsinking at large source lead.*
- 4. Power Dissipation to be de-rated as follows above 25°C:

Absolute Maximum:

 $P_T = 4.0W - (9mW/^{\circ}C) \times T_{HS}$

Recommended Continuous Operating: P_T = 3.0W - (9mW/°C) x T_{HS}

where T_{HS} = heatsink or ambient temperature.

5. Specifications subject to change without notice.

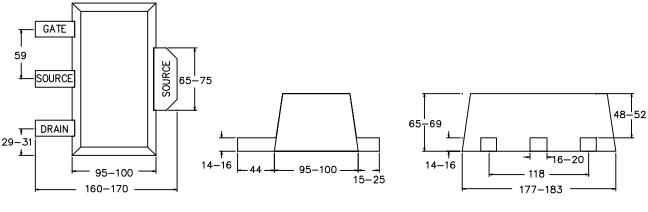
HANDLING PRECAUTIONS:

Care should be exercised during handling to avoid damage to the devices. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 1A (0-500V), and further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

APPLICATIONS NOTES AND DESIGN DATA:

Applications Notes are available from your local FSS Sales Representative, or directly from the factory. Complete design data, including S-parameters, Noise data, and Large-Signal models, is available on 3.5" diskette, or may be down-loaded from our Web Page.

PACKAGE OUTLINE: (dim. in mils; 1 mil = 0.001 in.)



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