AMERICAN MICROSYSTEMS, INC

LCD4401

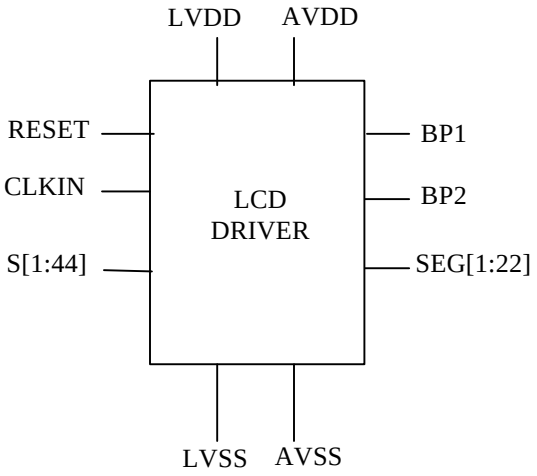
June, 1998 Preliminary

AMI 0.6 micron CMOS
C6L Double Poly

LCD Display Driver

Features

- 2 back planes
- 44 Segment
- 3 Voltage level



Description

LCD Driver cell produces 3 Voltage level signals (AVSS AVDD/2 AVDD) for the back planes (bp1,bp2) and 2 Voltage level signals (LVSS,LVDD) for the segment.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
AVDD	Analog Supply	Nominal 5V
AVSS	Analog Supply	Analog gnd
LVDD	Digital Supply	Nominal 5V
LVSS	Digital Supply	Digital gnd
RESET	Digital Input	Cell Reset
CLKIN	Digital Input	LCD Clock
S[1:44]	Digital Input	LCD Segment Select (S=1→Segment on)
BP1	Analog Output	LCD Back plane 1 Output
BP2	Analog Output	LCD Back plane 2 Output
SEG[1:22]	Digital Output	LCD Segment Output

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
AVDD	Analog Supply		4.5	5	5.5	V
LVDD	Digital Supply		4.5	5	5.5	V
T	Temperature		-40		85	C
Fs	LCD Clock Rate				10	KHz

Segment loads (50 pf,100meg)

Back plane loads (300pf)