Data Sheet
April 1998

microelectronics group

Lucent Technologies
Bell Labs Innovations

Comparator (CP-OpAmp)

Features

- Current programmable hysteresis (10 mV to 1 V)
- 6 mA current drive
- Less than 1 V head/floor room
- 150 V/µs slew rate
- 1.7 MΩ input impedance
- Low power (2.1 mA supply current)

Introduction

The primary advantage of comparators is their ability to switch states with small differences in input voltages. This is achieved by using high-gain, not necessarily stable, amplifiers with hysteresis, and output voltage clamping.

The primary disadvantage of the comparator is its size. Simple comparators can be made using basic op amps with positive feedback, but they do not have output voltage clamping or programmable hysteresis.

For applications that require flexibility, the comparator provides a basic topology for achieving this requirement.

Very often, the most cost-effective designs employ the simplest circuits (fewest devices) that meet the design specifications. The comparator has been chosen because of its simplicity. If its performance is satisfactory for a given application, it can be used as presented; if not, numerous suggestions have been included for improving the performance. These suggestions can be used as needed, albeit at a cost of requiring additional devices.

A comparator circuit, composed of an input stage, a feedback stage, an intermediate stage, an output stage, and output voltage clamps, is illustrated in Figure 1. The circuit takes advantage of the complementary nature of the CBIC process to achieve controlled and symmetrical behavior.

The comparator is intended to be biased with the voltage and current reference (VCR) circuit macrocell. If the resistors in the comparator are selected to be of the same type as those of the VCR, the voltages across the resistors* will be proportional to the bandgap voltage (VBG). The comparator may also be biased with an external current source.

Since transistors typically have higher gains at elevated temperatures, uniform performance over temperature is best achieved by biasing the transistors with negative temperature coefficient current sources. Using negative temperature coefficient current sources for biasing also helps ensure thermal stability† by lowering the dissipated power on the IC as the temperature increases.

In the following Description section, the dc, ac, and transient capabilities for the comparator are presented. The Performance Improvements section provides numerous ways to modify the comparator circuit to achieve improve performance. Further, this macrocell is fabricated using the Lucent Technologies Microelectronics Group ALA110 CBIC-V2 linear array for evaluation.

* Since devices of the same type usually match each other within 1%, while absolute values vary by more than 20% in most integrated-circuit fabrication processes, it is most often advantageous to utilize circuits where accuracy is controlled by device matching rather than by the absolute value of the devices.

† This is especially important since most SPICE class circuit simulators cannot simulate thermal stability.

Description

An elementary comparator circuit is illustrated in Figure 1. The circuit is composed of five parts: a differential input stage, a positive feedback stage that generates the hysteresis, an intermediate differential stage, a low output impedance unity gain driving buffer stage, and output high- and low-voltage clamps.

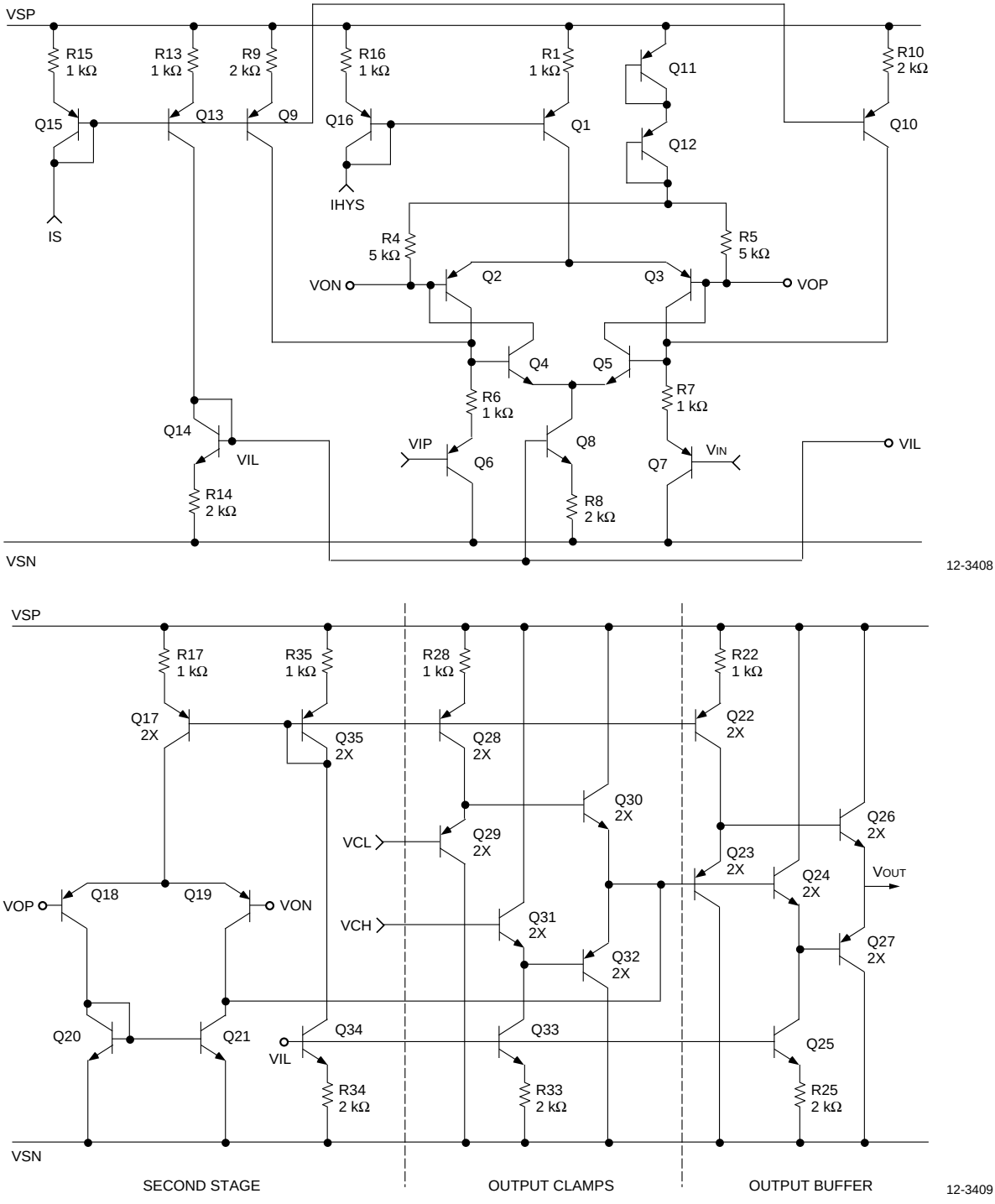

Figure 1. Comparator (CP-OpAmp) Schematic

Description (continued)

Differential Input Stage

The differential input stage is composed of transistors Q4 and Q5, which are biased by the current (I8) of transistor Q8. Assuming VBE6 = VBE7, the difference current I4 – I5 is:

$$I4 - I5 = I8 \times \tanh\frac{VIP + VR6 - (VIN - VR7)}{2 \times VT + R \times I8}$$

where VR6 = R6 (I9 + I2) and VR7 = R7 (I10 + I3).

Due to the nature of the positive feedback in the comparator circuit, the currents I2 and I3 are:

(I2, I3) = (0, I1) or (I2, I3) = (I1, 0)

resulting in hysteresis of 2 x I1 x R6 for R6 = R7.

The output of the input stage is VOP and VON. These voltages drive the feedback input stage Q2 and Q3, and the intermediate stage Q18 and Q19.

Intermediate Current Difference and Output Voltage Clamps Stage

The second stage is composed of the emitters of Q18 and Q19 as inputs, Q20 and Q21 form a current mirror for the positive current, and the collector currents of Q17 bias the stage. The current at the VSUM node is either I17 or –I17, depending on the state of the comparator. If the VSUM current is +I17, then the VSUM voltage clamps at VCH with I17 flowing into the emitter of Q32. If the VSUM current is –I17, then the VSUM voltage clamps at the VCL with –I17 flowing into the emitter of Q30.

Simulated Performance

dc Transfer Characteristics

Figure 2 illustrates the dc characteristics of the comparator where ΔV_{IN} = VIP – V_{IN}. The hysteresis is illustrated for two settings, 200 μA and 400 μA. For the 400 μA setting, the output voltage is clamped at ±0.5 V. For the 200 μA setting, the output voltage is clamped at ±1 V.

For an ideal comparator, VSUM would be at 0 V if VIP – V_{IN} = 0. Because of the impedance, nonideal devices, and device mismatch, VIP – V_{IN} usually requires to be offset for VSUM to equal V (i.e., offset voltage).

The rate at which VSUM varies during operation depends on the size of the differential current applied to the VSUM node. The maximum rate at which VSUM can vary (slew rate) is limited by the collector current of Q17 and the parasitic capacitance associated with the VSUM node.

A Low Output Impedance Unity Gain Driving Stage

The function of the comparator (i.e., differential input voltage to clamp output voltage) is essentially complete at the VSUM node. Since, in most applications, it is necessary to drive small impedances, a low output impedance driver output buffer is usually required.

The driver/output buffer stage presented in Figure 1 has a wide bandwidth (approximately the unity gain, Ft, of the transistors), an output-to-input impedance reduction of βnpn x βpnp, an output voltage swing to within 1 V of both voltage supply rails, and a current-drive capability of I22 x βnpn or I25 x βpnp.

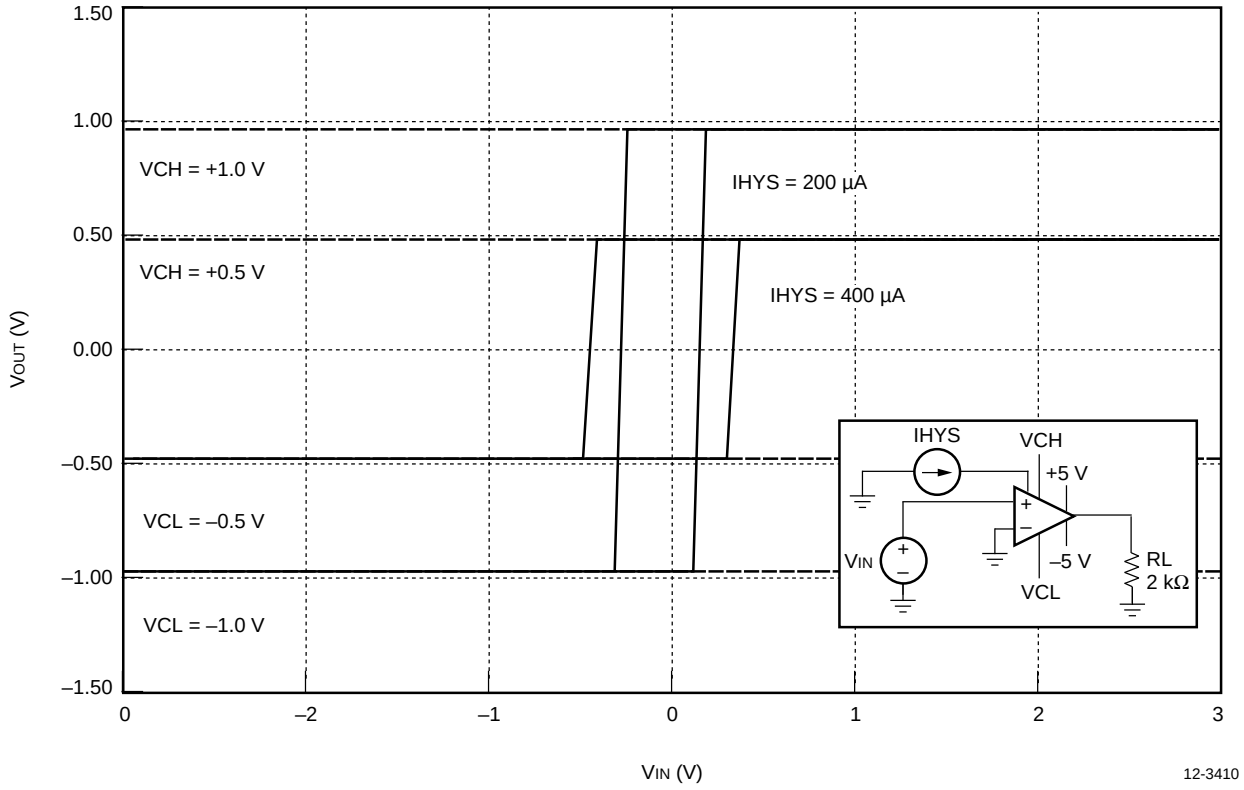

Figure 2. Simulated dc Transfer Characteristic for the CP-OpAmp

Simulated Performance (continued)

Slew Rate Limit

The slew rate limit is illustrated in Figure 3. A ±3 V 100 kHz input waveform is applied to the comparator for hysteresis settings of 200 µA and 400 µA. The output voltage is clamped at ±1 V and at ±0.5 V, respectively. The hysteresis can be seen as a delay after the zero crossing. The 400 µA hysteresis is approximately twice as long as the 200 µA hysteresis.

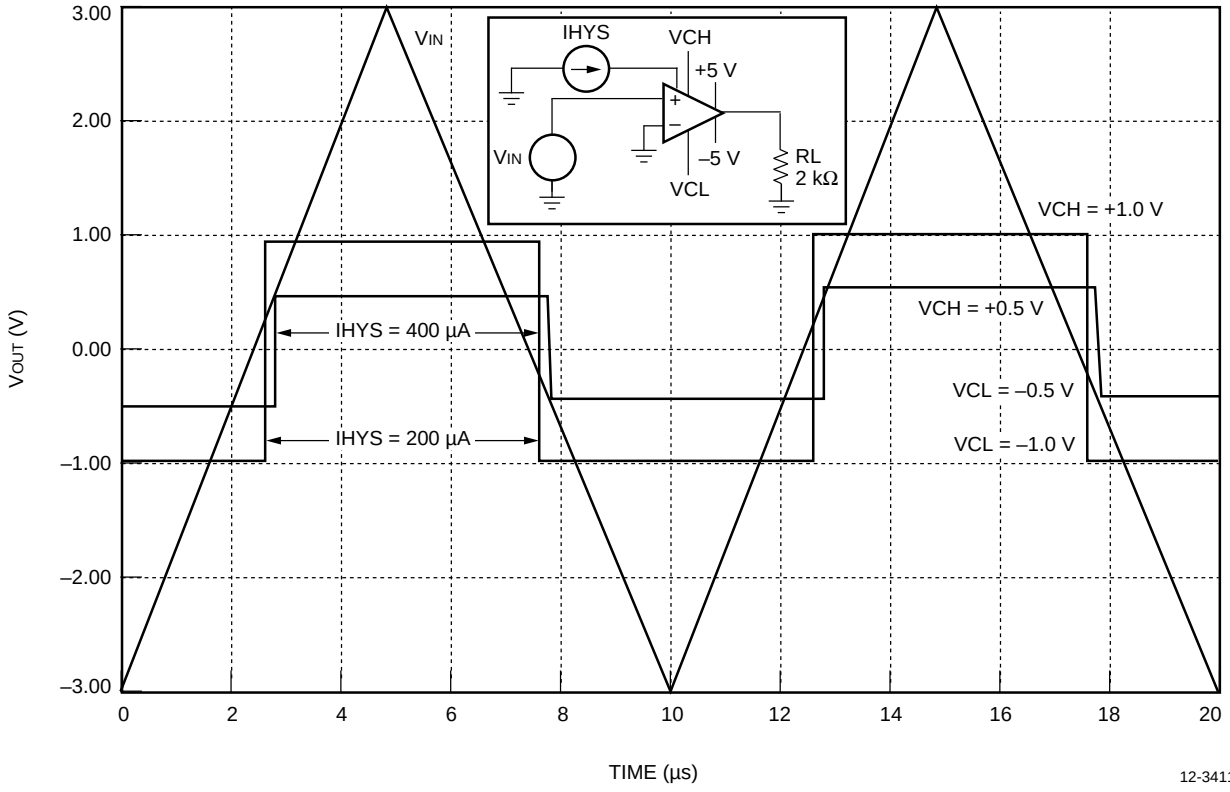

Figure 3. Simulated Transient Response of the CP-OpAmp Illustrating the Slew Rate Limit

Simulated Performance (continued)

Input Impedance

The input impedance as a function of frequency of the comparator is illustrated in Figure 4. The input impedance is over 1 MΩ to 1 MHz, and then drops off at 20 dB per decade, reaching 1 kΩ at 1 GHz.

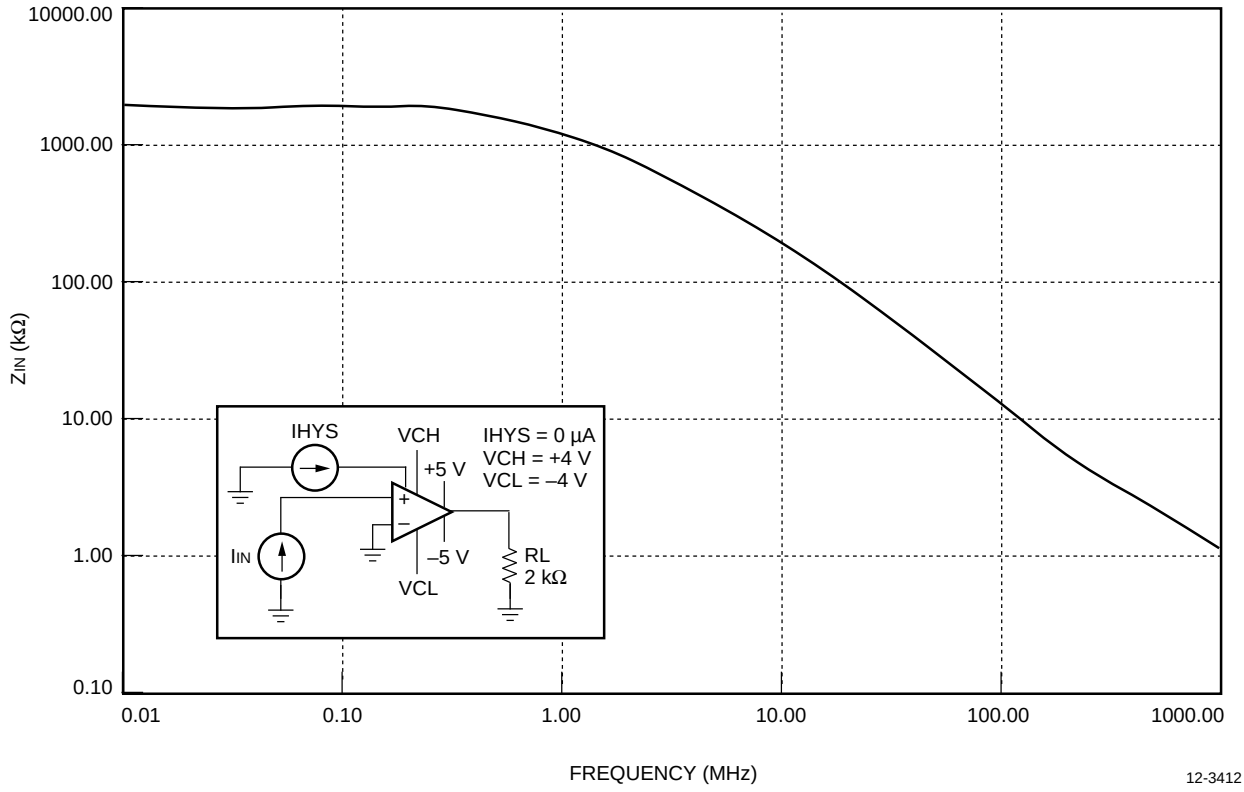

Figure 4. Simulated Input Impedance for the CP-OpAmp

Performance Improvements

Power

The dc power dissipation is related to the dc bias current plus the drive current, times the voltage drop across the IC. The ac power consumption is the power consumption plus the RMS power on the IC. The biasing current is set by the biasing circuits in the VCR macrocell. The VCR cell has been designed to compensate for process and temperature variations. The temperature variation is minimized by the use of a bandgap reference circuit, and the process variation is minimized by avoiding tolerances that depend on absolute device values.

Varying the value of the biasing current in the comparator changes the dc power proportionally. Changing the biasing current affects the slew rate and the current-drive capability.

dc Gain

The dc gain is controlled by I8, R4 and R5, and I17R and the impedance at the VSUM node. Hence, increasing I8 and/or I17, and/or R4 & R5, and/or increasing the impedance at the VSUM node will increase the dc gain.

Slew Rate

The slew rate is controlled by the difference current and the parasitic capacitance at the VSUM node. Increasing the current of I17 increases the slew rate. If the output voltage does not keep up with VSUM, then the slew rate is limited by I22 and/or I25.

Input Impedance

The input impedance can be increased by lowering the biasing current. An alternative to increasing the input impedance is to use an input-biasing current-cancellation circuit.

Current Drive

The output current drive can be increased by increasing the biasing current. This will also increase the dissipated power. An alternative is to use Darlingtons in the output stage. This will provide an extra stage of current gain, but will reduce the head room by one VBE.

Electrical Characteristics

Conditions: T_J = 25 °C, R_L = 2 kΩ, VSP = +5 V, VSN = –5 V.

Table 1. dc Characteristics

Name	Conditions	Typical Value	Unit
Voltage Supply Range	—	±1 to ±5	V
Supply Current Draw	V_{IN} = 1.24 mV	2.1	mA

Table 2. dc Performance

Name	Conditions	Typical Value	Unit
Input Bias Current	V_{IN} = 1.24 mV	1.7	µA
Input Impedance	V_{IN} = 1.24 mV	2	MΩ
Input Offset Voltage	—	1.24	mV
Output Voltage Swing (head/floor room)	VSP – V_{OUT}, V_{OUT} – VSN	1, 1	mV
Common-mode Range (head/floor room)	VSP – V_{IN}, V_{IN} – VSN	1, 1	mV
Hysteresis Range	IHYS = 0 µA to 400 µA	1 to 400	±mV
Clamp Range with Respect to Supplies	VSP – VCH, VCL – VSN	1, 1	V
Output Current Drive	—	6	mA

Table 3. Dynamic Performance

Name	Conditions	Typical Value	Unit
Slew Rate	Unity Gain	150	V/µs

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April 1998
DS97-015BPF