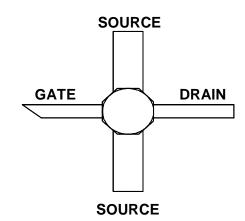
Solid State

PACKAGED LOW NOISE PHEMT

FEATURES

- 0.7 dB Typical Noise Figure at 12 GHz
- 12 dB Typical Associated Gain at 12 GHz
- 0.6 / 14 dB Typical NF/G_A at 2 GHz
- Low DC Power Consumption
- Color-Coded by I_{DSS} range



DESCRIPTION AND APPLICATIONS

The LPS200-P70 is a packaged Aluminum Gallium Arsenide / Indium Gallium Arsenide (AlGaAs/InGaAs) Pseudomorphic High Electron Mobility Transistor (PHEMT), utilizing an Electron-Beam direct-write 0.25 μ m by 200 μ m Schottky barrier gate. The recessed "mushroom" Ti/Pt/Au gate structure minimizes parasitic gate-source and gate resistances. The epitaxial structure and processing have been optimized for high dynamic range. The LPS200's active areas are passivated with Si₃N₄, and the P70 ceramic package is ideal for low-cost, high-performance applications that require a surface-mount package. Packages are color-coded by I_{DSS} range.

Typical applications include low noise receiver preamplifiers for commercial applications including Cellular/PCS systems, broad bandwidth commercial instrumentation, and commercial Space applications.

The LPS200 wafer lot screening is patterned after MIL-STD-19500, JANC grade.

PERFORMANCE SPECIFICATIONS ($T_A = 25^{\circ}C$)

SYMBOLS	PARAMETERS		MIN	TYP	MAX	UNITS
I _{DSS}	Saturated Drain-Source Current LPS	S200-P70-1 BLUE	15	25	30	mA
	$V_{DS} = 2V V_{GS} = 0V$ LPS	S200-P70-2 RED	31	40	50	mA
NF_{MIN}	Minimum Noise Figure					
	$V_{DS} = 2V$, $I_{DS} = 25\% I_{DSS} f = 12 \text{ GHz}$			0.7	1.3	dB
G_{A}	Associated Gain at Minimum Noise Figure					
	$V_{DS} = 2V$, $I_{DS} = 25\% I_{DSS} f = 12 \text{ GHz}$		10.5	12.0		dB
G_M	Transconductance	$V_{DS} = 2V V_{GS} = 0V$	60	90		mS
V _P	Pinch-Off Voltage	$V_{DS} = 2V I_{DS} = 1mA$	-0.25	-0.8	-1.5	V
I _{GSO}	Gate-Source Leakage Current	$V_{GS} = -3V$		1	15	μΑ

DSS-043 WA

Phone: (408) 988-1845 **Internet:** http://www.Filtronicsolidstate.com **FAX:** (408) 970-9950

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PACKAGED LOW NOISE PHEM

ABSOLUTE MAXIMUM RATINGS (25°C)						
SYMBOL	PARAMETER	RATING ¹				
V _{DS}	Drain-Source Voltage	4V				
V _{GS}	Gate-Source Voltage	-2V				
I _{DS}	Drain-Source Current	I _{DSS}				
I _G	Gate Current	5 mA				
P _{IN}	RF Input Power	50 mW				
Тсн	Channel Temperature	175°C				
T _{STG}	Storage Temperature	-65/175°C				
P _T	Power Dissipation	300mW ^{3,4}				

RECOMMENDED CONTINUOUS OPERATING LIMITS						
SYMBOL	PARAMETER	RATING ²				
V _{DS}	Drain-Source Voltage	3V				
V _{GS}	Gate-Source Voltage	-0.6V				
I _{DS}	Drain-Source Current	0.50 x I _{DSS}				
I _G	Gate Current	2 mA				
P _{IN}	RF Input Power	25 mW				
T _{CH}	Channel Temperature	150°C				
T _{STG}	Storage Temperature	-20/50°C				
P _T	Power Dissipation	225 mW ^{3,4}				
G_{XdB}	Gain Compression	4 dB				

NOTES:

- 1. Operating conditions that exceed the Absolute Maximum Ratings could result in permanent damage to the device.
- 2. Recommended Continuous Operating Limits should be observed for reliable device operation.
- 3. Power Dissipation defined as: $P_T = (P_{DC} + P_{IN}) P_{OUT}$, where: $P_{DC} = DC$ bias power, $P_{OUT} = RF$ output power, and $P_{IN} = RF$ input power.
- 4. Power Dissipation to be de-rated as follows above 25°C:

Absolute Maximum:

 $P_T = 300 \text{mW} - (3.5 \text{mW/}^{\circ}\text{C}) \times T_{HS}$

Recommended Continuous Operating: P_T = 225mW - (3.8mW/°C) x T_{HS}

where T_{HS} = heatsink or ambient temperature.

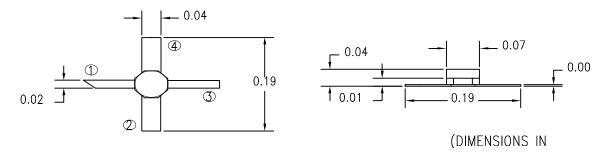
HANDLING PRECAUTIONS:

Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 1A (0-500V), and further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

PACKAGE CHARACTERISTICS:

The P70 package is available with a standard gold over nickel finish. The package lids are epoxy sealed and are capable of passing MIL-STD hermeticity (Gross Leak).

PACKAGE OUTLINE:



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