Advance Data Sheet
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microelectronics group

Lucent Technologies
Bell Labs Innovations

LU3X32FT Two-Port 3 V 10/100 Ethernet Transceiver TX/FX

Note: For sustaining support only, not for new designs.

Overview

The LU3X32FT is a fully integrated two-port 10 Mbits/s/100 Mbits/s physical layer device with transceiver. This part was designed for 10 Mbits/s/ 100 Mbits/s applications where board space, cost, and power are at a premium and stringent functional interoperability is a necessity. Operating at 3.3 V, the LU3X32FT is a powerful device for the forward migration of legacy 10 Mbits/s products and noncompliant 100 Mbits/s devices. The LU3X32FT was designed from the beginning to conform fully with all pertinent specifications, from the ISO/IEC 11801 and EIA/TIA 568 cabling guidelines to ANSI X3.263 TP-PMD to *IEEE** 802.3 ethernet specifications.

Features

- Single-chip integrated two-port physical layer and transceiver for 10Base-T and/or 100Base-T functions
- *IEEE* 802.3 compatible 10Base-T and 100Base-T physical layer interface and ANSI X3.263 TP-PMD compatible transceiver
- PECL interface for external FX transceiver
- Built-in analog 10 Mbits/s receive filter, removing the need for external filters
- Built-in 10 Mbits/s transmit filter
- 10 Mbits/s PLL exceeding tolerances for both preamble and data jitter
- 100 Mbits/s PLL, combined with the digital adaptive equalizer, robustly handles variations in rise-fall time, excessive attenuation due to channel loss, duty-cycle distortion, crosstalk, and baseline wander
- Transmit rise-fall time manipulated to provide lower emissions, amplitude fully compatible for proper interoperability
- Programmable scrambler seed for better FCC compliancy
- Selectable CIM, Class II support, and powerful MII drivers for repeater applications
- *IEEE* 802.3U clause 28 compliant autonegotiation for full 10 Mbits/s and 100 Mbits/s control
- Fully configurable via pins and management accesses
- PHY MIB support
- Symbol mode option
- Low-power –300 mA max
- Low autonegotiation power –30 mA/port
- Very low powerdown mode <5 mA/port
- 128-pin TQFP package

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Description

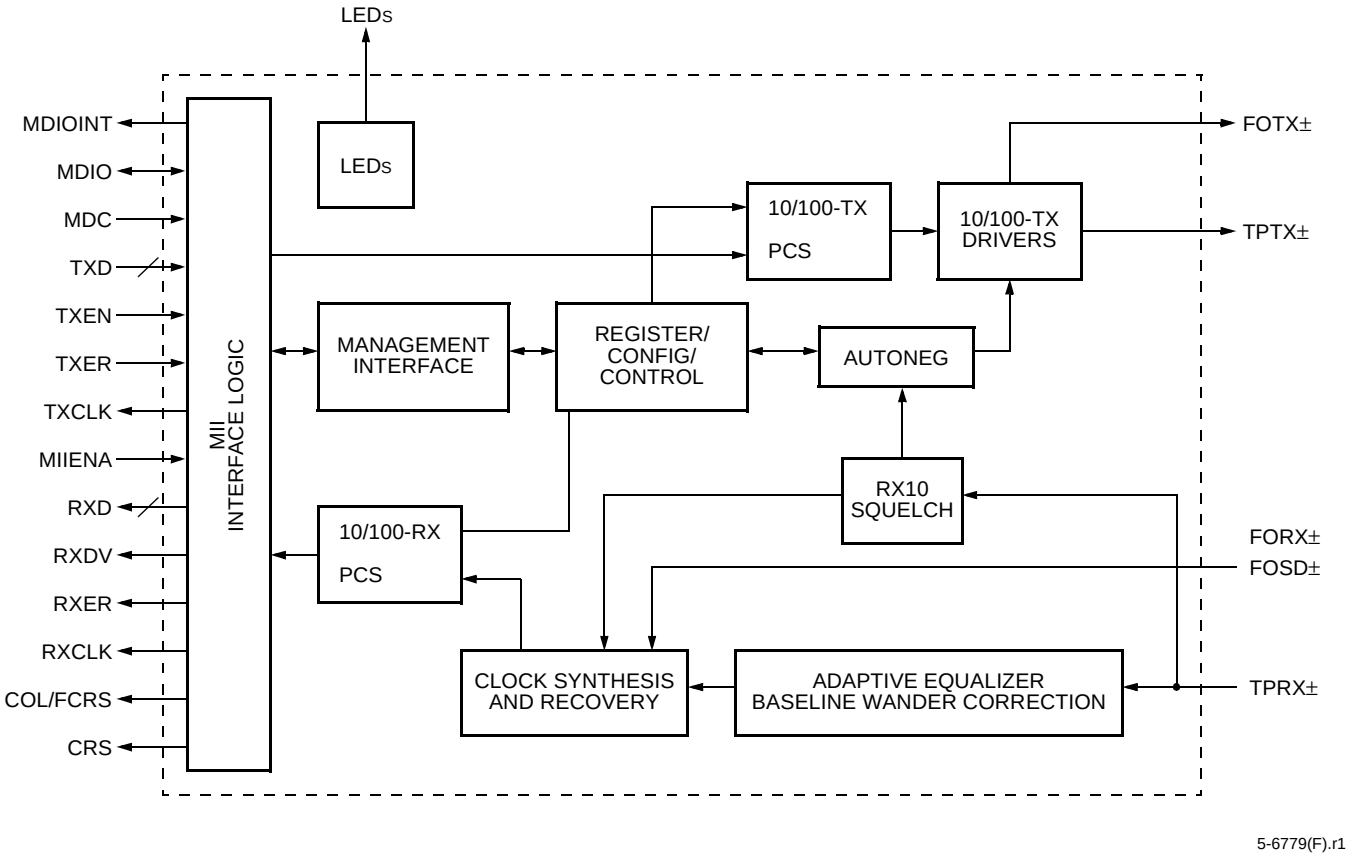

Figure 1. LU3X32FT Block Diagram (Per Port)

Pin Information

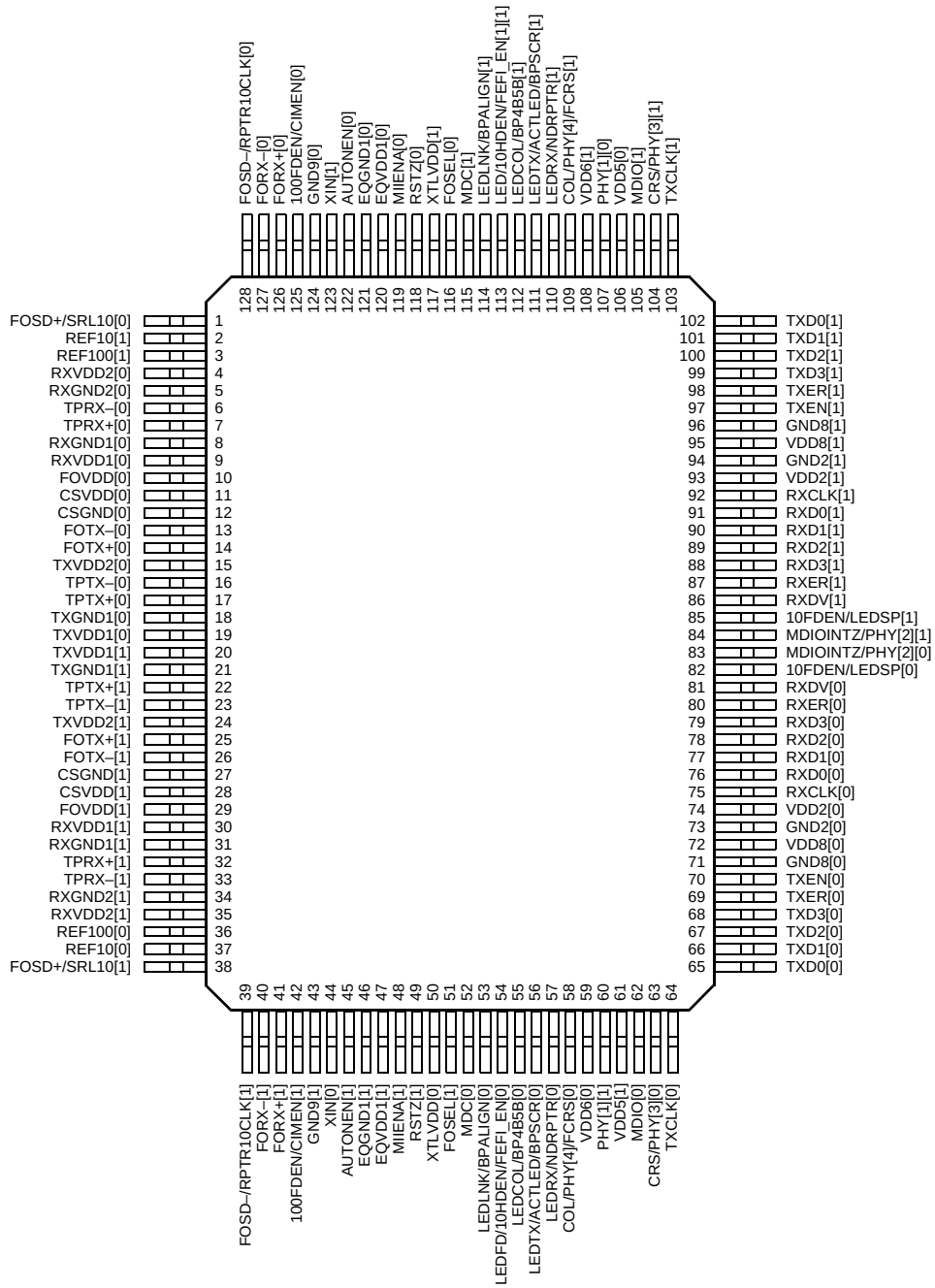

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Figure 2. Pin Diagram

Pin Descriptions

Table 1. Twisted-Pair Magnetic Interface

Pin No.	Pin Name	I/O	Pin Description
22, 17 23, 16	TPTX+[1:0] TPTX–[1:0]	O	**Twisted-Pair Transmit Driver Pairs**. These pins are used to send 100Base-T MLT-3 signals or 10Base-T Manchester signals across UTP cable.
32, 7 33, 6	TPRX+[1:0] TPRX–[1:0]	I	**Twisted-Pair Receive Pair**. These pins receive 100Base-T MLT-3 data or 10Base-T Manchester data from the UTP cable.

Table 2. Fiber-Optic Transceiver Interface

Pin No.	Pin Name	I/O	Pin Description
25, 14 26, 13	FOTX+[1:0] FOTX–[1:0]	O	**Fiber-Optic Transmit Driver Pair**. These pins are used to transmit differential PECL level NRZI data to a fiber-optic transceiver.
41, 126 40, 127	FORX+[1:0] FORX–[1:0]	I	**Fiber-Optic Receive Pair**. These pins are used to receive differential PECL level NRZI data from a fiber-optic transceiver.
38, 1 39, 128	FOSD+/SRL10[1:0] FOSD–/ RPTR10CLK[1:0]	I	**Fiber-Optic Signal Detect Differential Input Pair**. While operating in fiber mode, these pins are used to detect whether or not the fiber-optic receive pairs are receiving valid signal levels. See Table 8 for SRL10 and RPTR10CLK desscriptions. If fiber and serial 10 modes are not being used, tie all these pins low.

Note: Many of these signals are dual-function pins. During reset, these pins may be pulled up or down (as shown in Figure 5) to configure various options. The secondary function is shown in smaller print and described in Table 8.

Table 3. Twisted-Pair Transceiver Control

Pin No.	Pin Name	I/O	Pin Description
36, 3	REF100[1:0]	I	**Reference Pin for 100 Mbits/s Twisted-Pair Driver**. The value of the connected resistor is 301 Ω.
37, 2	REF10[1:0]	I	**Reference Pin for 10 Mbits/s Twisted-Pair Driver**. The value of the connected resistor is 4.64 kΩ.

Table 4. MII Interface

Pin No.	Pin Name	I/O	Pin Description
86, 81	RXDV[1:0]	O	**Receive Data Valid**.
87, 80	RXER[1:0]	O	**Receive Error**.
88, 79	RXD3[1:0]	O	**Receive Data[3]**.
89, 78	RXD2[1:0]	O	**Receive Data[2]**.
90, 77	RXD1[1:0]	O	**Receive Data[1]**.
91, 76	RXD0[1:0]	O	**Receive Data[0]**.
92, 75	RXCLK[1:0]	O	**Receive Clock**.
97, 70	TXEN[1:0]	I	**Transmit Enable**.
98, 69	TXER[1:0]	I	**Transmit Error**.
99, 68	TXD3[1:0]	I	**Transmit Data[3]**.

Pin Descriptions (continued)

Table 4. MII Interface (continued)

Pin No.	Pin Name	I/O	Pin Description
100, 67	TXD2[1:0]	I	**Transmit Data[2]**.
101, 66	TXD1[1:0]	I	**Transmit Data[1]**.
102, 65	TXD0[1:0]	I	**Transmit Data[0]**.
103, 64	TXCLK[1:0]	O	**Transmit Clock**. This pin outputs during node mode only. For 100 Mbits/s repeater mode, all transmit related MII signals should be synchronized to 25 MHz clock on XIN pin. See Table 8 for 10 Mbits/s repeater mode clocking.
104, 63	CRS/PHY[3][1:0]	I/O	**Carrier Sense/PHY Address [3]**. This output pin indicates the carrier sense condition. It is only active on receive while in repeater mode. See Table 5 for PHY[3] description.
109, 58	COL/FCRS/PHY[4] [1:0]	I/O	**Collision/False Carrier Sense**. This output pin indicates collision condition in node operation and indicates false carrier sense condition in repeater mode. This output is squelch jabber in 10 Mbits/s mode. See Table 5 for PHY[4] description.
105, 62	MDIO[1:0]	I/O	**Management Data I/O**.
115, 52	MDC[1:0]	I	**Management Data Clock**.
119, 48	MIIENA[1:0]	I	**MII Enable**. A logic 0 on this pin tri-states all RX interface signals of MII. This pin is intended to be used by the repeater controller to selectively enable one of the PHYs in the system. For node applications, this pin is ignored.
84, 83	MDIOINTZ/PHY[2][1:0]	I/O	**MDIO Interrupt (Active-Low)**. The MDIO interrupt pin outputs a logic 0 pulse of 40 ns, synchronous to XIN, whenever an unmasked interrupt condition is detected. Refer to management registers 1Dh and 1Eh for interrupt conditions. See Table 5 for PHY[2] description.

Note: Many of these signals are dual-function pins. During reset, these pins may be pulled up or down (as shown in Figure 5) to configure various options. The secondary function is shown in smaller print and described in Table 5.

Table 5. PHY Address Configuration

Pin No.	Pin Name	I/O	Pin Description
	PHY[0]		**PHY Address [4:1]**. These 8 pins are detected during powerup or reset to initialize the PHY address used for MII management register interface. PHY address 00h forces the PHY into MII isolate mode. PHY address pins [4:2] have an internal 40 kΩ pull-down. PHY address [0] is forced to 0 for port 0, and 1 for port 1. See Table 4 for MDIOINTZ, CRS, COL, and FCRS descriptions.
107, 60	PHY[1][1:0]	I	
84, 83	PHY[2]/MDIOINTZ[1:0]	I/O	
104, 63	PHY[3]/CRS[1:0]	I/O	
109, 58	PHY[4]/COL/FCRS[1:0]	I/O	

Pin Descriptions (continued)

Table 6. 100 Base-X PCS Configuration

Pin No.	Pin Name	I/O	Pin Description
111, 56	BPSCR/LEDTX/ ACTLED[1:0]	I/O	**Bypass Scrambler Mode (Ports 1, 0)**. A high value on this pin during powerup or reset will bypass the scramble/descramble operations in the 100Base-X data path. This pin has an internal 40 kΩ pull-down. In fiber mode, this pin should be pulled high. See Table 9 for LEDTX and ACTLED description.
114, 53	BPALIGN/LEDLNK[1:0]	I/O	**Bypass Alignment Mode (Ports 1, 0)**. A high value on this pin during powerup or reset will bypass the alignment feature of the PHY. This bypass mode provides a symbol interface. This pin has an internal 40 kΩ pull-down. See Table 9 for LEDLNK description.
112, 55	BP4B5B/LEDCOL[1:0]	I/O	**Bypass 4B5B Mode.** A high value on this pin during powerup or reset will bypass the 4B/5B encoder of the PHY. This pin has an internal 40 kΩ pull-down. See Table 9 for LEDCOL description.

Note: Many of these signals are dual-function pins. During reset, these pins may be pulled up or down (as shown in Figure 5) to configure various options. The secondary function is shown in smaller print and described in Table 9.

Table 7. Autonegotiation Configuration

Pin No.	Pin Name	I/O	Pin Description
122, 45	AUTONEN[1:0]	I	**Autonegotiation Enable (Ports 1, 0)**. A high value on these pins during powerup or reset will enable autonegotiation, a low value will disable it.
125, 42	100FDEN/CIMEN[1:0]	I	**100 Full-Duplex Enable (Ports 1, 0)**. Logic level of this pin is detected at powerup or reset to determine whether 100 Mbits/s full-duplex mode is available. The 100 Mbits/s full-duplex mode is available only if NDPRTR pin is low during reset indicating node operation. When autonegotiation is enabled, this input sets the ability register bit in advertisement register 4. When autonegotiation is not enabled, this input will select the mode of operation. See Table 8 for CIMEN description.
85, 82	10FDEN/LEDSP[1:0]	I/O	**10 Full-Duplex Enable (Ports 1, 0)**. Logic level of this pin is detected at powerup or reset to determine whether 10 Mbits/s full-duplex mode is available. The 10 Mbits/s full-duplex mode is available only if NDPRTR pin is low during reset indicating node operation. When autonegotiation is enabled, this input sets the ability register bit in advertisement register 4. When autonegotiation is not enabled, this input will select the mode of operation. This pin has an internal 40 kΩ pull-up resistor. See Table 9 for LEDSP description.

Pin Descriptions (continued)

Table 7. Autonegotiation Configuration (continued**)**

Pin No.	Pin Name	I/O	Pin Description
113, 54	10HDEN/LEDFD/FEFI-EN[1:0]	I/O	**10 Half-Duplex Enable**. The logic level of this pin is detected at powerup or reset to determine whether 10Mbits/s half-duplex mode is available. When autonegotiation is enabled, this input sets the ability register bit in advertisement register 4. When autonegotiation is not enabled, this input will select the mode of operation. This pin has an internal 40 kΩ pull-up resistor. See Table 8 for FEFI_EN and Table 9 for LEDFD descriptions.

Note: Many of these signals are dual-function pins. During reset, these pins may be pulled up or down (as shown in Figure 5) to configure various options. The secondary function is shown in smaller print and described in Table 8.

Table 8. Special Mode Configurations

Pin No.	Pin Name	I/O	Pin Description
110, 57	NDRPTR/LEDRX[1:0]	I/O	**Node-Repeater Select (Ports 1, 0)**. These pins are detected during powerup or reset to determine the mode of operation. If this pin is at logic high level, then the PHY will go into Repeater mode; otherwise, if logic low it will operate in node mode. These pins have an internal 40 kΩ pull-down. See Table 9 for LEDRX description.
125, 42	CIMEN/100FDEN[1:0]	I	**Carrier Integrity Monitor Enable (Ports 1, 0)**. The CIM function is only used for repeater operation. If both NDRPTR pin and CIMEN pin are at logic high level during powerup or reset, then the CIM function is enabled. See Table 7 for 100FDEN description.
116, 51	FOSEL[1:0]	I	**Fiber-Optic Mode Select**. This pin is tested during powerup or reset only. If this pin is detected to be at logic high level, then the PHY goes into fiber-optic mode.
38, 1	SRL10/FOSD+[1:0]	I	**Serial Mode Select**. At powerup or reset, if FOSEL pin is pulled low and SRL10 is pulled high, then the MII interface will be operated in serial mode for 10 Mbits/s operation. Fiber-optic mode and 10 Mbits/s serial mode cannot be set at the same time. Note that the serial mode is only supported for 10 Mbits/s repeater operation. See Table 2 for FOSD+ description.
128, 39	RPTR10CLK/FOSD–[1:0]	I/O	**10 Mbits/s Repeater Clock**. For 10 Mbits/s repeater mode, an external 10 MHz clock should be connected to this pin for clocking of the transmit data. See Table 2 for FOSD– description.
113, 54	FEFI_EN/10HDEN/LEDFD[1:0]	I/O	**Far-End Fault Indicator Enable**. At powerup or reset, if FOSEL pin is set high, logic level of this pin is latched into bit 11 of register 18h. This pin has an internal 40 kΩ pull-up resistor. See Table 7 for 10HDEN and Table 9 for LEDFD description.

Table 9. LED and Status Outputs

Pin No.	Pin Name	I/O	Pin Description
110, 57	LEDRX/NDRPTR[1:0]	I/O	**Receive LED (Ports 1, 0)**. This output will drive a 10 mA LED if the PHY is receiving data from the UTP cable. Place a 10 kΩ resistor across the LED pins if setting to nondefault mode, i.e., repeater mode. See Table 8 for NDRPTR description.
111, 56	LEDTX/ACTLED/ BPSCR[1:0]	I/O	**Transmit LED or Activity LED (Ports 1, 0)**. When bit 7 of register 17h is 0, this output will drive a 10 mA LED if the PHY is transmitting data; if the control bit is set, then the LED will be driven whenever there is a receive or transmit over the cable. Place a 10 kΩ resistor across the LED pins if setting to nondefault mode, i.e., bypass scrambler mode. See Table 6 for BPSCR description.
114, 53	LEDLNK/BPALIGN[1:0]	I/O	**Link LED (Ports 1, 0)**. This output will drive a 10 mA LED for as long as a valid link exists across the cable. Place a 10 kΩ resistor across the LED pins if setting to nondefault mode, i.e., bypass align mode. See Table 6 for BPALIGN description.
85, 82	LEDSP/10FDEN[1:0]	I/O	**Speed Status (Ports 1, 0)**. This output can be used to drive a 10 mA LED for as long as the PHY is in 100 Mbits/s mode. Place a 10 kΩ resistor across the LED pins if setting to nondefault mode, i.e., 10FD disable mode. See Table 7 for 10FDEN description.
113, 54	LEDFD/10HDEN/ FEFI_EN[1:0]	I/O	**Full-Duplex Status**. This output will drive a 10 mA LED when the LU3X32FT is in full-duplex mode. Place a 10 kΩ resistor across the LED pins if setting to nondefault mode, i.e., 10HD disable mode, as shown in Figure 5. See Table 7 for 10HDEN and Table 8 for FEFI_EN description.
112, 55	LEDCOL/BP4B5B[1:0]	I/O	**Collision LED**. This output will drive a 10 mA LED whenever the PHY senses a collision has occurred. Place a 10 kΩ resistor across the LED pins if setting to nondefault mode, i.e., bypass 4B/5B mode. See Table 6 for BP4B5B description.

Pin Descriptions (continued)

Table 10. Clock and Chip Reset

Pin No.	Pin Name	I/O	Pin Description
123, 44	XIN[1:0]	I	**25 MHz Clock Input (Ports 1, 0)**.
118, 49	RSTZ[1:0]	I	**Reset (Ports 1, 0) (Active-Low)**.

Table 11. Power and Ground

Plane	V_{CC} Pin		Associated Ground Pin	
	Name	Pin No.	Name	Pin No.
RX Analog	$RXV_{DD}1$[1:0] $RXV_{DD}2$[1:0]	30, 9 35, 4	RXGND1[1:0] RXGND2[1:0]	31, 8 34, 5
TX Analog	$TXV_{DD}1$[1:0] $TXV_{DD}2$[1:0]	20, 19 24, 15	TXGND1[1:0]	21, 18
CS	CSV_{DD}[1:0] $FOV_{DD}10$[1:0]	28, 11 29, 10	CSGND[1:0]	27, 12
Digital	$V_{DD}2$[1:0] $V_{DD}5$[1:0] $V_{DD}6$[1:0] $V_{DD}8$[1:0] $EQV_{DD}1$[1:0]	93, 74 106, 61 108, 59 95, 72 120, 47	GND2[1:0] GND8[1:0] GND9[1:0] EQGND1[1:0]	94, 73 96, 71 124, 43 121, 46
Clock	$XTLV_{DD}$[1:0]	117, 50	—	—

Functional Description

The LU3X32FT integrates a 100Base-X physical sublayer (PHY), a 100Base-TX physical medium dependent (PMD) transceiver and a complete 10Base-T module into a single chip for both 10 Mbits/s and 100 Mbits/s Ethernet operation for two-ports. It also supports 100Base-FX operation through external fiber-optic transceivers. This device provides two *IEEE* 802.3U compliant media independent interfaces (MII) to communicate between the physical signaling and the medium access control (MAC) layers for both 100Base-X and 10Base-T operations. The device is capable of operating in either full-duplex mode or half-duplex mode in either 10 Mbits/s or 100 Mbits/s operation independently per port. Operational modes can be selected by hardware configuration pins or software settings of management registers, or they can be determined by the on-chip autonegotiation logic.

The 10Base-T section of each port consists of the 10 Mbits/s transceiver modules with filters and Manchester ENDEC modules.

The 100Base-X section of the each port implements the following functional blocks:

- 100Base-X physical coding sublayer (PCS)
- 100Base-X physical medium attachment (PMA)
- Twisted-pair transceiver (PMD)

The 100Base-X and 10Base-T sections of each port share the following functional blocks:

- Clock synthesizer module (CSM)
- MII registers
- *IEEE* 802.3U autonegotiation

Each of these functional blocks is described below.

Media Independent Interface (MII)

The LU3X32FT implements an *IEEE* 802.3U Clause 22 compliant MII interface as described below.

Interface Signals

Transmit Data Interface. Each MII transmit data interface comprises seven signals: TXD[3:0] are the nibble size data path, TXEN signals the presence of data on TXD, TXER indicates substitution of data with the HALT symbol, and TXCLK carries the transmit clock that synchronizes all the transmit signals. In node mode, TXCLK is supplied by the on-chip clock synthesizer; in 100 Mbits/s repeater mode, transmit signals are synchronized to the clock on XIN pin; in 10 Mbits/s repeater mode operation, an external clock must be connected to the RPTR10CLK pin to synchronize the data transfer.

Receive Data Interface. Each MII receive data interface also comprises seven signals: RXD[3:0] are the nibble size data path, RXDV signals the presence of data on RXD, RXER indicates the validity of data, and RXCLK carries the receive clock. Depending upon the operation mode, RXCLK signal is generated by the clock recovery module of either the 100Base-X or 10Base-T receiver.

Status Interface. Two status signals, COL and CRS, are generated in the LU3X32FT to indicate collision status and carrier sense status to the MAC for each port. COL is asserted asynchronously whenever that port is transmitting and receiving at the same time in a half-duplex operation mode. In full-duplex mode, COL is inactive. For repeater mode operation, the COL signal line indicates false carrier sense condition. CRS is asserted asynchronously whenever there is activity on either the transmitter or the receiver. In repeater or full-duplex mode, CRS is asserted only when there is activity on the receiver.

Functional Description (continued)

Operation Modes

Each port of the LU3X32FT supports three operation modes and an isolate mode as described below.

100 Mbits/s Mode. For 100 Mbits/s operation, the MII operates in nibble mode with a clock rate of 25 MHz. In normal operation, the MII data at RXD[3:0] and TXD[3:0] are 4-bit wide. In bypass mode (either BYP_4B5B or BYP_ALIGN option selected), the MII data takes the form of 5-bit code-groups. The least significant 4 bits appear on TXD[3:0] and RXD[3:0] as usual, and the most significant bits (TXD[4] and RXD[4]) appear on the TXER and RXER pins, respectively.

10 Mbits/s Nibble Mode. For 10 Mbits/s nibble mode operation, the TXCLK and RXCLK operate at 2.5 MHz. The data paths are 4 bits wide using TXD[3:0] and RXD[3:0] signal lines. This mode is not supported for repeaters.

10 Mbits/s Serial Mode. The LU3X32FT implements a serial mode for 10Base-T repeater applications. This mode is selected by strapping the NDRPTR pin (57, 110) and SRL10 pin (pins 1, 38) to logic high level and hold FOSEL pin (pins 116, 51) at logic low level during powerup or reset. When operating in this mode, the LU3X32FT accepts NRZ serial data on the TXD[0] input and provides NRZ serial data output on RXD[0] with a clock rate of 10 MHz. The unused MII signals TXD[3:1], RXD[3:1], and RXDV are ignored during serial mode. The PCS control signals CRS and COL continue to function normally.

MII Isolate Mode. The LU3X32FT implements an MII isolate mode that is controlled by bit 10 of the control register (register address 0h). The LU3X32FT will set this bit to one if the PHY address is set to 00000 upon powerup/hardware reset. Otherwise, the LU3X32FT will initialize this bit to 0. Setting the bit to a 1 will also put the PHY in MII isolate mode. Note that port 1 cannot powerup/reset into isolate mode, since its PHY[0] is forced to 1; however, it can be programmed into isolate mode by setting bit 10 of the control register (register 0h).

The isolate mode can also be activated by setting the PHY address (bits 4 through 0 of register 19h) to 0 through the serial management interface, although the content of the isolate register is not affected by the modification of PHY address.

In isolate mode, the LU3X32FT does not respond to packet data present at TXD[3:0], TXEN, and TXER inputs and presents a high impedance on the TXCLK, RXCLK, RXDV, RXER, RXD[3:0], COL, and CRS outputs. The LU3X32FT will continue to respond to all management transactions.

Serial Management Interface

Each port of the LU3X32FT supports SMI. The serial management interface (SMI) is used to both obtain status from and to configure each PHY. This mechanism corresponds to the MII spec for 100Base-X (Clause 22) and supports registers 0 through 6. Additional vendor-specific registers are implemented within the range of 16 to 31. All the registers are described in the register section.

Functional Description (continued)

Management Register Access. The SMI consists of two pins, management data clock (MDC) and management data input/output (MDIO). The LU3X32FT is designed to support an MDC frequency ranging up to the *IEEE* specification of 2.5 MHz. Each MDIO line is bidirectional and may be shared by up to 32 devices (16 LU3X32FT devices).

The MDIO pin requires a pull-up resistor which, during IDLE and turnaround periods, will pull MDIO to a logic one state. Each MII management data frame is 64 bits long. The first 32 bits are preamble consisting of 32 contiguous logic one bits on MDIO and 32 corresponding cycles on MDC. Following preamble is the start-of-frame field indicated by a <01> pattern. The next field signals the operation code (OP): <10> indicates READ from MII management register operation, and <01> indicates WRITE to MII management register operation. The next two fields are PHY device address and MII management register address. Both of them are 5-bits wide, and the most-significant bit is transferred first.

During READ operation, a 2-bit turnaround (TA) time spacing between register address field and data field is provided for the MDIO to avoid contention. Following the turnaround time, a 16-bit data stream is read from or written into the MII management registers of the LU3X32FT.

The LU3X32FT supports a preamble suppression mode as indicated by a 1 in bit 6 of the basic mode status register (BMSR, address 01h.) If the station management entity (i.e., MAC or other management controller) determines that all PHYs in the system support preamble suppression by reading a 1 in this bit, then the station management entity need not generate preamble for each management transaction. The LU3X32FT requires a single initialization sequence of 32 bits of preamble following powerup/hardware reset. This requirement is generally met by the mandatory pull-up resistor on MDIO or the management access made to determine whether preamble suppression is supported. While the LU3X32FT will respond to management accesses without preamble, a minimum of one idle bit between management transactions is required as specified in *IEEE* 802.3U.

The PHY device addresses for the LU3X32FT are stored in the PHY address registers (register address 19h). It is initialized by the four I/O pins designated as PHY[4:1] during powerup or hardware reset. PHY[0] is forced to 0 for port 0 and 1 for port 1. The entire PHY address can be changed by writing into PHY address register, address 19h.

MDIO Interrupt. The LU3X32FT implements interrupt capability that can be used to notify the management station of certain events. It generates an active-low interrupt pulse on the MDIOINT output pin whenever one of the interrupt status registers (register address 1Eh) becomes set while its corresponding interrupt mask register (register address 1Dh) is unmasked. Reading the interrupt status register (register 1Eh) shows the source of the interrupts, and clears all bits of the interrupt status register.

In addition to the MDIOINT pins, the LU3X32FT can also support the interrupt scheme used by the *TI ThunderLAN** MAC. This option can be enabled by setting bit 11 of register 17h. Whenever this bit is set, the interrupt is signaled through both the MDIOINT pin and embedded in the MDIO signal.

* *TI* is a registered trademark and *ThunderLAN* is a trademark of Texas Instruments, Inc.

Functional Description (continued)

100Base-X Module

The LU3X32FT implements a 100Base-X compliant PCS and PMA and 100Base-TX compliant TP-PMD for each port as illustrated in Figure 3. Bypass options for each of the major functional blocks within the 100Base-X PCS provide flexibility for various applications. 100 Mbits/s PHY loopback is included for diagnostic purposes.

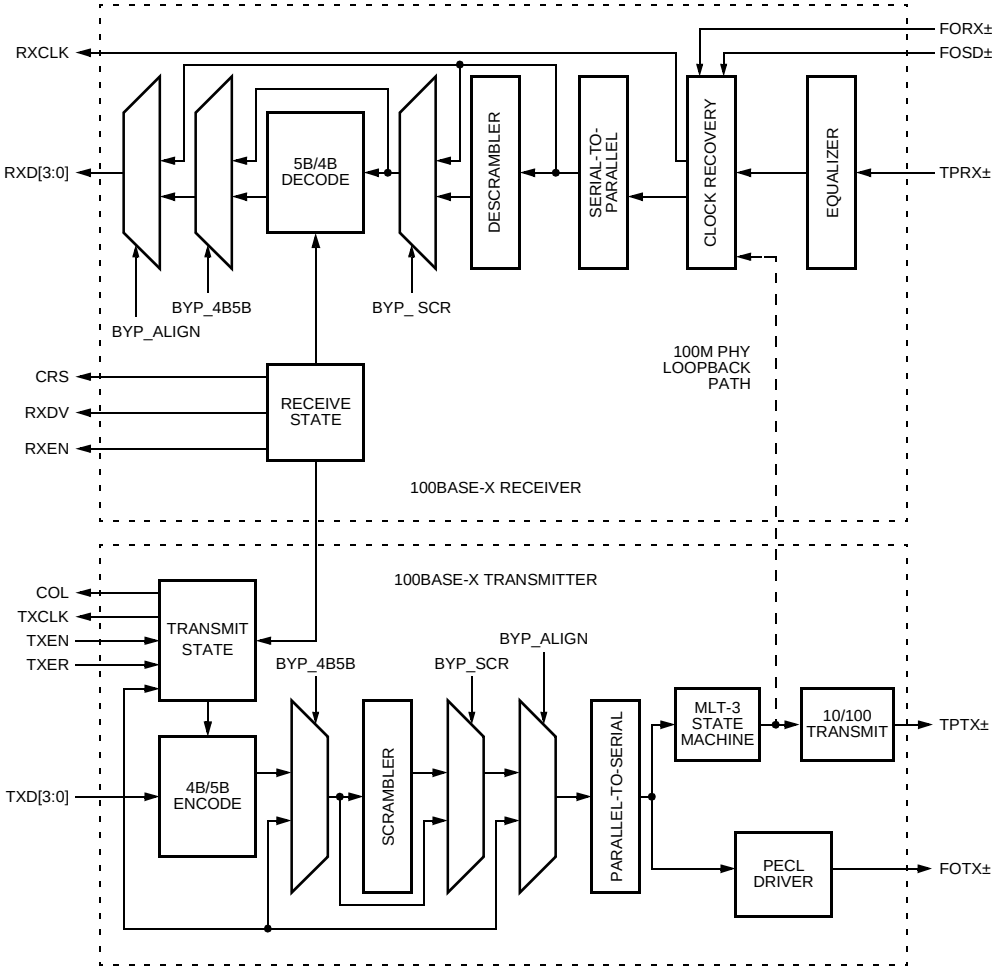

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Figure 3. 100Base-X Data Path (per port)

100Base-X Transmitter

The 100Base-X transmitter consists of functional blocks which convert synchronous 4-bit nibble data, as provided by the MII, to a 125 Mbits/s serial data stream. This data stream may be routed either to the on-chip twisted-pair PMD for 100Base-TX signaling, or to an external fiber-optic PMD for 100Base-FX applications. The LU3X32FT implements the 100Base-X transmit state machines as specified in the *IEEE* 802.3U standard, Clause 24 and comprises the following functional blocks in its data path:

- Symbol encoder
- Scrambler block
- Parallel/serial converter and NRZ/ NRZI encoder block

Functional Description (continued)

Symbol Encoder. The symbol encoder converts 4-bit (4B) nibble data generated by the MAC into 5-bit (5B) symbols for transmission. This conversion is required to allow control symbols to be combined with data symbols. Refer to the table below for 4B to 5B symbol mapping.

Following onset of the TXEN signal, the 4B/5B symbol encoder replaces the first two nibbles of the preamble from the MAC frame with a /J/K code-group pair (11000 10001) start-of-stream delimiter (SSD). The symbol encoder then replaces subsequent 4B codes with corresponding 5B symbols. Following negation of the TXEN signal, the encoder substitutes the first two IDLE symbol with a /T/R code-group pair (01101 00111) end-of-stream delimiter (ESD) and then continuously injects IDLE symbols into the transmit data stream until the next transmit packet is detected.

Assertion of the TXER input while the TXEN input is also asserted will cause the LU3X32FT to substitute HALT code-groups for the 5B code derived from data present at TXD[3:0]. However, the SSD (/J/K) and ESD (/T/R) will not be substituted with halt code-groups. As a result, the assertion of TXER while TXEN is asserted will result in a frame properly encapsulated with the /J/K and /T/R delimiters which contains HALT code-groups in place of the data code-groups.

The 100 Mbits/s symbol decoder translates all invalid code groups into 0Eh by default. In case the ACCEPT HALT register is set (bit 5 of register 18h), the HALT code group (00100) is translated into 05h instead.

Functional Description (continued)

Table 12. Symbol Code Scrambler

Symbol Name	5B Code [4:0]	4B Code [3:0]	Interpretation
0	11110	0000	Data 0
1	01001	0001	Data 1
2	10100	0010	Data 2
3	10101	0011	Data 3
4	01010	0100	Data 4
5	01011	0101	Data 5
6	01110	0110	Data 6
7	01111	0111	Data 7
8	10010	1000	Data 8
9	10011	1001	Data 9
A	10110	1010	Data A
B	10111	1011	Data B
C	11010	1100	Data C
D	11011	1101	Data D
E	11100	1110	Data E
F	11101	1111	Data F
I	11111	undefined	IDLE: interstream fill code
J	11000	0101	First start-of-stream delimiter
K	10001	0101	Second start-of-stream delimiter
T	01101	undefined	First end-of-stream delimiter
R	00111	undefined	Second end-of-stream delimiter
H	00100	undefined	HALT: transfer error
V	00000	undefined	Invalid code
V	00001	undefined	Invalid code
V	00010	undefined	Invalid code
V	00011	undefined	Invalid code
V	00101	undefined	Invalid code
V	00110	undefined	Invalid code
V	01000	undefined	Invalid code
V	01100	undefined	Invalid code
V	10000	undefined	Invalid code
V	11001	undefined	Invalid code

Functional Description (continued)

Scrambler Block. For 100Base-TX applications, the scrambler is required to control the radiated emissions at the media connector and on the twisted-pair cable.

The LU3X32FT implements a data scrambler as defined by the TP-PMD stream cipher function per port. The scrambler uses an 11-bit ciphering linear feedback shift register (LFSR) with the following recursive linear function:

$$X[n] = X[n - 11] + X[n - 9] \text{ (modulo 2)}$$

The output of the LFSR is combined with data from the encoder via an exclusive-OR logic function. By scrambling the data, the total energy launched onto the cable is randomly distributed over a wide frequency range.

A seed value for the scrambler function can be loaded by setting bit 4 of register 18h. When this bit is set, the content of bits 10 through 0 of register 19h, that compose of the 5-bit PHY address and a 6-bit user seed, will be loaded into the LFSR. By specifying unique seed value for each PHY in a system, the total EMI energy produced by a repeater application can be reduced.

Parallel to Serial & NRZ-NRZI Conversion. After the transmit data stream is scrambled, data is loaded into a shift register and clocked out with a 125 MHz clock into a serial bit stream. The serialized data is further converted from NRZ to NRZI format, which produces a transition on every logic 1 and no transition on logic 0.

Collision Detect. During 100 Mbits/s half-duplex operation, collision condition is detected if the transmitter and receiver become active simultaneously. Collision detection is indicated by the COL pin of the MII. For full-duplex applications, the COL signal is never asserted. A collision test register exists at address 0 bit 7.

100Base-X Receiver

The 100Base-X receivers consist of functional blocks required to recover and condition the 125 Mbits/s receive data stream. The LU3X32FT implements the 100Base-X receive state machine diagram as given in ANSI/*IEEE* Standard 802.3u, Clause 24 for each port. The 125 Mbits/s receive data stream may originate from the on-chip twisted-pair transceiver in a 100Base-TX application. Alternatively, the receive data stream may be generated by an external optical receiver as in a 100Base-FX application.

Each receiver block consists of the following functional blocks:

- Clock recovery module
- NRZI/ NRZ and serial/parallel decoder
- Descrambler
- Symbol alignment block
- Symbol decoder
- Collision detect block
- Carrier sense block
- Stream decoder block

Clock Recovery. The clock recovery module accepts 125 Mbits/s scrambled NRZI data stream from either the on-chip 100Base-TX receiver or from an external 100Base-FX transceiver. The LU3X32FT uses an onboard digital phase-locked loop (PLL) to extract clock information of the incoming NRZI data, which is then used to retime the data stream and set data boundaries.

After power-on or reset, the PLL locks to a free-running 25 MHz clock derived from the external clock source. When initial lock is achieved, the PLL switches to lock to the data stream, extracts a 125 MHz clock from the data, and uses it for bit framing of the recovered data.

Functional Description (continued)

NRZI/NRZ & Serial/Parallel Conversion. The recovered data is converted from NRZI to NRZ format. The data is not necessarily aligned to 4B/5B code-group's boundary.

Data Descrambling. The descrambler acquires synchronization with the data stream by recognizing IDLE bursts of 40 or more bits and locking its deciphering linear feedback shift register (LFSR) to the state of the scrambling LFSR. Upon achieving synchronization, the incoming data is XORed by the deciphering LFSR and descrambled.

In order to maintain synchronization, the descrambler continuously monitors the validity of the unscrambled data that it generates. To ensure this, a link state monitor and a hold timer are used to constantly monitor the synchronization status. Upon synchronization of the descrambler, the hold timer starts a 722 µs countdown. Upon detection of sufficient IDLE symbols within the 722 µs period, the hold timer will reset and begin a new countdown. This monitoring operation will continue indefinitely given a properly operating network connection with good signal integrity. If the link state monitor does not recognize sufficient unscrambled IDLE symbols within the 722 µs period, the descrambler will be forced out of the current state of synchronization and reset in order to reacquire synchronization. Register 18h, bit 3, can be used to extend the timer to 2 ms.

Symbol Alignment. The symbol alignment circuit in the LU3X32FT determines code word alignment by recognizing the /J/K delimiter pair. This circuit operates on unaligned data from the descrambler. Once the /J/K symbol pair (11000 10001) is detected, subsequent data is aligned on a fixed boundary.

Symbol Decoding. The symbol decoder functions as a look up table that translates incoming 5B symbols into 4B nibbles. The symbol decoder first detects the /J/K symbol pair preceded by IDLE symbols and replaces the symbol with MAC preamble. All subsequent 5B symbols are converted to the corresponding 4B nibbles for the duration of the entire packet. This conversion ceases upon the detection of the /T/R symbol pair denoting the end of stream delimiter (ESD). The translated data is presented on the RXD[3:0] signal lines with RXD[0] represents the least-significant-bit of the translated nibble.

Valid Data Signal. The receive data valid signal (RXDV) indicates that recovered and decoded nibbles are being presented on the RXD[3:0] outputs synchronous to RXCLK. RXDV is asserted when the first nibble of translated / J/K is ready for transfer over the media independent interface (MII). It remains active until either the /T/R delimiter is recognized, link test indicates failure, or no signal is detected. On any of these conditions, RXDV is deasserted.

Receiver Errors. The RXER signals are used to communicate receiver error conditions. While the receiver is in a state of holding RXDV asserted, the RXER will be asserted for each code word that does not map to a valid code-group.

100Base-X Link Monitor

The 100Base-X link monitor function allows the receivers to ensure that reliable data is being received. Without reliable data reception, the link monitor will halt both transmit and receive operations until such time that a valid link is detected.

The LU3X32FT performs the link integrity test as outlined in *IEEE* 100Base-X (Clause 24) Link Monitor state diagram. The link status is multiplexed with 10 Mbits/s link status to form the reportable link status bit in serial management register 1, and driven to the LEDLNK pin.

When persistent signal energy is detected on the network, the logic moves into a link-ready state after approximately 500 µs and waits for an enable from the autonegotiation module. When received, the link-up state is entered, and the transmit and receive logic blocks become active. Should autonegotiation be disabled, the link integrity logic moves immediately to the link-up state after entering the link-ready state.

Functional Description (continued)

Carrier Sense. Carrier sense (CRS) for 100 Mbits/s operation is asserted upon the detection of two non-contiguous zeros occurring within any 10-bit boundary of the receive data stream.

The carrier sense function is independent of symbol alignment. For 100 Mbits/s half-duplex operation, CRS is asserted during either packet transmission or reception. For 100 Mbits/s full-duplex operation, CRS is asserted only during packet reception. When the IDLE symbol pair is detected in the receive data stream, CRS is deasserted. In repeater mode, CRS is only asserted due to receive activity.

Bad SSD Detection. A bad start of stream delimiter (Bad SSD) is an error condition that occurs in the 100Base-X receiver if carrier is detected (CRS asserted), and a valid /J/K set of code groups (SSD) is not received.

If this condition is detected, then the LU3X32FT will assert RXER and present RXD[3:0] = 1110 to the MII for the cycles that correspond to received 5B code-groups until at least two IDLE code groups are detected. In addition, the false carrier counter (address 13h) will be incremented by one. Once at least two IDLE code groups are detected, RXER and CRS become de-asserted.

Far-End Fault Indication. Autonegotiation provides a mechanism for transferring information from the local station to the link partner that a remote fault has occurred for 100Base-TX. As autonegotiation is not currently specified for operation over fiber, the far-end fault indication function (FEFI) provides this capability for 100Base-FX applications.

A remote fault is an error in the link that one station can detect while the other cannot. An example of this is a disconnected wire at a station's transmitter. This station will be receiving valid data and will detect that the link is good via the link integrity monitor, but will not be able to detect that its transmission is not propagating to the other station.

A 100Base-FX station that detects such a remote fault may modify its transmitted IDLE stream from all ones to a group of 84 ones followed by a single 0. This is referred to as the FEFI IDLE pattern.

The FEFI function is controlled by bit 11 of register 18h. It is initialized to 1 (enabled) if both the FOSEL pin and FEFI_EN pin are at logic high level during powerup or reset. If the FEFI function is enabled, the LU3X32FT will halt all current operations and transmit the FEFI IDLE pattern when FOSD+/FOSD– signal is deasserted following a good link indication from the link integrity monitor. Transmission of the FEFI IDLE pattern will continue until FOSD+/FOSD– signal is asserted. If three or more FEFI IDLE patterns are detected by the LU3X32FT, then bit 4 of the basic mode status register (address 01h) is set to one until read by management. Additionally, upon detection of far-end fault, all receive and transmit MII activity is disabled/ignored.

Carrier Integrity Monitor. The carrier integrity monitor (CIM) function protects the repeater from transient conditions that would otherwise cause spurious transmission due to a faulty link. This function is required for repeater applications and is not specified for node applications.

The CIM function is controlled by bit 10 of register 18h. It is initialized to 1 (enabled) if both the NDRPTR pin and CIMEN pin are at logic high level during powerup or reset. If the CIM determines that the link is unstable, the LU3X32FT will not propagate the received data or control signaling to the MII and will ignore data transmitted via the MII. The LU3X32FT will continue to monitor the receive stream for valid carrier events. The false carrier counter (address 13h) increments each time the link is unstable (bad SSD), the FCRS pin stays high as long as error condition exists. Two back-to-back false carrier events will isolate the PHY, incrementing the associated isolate counter (register address 12h) once.

Functional Description (continued)

100Base-TX Transceiver

LU3X32FT implements TP-PMD compliant transceivers for 100Base-TX operation. The differential transmit driver is shared by the 10Base-T and 100Base-TX subsystems. This arrangement results in one device that uses the same external magnetics for both the 10Base-T and the 100Base-TX transmission with simple RC component connections. The individually wave-shaped 10Base-T and 100Base-TX transmit signals are multiplexed in the transmit output driver section.

Transmit Drivers. The LU3X32FT 100Base-TX transmit drivers implement MLT-3 translation and wave-shaping functions. The rise/fall time of the output signal is closely controlled to conform to the target range specified in the ANSI TP-PMD standard.

Twisted-Pair Receiver. For 100Base-TX operation, the incoming signal is detected by the on-chip twisted-pair receivers that comprise the differential line receiver, an adaptive equalizer, and baseline wander compensation circuits.

The LU3X32FT uses adaptive equalizers which change filter frequency response in accordance with cable length. The cable length is estimated based on the incoming signal strength. The equalizer tunes itself automatically for any cable length to compensate for the amplitude and phase distortions incurred from the cable.

10Base-T Module

The 10Base-T transceiver modules are *IEEE* 802.3 compliant. They include the receiver, transmitter, collision, heartbeat, loopback, jabber, waveshaper, and link integrity functions, as defined in the standard. Figure 4 provides an overview for the 10Base-T modules.

The LU3X32FT 10Base-T modules are comprised of the following functional blocks:

- Manchester encoder and decoder
- Collision detector
- Link test function
- Transmit driver and receiver
- Serial and parallel interface
- Jabber and SQE test functions
- Polarity detection and correction

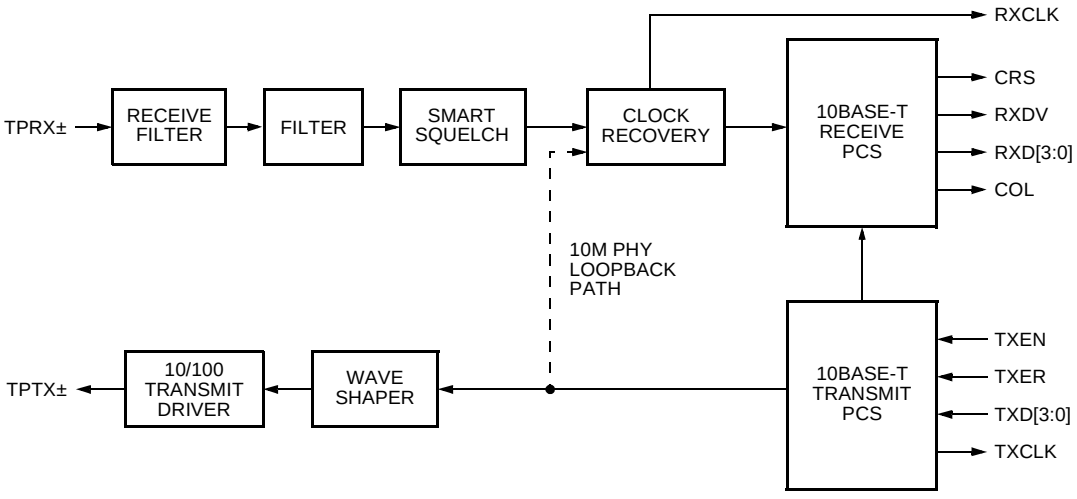

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Figure 4. 10Base-T Module Data Path (per port)

Functional Description (continued)

Operation Modes

The LU3X32FT 10Base-T modules are capable of operating in either half-duplex mode or full-duplex mode. In half-duplex mode, the LU3X32FT functions as an *IEEE* 802.3 compliant transceiver with fully integrated filtering. The COL pin signals squelch jabber, and the CRS is asserted during transmit and receive. In full-duplex mode, the LU3X32FT can simultaneously transmit and receive data.

Manchester Encoder/Decoder. Data encoding and transmission begins when the transmit enable input (TXEN) goes high and continues as long as the transceiver is in good link state. Transmission ends when the transmit enable input goes low. The last transition occurs at the center of the bit cell if the last bit is a 1, or at the boundary of the bit cell if the last bit is 0.

Decoding is accomplished by a differential input receiver circuit and a phase-locked loop that separates the Manchester-encoded data stream into clock signals and NRZ data. The decoder detects the end of a frame when no more mid-bit transitions are detected. Within one and a half bit times after the last bit, carrier sense is de-asserted.

Transmit Driver and Receiver. LU3X32FT integrates all the required signal conditioning functions in its 10Base-T blocks such that external filters are not required. Only an isolation transformer and impedance matching resistors are needed for the 10Base-T transmit and receive interface. The internal transmit filtering ensures that all the harmonics in the transmit signal are attenuated properly.

Smart Squelch. The smart squelch circuit is responsible for determining when valid data is present on the differential receive. The LU3X32FT implements an intelligent receive squelch on the TPRX± differential inputs to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the *IEEE* 802.3 10Base-T standard) to determine the validity of data on the twisted-pair inputs.

The signal at the start of the packet is checked by the analog squelch circuit, and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly, the opposite squelch level must then be exceeded within 150 ns. Finally, the signal must exceed the original squelch level within a further 150 ns to ensure that the input waveform will not be rejected.

Only after all of these conditions have been satisfied will a control signal be generated to indicate to the remainder of the circuitry that valid data is present.

Valid data is considered to be present until the squelch level has not been generated for a time longer than 200 ns, indicating end-of-packet. Once good data has been detected, the squelch levels are reduced to minimize the effect of noise causing premature end-of-packet detection. The receive squelch threshold level can be lowered for use in longer cable applications. This is achieved by setting bit 11 or register address 1Ah.

Carrier Sense. Carrier sense (CRS) may be asserted due to receive activity once valid data is detected via the smart squelch function.

For 10 Mbits/s half-duplex operation, CRS is asserted during either packet transmission or reception.

For 10 Mbits/s full-duplex operation, the CRS is asserted only due to receive activity. In repeater mode, CRS is only asserted due to receive activity. CRS is deasserted following an end of packet.

Collision Detection. For half-duplex operation, a 10Base-T collision is detected when the receive and transmit channels are active simultaneously. Collisions are reported by the COL signal on the MII. If the ENDEC is transmitting when a collision is detected. The COL signal remains set for the duration of the collision.

Functional Description (continued)

SQE Test Function. Approximately 1 µs after the transmission of each packet, a signal quality error (SQE) signal of approximately 10 bit times is generated (internally) to indicate successful transmission. SQE is reported as a pulse on the COL signal of the MII. This function can be enabled by setting bit 12 of register 1Ah. The SQE test function is disabled in full-duplex mode.

Jabber Function. The jabber function monitors the LU3X32FTs output and disables the transmitter if it attempts to transmit a longer than legal-sized packet. If TXEN is high for greater than 24 ms, the 10Base-T transmitter will be disabled and COL will go active-high.

Once disabled by the jabber function, the transmitter stays disabled for the entire time that the TXEN signal is asserted. This signal has to be deasserted for approximately 256 ms (the unjab time) before the jabber function reenables the transmit outputs and de-asserts COL signal.

The jabber function can be disabled by setting bit 10 of register 1Ah.

Link Test Function. A link pulse is used to check the integrity of the connection with the remote end. If valid link pulses are not received, the link detector disables the 10Base-T twisted-pair transmitter, receiver, and collision detection functions.

The link pulse generator produces pulses as defined in the *IEEE* 802.3 10Base-T standard. Each link pulse is nominally 100 ns in duration and is transmitted every 16 ms, in the absence of transmit data.

Automatic Link Polarity Detection. The LU3X32FT's 10Base-T transceiver modules incorporate an automatic link polarity detection circuit. The inverted polarity is determined when seven consecutive link pulses of inverted polarity or three consecutive receive packets are received with inverted end-of-packet pulses. If the input polarity is reversed, the error condition will be automatically corrected and reported in bit 15 of register 1Ch.

The automatic link polarity detection function can be disabled by setting bit 3 of register 1Ah.

Clock Synthesizer

The LU3X32FT implements a clock synthesizer that generates all the reference clocks needed from a single external frequency source. The clock source must be a TTL level signal at 25 MHz ± 50 ppm, as shown in Figure 15.

Functional Description (continued)

Autonegotiation

The autonegotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest-performance mode of operation supported by both devices. Fast link pulse (FLP) bursts provide the signaling used to communicate autonegotiation abilities between two devices at each end of a link segment. For further detail regarding autonegotiation, refer to Clause 28 of the *IEEE* 802.3U specification. The LU3X32FT supports four different Ethernet protocols, so the inclusion of autonegotiation ensures that the highest-performance protocol will be selected based on the ability of the link partner.

The autonegotiation function within the LU3X32FT can be controlled either by internal register access or by the use of configuration pins. At powerup and at device reset, the configuration pins are sampled. If disabled, autonegotiation will not occur until software enables bit 12 in register 0. If autonegotiation is enabled, the negotiation process will commence immediately.

When autonegotiation is enabled, the LU3X32FT transmits the abilities programmed into the autonegotiation advertisement register at address 04h via FLP bursts. Any combination of 10 Mbits/s, 100 Mbits/s, half-duplex, and full-duplex modes may be selected. Autonegotiation controls the exchange of configuration information. Upon successful autonegotiation, the abilities reported by the link partner are stored in the autonegotiation link partner ability register at address 05h.

The contents of the autonegotiation link partner ability register are used to automatically configure to the highest-performance protocol between the local and far-end nodes. Software can determine which mode has been configured by autonegotiation by comparing the contents of register 04h and 05h and then selecting the technology whose bit is set in both registers of highest priority relative to the following list:

1. 100Base-TX full duplex (highest priority)
2. 100Base-TX half duplex
3. 10Base-T full duplex
4. 10Base-T half duplex (lowest priority)

The basic mode control register at address 00h provides control of enabling, disabling, and restarting of the autonegotiation function. When autonegotiation is disabled the speed selection bit (bit 13) controls switching between 10 Mbits/s or 100 Mbits/s operation, while the duplex mode bit (bit 8) controls switching between full-duplex operation and half-duplex operation. The speed selection and duplex mode bits have no effect on the mode of operation when the autonegotiation enable bit (bit 12) is set.

The basic mode status register at address 01h indicates the set of available abilities for technology types (bits 15 to 10), autonegotiation ability (bit 3), and extended register capability (bit 0). These bits are hardwired to indicate the full functionality of the LU3X32FT. The BMSR also provides status on:

- Whether autonegotiation is complete (bit 5).
- Whether the link partner is advertising that a remote fault has occurred (bit 4).
- Whether a valid link has been established (bit 2).

The autonegotiation advertisement register at address 04h indicates the autonegotiation abilities to be advertised by the LU3X32FT. All available abilities are transmitted by default, but any ability can be suppressed by writing to this register or configuring external pins.

The autonegotiation link partner ability register at address 05h indicates the abilities of the link partner as indicated by autonegotiation communication. The contents of this register are considered valid when the autonegotiation complete bit (bit 5, register address 01h) is set.

Functional Description (continued)

Reset Operation

The LU3X32FT can reset each port either by hardware or software. A hardware reset is accomplished by applying a negative pulse, with a duration of at least 1 ms, to the RSTZ pin of the LU3X32FT during normal operation. A software reset is activated by setting the RESET bit in the basic mode control register (bit 15, register 00h). This bit is self-clearing and, when set, will return a value of 1 until the software reset operation has completed.

Both hardware and software reset operations initialize all registers to their default values. This process includes re-evaluation of all hardware configurable registers.

Logic levels on several I/O pins are detected during the hardware and software reset period to determine the initial functionality of each of the ports. Some of these pins are used as output ports after reset operation.

Care must be taken to ensure that the configuration setup will not interfere with normal operation. Dedicated configuration pins can be tied to VCC or ground directly. Configuration pins multiplexed with logic level output functions should be either weakly pulled-up or weakly pulled-down through resistors. Configuration pins multiplexed with LED outputs should be set up with one of the following circuits shown in Figure 5. Note that the 10 kΩ resistor is needed only for nondefault configuration.

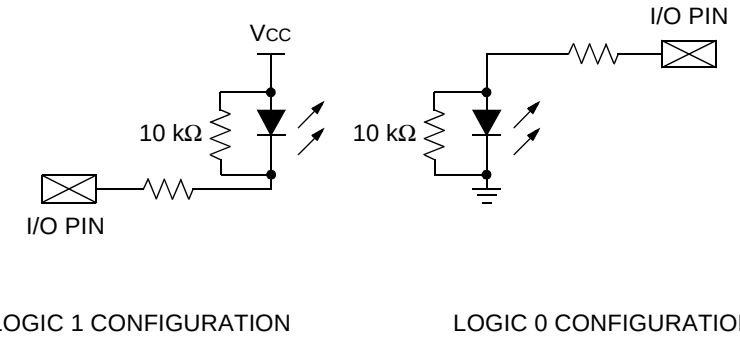

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Figure 5. Hardware RESET Configurations

PHY Address

During hardware reset, the logic level of the PHY address pins are latched into bits 4 through 1 of the PHY address register, address 19h, respectively. Because the LU3X32FT implements two physical layers, the PHY address bit 0 is internally set to 0 for port 0 and 1 for port 1. This 5-bit address is used as the PHY address for serial management interface communication. Note that initializing all configurable PHY addresses to zero automatically isolates the MII interface of port 0.

Node/Repeater Mode Select

A logic 1 level on pins 57 or 110 during reset configures the port to function as a repeater. Otherwise, this device will function in node mode.

Fiber Mode Select

A logic 1 level on pins 51 or 116 during reset configures the 100 Mbits/s section of the respective port for 100Base-FX operation.

Functional Description (continued)

Autonegotiation & Speed Configuration

The three pins listed in Table 13 configure the speed capability of LU3X32FT. The logic state of these pins, at powerup or reset, are latched into the advertisement register (register address 04h) for autonegotiation purpose. These pins are also used for evaluating the default value in the base mode control register (register 00h) according to the Table 13.

Table 13. Initial Value of Autonegotiation Registers

Configuration Pins at RESET			Registers Initial Value		
AUTONEN Pins 45, 122	**100FDEN Pins 42, 125 (Reg 4.8)**	**10FDEN Pins 82, 85 (Reg 4.6)**	**AUTONEG Reg 0.12**	**SPEED Reg 0.13**	**DUPLEX Reg 0.8**
0	1	X	0	1	1
0	0	1	0	1	1
0	0	0	0	1	0
1	X	X	1	0	0

Functional Description (continued)

100Base-X PCS Configuration

The logic state of BPSCR and BPALIGN pins latched into bits 15 and 12 of the Config 100 register at address 18h during powerup or reset. Bit 14 of register 18h (BP4B5B) is initialized to 0 during power-on or reset. These registers configure the functionality of 100Base-X PCS (physical coding sublayer).

Register Descriptions

Table 14. MII Management Registers Legends

Register Address	Register Name	Basic/Extended
0h	Control register	B
1h	Status register	B
2h—3h	PHY identifier register	E
4h	Autonegotiation advertisement register	E
5h	Autonegotiation link partner ability register	E
6h	Autonegotiation expansion register	E
7h—Fh	*IEEE* reserved	E
12h	Isolate counter	E
13h	False carrier counter	E
15h	Receive error counter	E
17h	PHY control/status register	E
18h	Config 100 register	E
19h	PHY address register	E
1Ah	Config 10 register	E
1Bh	Status 100 register	E
1Ch	Status 10 register	E
1Dh	Interrupt mask register	E
1Eh	Interrupt status register	E

Legend for Tables 15—32:
RO—Read only
R/W—Read and write capable
SC—Self-clearing
LL—Latching low, unlatch on read
LH—Latching high, unlatch on read
COR—Clear on read

Register Description (continued)

Table 15. Control Register (Per Port) [Register 0h]

Bit(s)	Name	Description	R/W	Default
15	Reset	1—PHY reset. 0—Normal operation. Setting this bit initiates the software reset function that resets the entire LU3X32FT device, except for the phase-locked loop circuit. It will relatch in all hardware configuration pin values and set all registers to their default values. The software reset process takes 25 µs to complete. This bit, which is self-clearing, returns a value of 1 until the reset process is complete.	R/W SC	0h
14	Loopback	1—Enable loopback mode. 0—Disable loopback mode. This bit controls the PHY loopback operation that isolates the network transmitter outputs (TPTX± and FOTX±) and routes the MII transmit data to the MII receive data path. This function should only be used when autonegotiation is disabled (bit 12 = 0). The specific PHY (10Base-T or 100Base-X) used for this operation is determined by bits 12 and 13 of this register.	R/W	0h
13	Speed Selection	1—100 Mbits/s. 0—10 Mbits/s. Link speed is selected by this bit or by autonegotiation if bit 12 of this register is set (in which case, the value of this bit is ignored). At powerup or reset, this bit will be set unless AUTONEN, 100FDEN, and 100HDEN pin are all in logic low state.	R/W	Pin
12	Autonegotiation Enable	1—Enable autonegotiation process. 0—Disable autonegotiation process. This bit determines whether the link speed should be set up by the autonegotiation process. It is set at powerup or reset if the AUTONEN pin detects a logic 1 input level.	R/W	Pin
11	Powerdown	1—Powerdown. 0—Normal operation. Setting this bit puts the LU3X32FT into powerdown mode. During the powerdown mode, TX± and all LED outputs are tri-stated, FOTX± output are turned off, and the MII interface is isolated. RSTZ is used to clear register.	R/W	0h

Register Description (continued)

Table 15. Control Register (Per Port) [Register 0h] (continued)

Bit(s)	Name	Description	R/W	Default
10	Isolate	1—Isolate PHY from MII. 0—Normal operation. Setting this control bit isolates the part from the MII, with the exception of the serial management interface. When this bit is asserted, the LU3X32FT does not respond to TXD[3:0], TXEN, and TXER inputs, and it presents a high impedance on its TXCLK, RXCLK, RXDV, RXER, RXD[3:0], COL, and CRS outputs. This bit is initialized to 0 unless the configuration pins for the PHY address are set to 00000h during powerup or reset.	R/W	Pins
9	Restart Autonegotiation	1—Restart autonegotiation process. 0—Normal operation. Setting this bit while autonegotiation is enabled forces a new autonegotiation process to start. This bit is self-clearing and returns to 0 after the autonegotiation process has commenced.	R/W, SC	0h
8	Duplex Mode	1—Full-duplex mode. 0—Half-duplex mode. If autonegotiation is disabled, this bit determines the duplex mode for the link. At powerup or reset, this bit is set to 0 if the NDRPTR bit indicates REPEATER operation. Otherwise, this bit is set to 1 if AUTONEN pin detects a logic 0 and either 100FDEN or 10FDEN pin detects a logic 1.	R/W	Pin
7	Collision Test (only applicable while in PHY loopback mode)	1—Enable COL signal test. 0—Disable COL signal test. When set, this bit will cause the COL signal of MII interface to be asserted in response to the assertion of TXEN.	R/W	0h
6:0	Reserved	Not used.	RO	0h

Register Description (continued)

Table 16. Status Register Bit Definitions (Per Port) [Register 1h]

Bit(s)	Name	Description	R/W	Default
15	100Base-T4	1—Capable of 100Base-T4. 0—Not capable of 100Base-T4. This bit is hardwired to 0, indicating that the LU3X32FT does not support 100Base-T4.	RO	0h
14	100Base-X Full Duplex	1—Capable of 100Base-X full-duplex mode. 0—Not capable of 100Base-X full-duplex mode. This bit is hardwired to 0, indicating that the LU3X32FT does not support 100Base-X full-duplex mode.	RO	1h
13	100Base-X Half Duplex	1—Capable of 100Base-X half-duplex mode. 0—Not capable of 100Base-X half-duplex mode. This bit is hardwired to 1, indicating that the LU3X32FT supports 100Base-X half-duplex mode.	RO	1h
12	10 Mbits/s Full Duplex	1—Capable of 10 Mbits/s full-duplex mode. 0—Not capable of 10 Mbits/s full-duplex mode. This bit is hardwired to 0, indicating that the LU3X32FT does not support 10Base-T full-duplex mode.	RO	1h
11	10 Mbits/s Half Duplex	1—Capable of 10 Mbits/s half-duplex mode. 0—Not capable of 10 Mbits/s half-duplex mode. This bit is hardwired to 1, indicating that the LU3X32FT supports 10Base-T half-duplex mode.	RO	1h
10	100Base-T2	1—Capable of 100Base-T2. 0—Not capable of 100Base-T2. This bit is hardwired to 0, indicating that the LU3X32FT does not support 100Base-T2.	RO	0h
9:7	Reserved	Ignore when read.	RO	0h
6	MF Preamble Suppression	1—Accepts management frames with preamble suppressed. 0—Will not accept management frames with preamble suppressed. This bit is hardwired to 1, indicating that the LU3X32FT accepts management frame without preamble. A minimum of 32 preamble bits are required following power-on or hardware reset. One idle bit is required between any two management transactions as per *IEEE* 802.3u specification.	RO	1h
5	Autonegotiation Complete	1—Autonegotiation process completed. 0—Autonegotiation process not completed. If autonegotiation is enabled, this bit indicates whether the autonegotiation process has been completed.	RO	0h

Register Description (continued)

Table 16. Status Register Bit Definitions (Per Port) [Register 1h] (continued)

Bit(s)	Name	Description	R/W	Default
4	Remote Fault	1—Remote fault detected. 0—Remote fault not detected. This bit is latched to 1 if the RF bit in the autonegotiation link-partner ability register (bit 13, register address 05h) is set or the receive channel meets the far end fault indication function criteria. It is unlatched when this register is read.	RO, LH	0h
3	Autonegotiation Ability	1—Capable of autonegotiation. 0—Not capable of autonegotiation. This bit defaults to 1, indicating that LU3X32FT is capable of autonegotiation.	RO	1h
2	Link Status	1—Link is up. 0—Link is down. This bit reflects the current state of the link-test-fail state machine. Loss of a valid link causes a 0 latched into this bit. It remains 0 until this register is read by the serial management interface.	RO, LL	0h
1	Jabber Detect	1—Jabber condition detected. 0—Jabber condition not detected. During 10Base-T operation, this bit indicates the occurrence of a jabber condition. It is implemented with a latching function so that it becomes set until it is cleared by a read.	RO, LH	0h
0	Extended Capability	1—Extended register set. 0—No extended register set. This bit defaults to 1, indicating that the LU3X32FT implements extended registers.	RO	1h

Table 17. PHY Identifier (Per Port) [Register 2h]

Bit(s)	Name	Description	R/W	Default
15:0	PHY-ID[15:0]	*IEEE* Address.	RO	0043h

Table 18. PHY Identifier (Per Port) [Register 3h]

Bit(s)	Name	Description	R/W	Default
15:10	PHY-ID[15:0]	*IEEE* Address/Model No./ Rev. No. This number may change in future revisions.	RO	7421h

Register Description (continued)

Table 19. Advertisement (Per Port) [Register 4h]

Bit(s)	Name	Description	R/W	Default
15	Next Page	1—Capable of next page function. 0—Not capable of next page function. This bit is defaults to 0, indicating that LU3X32FT is not next page capable.	RO	0h
14	Reserved	Reserved.	RO	0h
13	Remote Fault	1—Remote fault has been detected. 0—No remote fault has been detected. This bit is written by serial management interface for the purpose of communicating the remote fault condition to the auto-negotiation link partner.	R/W	0h
12:10	*IEEE* Reserved	These 3 bits default to 0.	RO	0h
9	Technology Ability Field for 100Base-T4	This bit defaults to 0, indicating that the LU3X32FT does not support 100Base-T4.	RO	0h
8	Technology Ability Field for 100FDEN	Advertised ability of 100 Mbits/s full-duplex of this PHY. At powerup or reset, the logic level of 100FDEN pin is latched into this bit.	R/W	Pin
7	Technology Ability Field for 100HDEN	Advertised ability of 100 Mbits/s half-duplex of this PHY.	R/W	1h
6	Technology Ability Field for 10FDEN	Advertised ability of 10 Mbits/s full-duplex of this PHY. At powerup or reset, the logic level of 10FDEN pin is latched into this bit.	R/W	Pin
5	Technology Ability Field for 10HDEN	Advertised ability of 10 Mbits/s half-duplex of this PHY.	R/W	Pin
4:0	Selector Field	These 5 bits are hardwired to 00001h, indicating that the LU3X32FT supports *IEEE* 802.3 CSMA/CD.	RO	01h

Table 20. Autonegotiation Link Partner Ability (Per Port) [Register 5h]

Bit(s)	Name	Description	R/W	Default
15	Next Page	1—Capable of next page function. 0—Not capable of next page function.	RO	0h
14	Acknowledge	1—Link partner acknowledges reception of the ability data word. 0—Not acknowledged.	RO	0h
13	Remote Fault	1—Remote fault has been detected. 0—No remote fault has been detected.	RO	0h
12:5	Technology Ability Field	Supported technologies.	RO	0h
4:0	Selector Field	Encoding definitions.	RO	0h

Register Description (continued)

Table 21. Autonegotiation Expansion Register (Per Port) [Register 6h]

Bit(s)	Name	Description	R/W	Default
15:5	Reserved	Reserved.	RO	0h
4	Parallel Detection Fault	1—Fault has been detected. 0—No fault detected. This bit is set if the parallel detection fault state of the autonegotiation arbitration state machine is visited during the autonegotiation process. It will remain set until this register is read.	RO, LH	0h
3	Link Partner Next Page Able	1—Link partner is next page capable. 0—Link partner is not next page capable. This bit indicates whether the link partner is next page able. It is meaningful only when the autonegotiation complete bit (bit 5, register 1) is set.	RO	0h
2	Next Page Able	1—Local device is next page capable. 0—Local device is not next page capable. This bit defaults to 0 indicating that LU3X32FT is not next page able.	RO	0h
1	Page Received	1—A new page has been received. 0—No new page has been received. This bit is latched to 1 when a new link code word page has been received. This bit is automatically cleared when the autonegotiation link partner ability register (register 05h) is read by management interface.	RO, LH	0h
0	Link Partner Autonegotiation Able	1—Link partner is autonegotiation able. 0—Link partner is not autonegotiation able.	RO	0h

Table 22. Isolate Counter (Per Port) [Register 12h]

Bit(s)	Name	Description	R/W	Default
15:8	Reserved	Reserved.	RO	0h
7:0	CIM Isolate Counter	Number of times isolated since reset or read. May roll over depending on value of CSMODE bit (bit 13 of register 17h).	RO, COR	0h

Table 23. False Carrier Counter (Per Port) [Register 13h]

Bit(s)	Name	Description	R/W	Default
15:0	False Carrier Count	Number of false carrier conditions since reset or read. The counter is incremented once for each packet that has false carrier condition detected. This counter may roll over depending on value of CSMODE bit (bit 13 of register 17h).	RO, COR	0h

Register Description (continued)

Table 24. Receive Error Counter (Per Port) [Register 15h]

Bit(s)	Name	Description	R/W	Default
15:0	RX Error Count	Number of receive errors since last reset. The counter is incremented once for each packet that has receive error condition detected. This counter may roll over depending on value of the CSMODE bit (bit 13 of register 17h).	RO, COR	0h

Table 25. PHY Control/Status Register (Per Port) [Register 17h]

Bit(s)	Name	Description	R/W	Default
15	NDRPTR	1—Repeater mode. 0—Node mode. This bit determines whether LU3X32FT is operating as a node or a repeater. It is initialized to the logic level of NDRPTR pin at powerup or reset.	RO	Pin
14	FOSEL	1—Fiber mode. 0—TX mode. For 100Base-X operation, this bit determines whether LU3X32FT interfaces with the network through the internal 100Base-TX transceiver or using external fiber-optic transceiver. It is initialized to the logic level of FOSEL pin at powerup or reset.	RO	Pin
13	CSMODE	1—Counter sticks at FFFFh. 0—Counters roll over. This bit controls the operation of isolate counter, false carrier counter, and receive error counters.	R/W	0h
12	TPTXTR	1—3-state transmit pairs. 0—Normal operation. When this bit is set, the twisted-pair transmitter outputs of all four ports are tri-stated.	R/W	Pin
11	*ThunderLAN* interrupt Enable	1—MDIO *ThunderLAN* interrupt enabled. 0—MDIO *ThunderLAN* interrupt disabled. This bit enables/disables the *TI ThunderLAN* interrupt mechanism.	R/W	0h
10	MF Preamble Suppression Enable	1—MDIO preamble suppression enabled. 0—MDIO preamble suppression disabled. LU3X32FT can accept management frames without preamble as described in bit 6 of register 1h. This bit allows the user to enable or disable the preamble suppression function.	R/W	1h
9	Speed Status	1—Part is in 100 Mbits/s mode. 0—Part is in 10 Mbits/s mode. This value is not defined during the auto-negotiation period.	RO	0h

Register Description (continued)

Table 25. PHY Control/Status Register (Per Port) [Register 17h] (continued)

Bit(s)	Name	Description	R/W	Default
8	Duplex Status	1—Part is in full-duplex mode. 0—Part is in half-duplex mode. This value is not defined during the auto-negotiation period.	RO	0h
7	Activity LED On	1—LEDTX/ACTLED active on both transmit and receive. 0—LEDTX/ACTLED active on transmit only.	R/W	0h
6	LEDRX off	1—3-state LEDRX output. 0—Normal operation.	R/W	0
5	LEDTX/ACTLED off	1—3-state LEDTX/ACTLED output. 0—Normal operation.	R/W	0
4	LEDLNK off	1—3-state LEDLNK output. 0—Normal operation.	R/W	0
3	LEDCOL off	1—3-state LEDCOL output. 0—Normal operation.	R/W	0
2	LEDFD off	1—3-state LEDFD output. 0—Normal operation.	R/W	0
1	LEDSP off	1—3-state LEDSP output. 0—Normal operation.	R/W	0
0	LED Pulse Stretching Disable	1—LED pulse stretching disabled. 0—LED pulse stretching enabled. When set to 0, all LED outputs are stretched 48 ms—72 ms.	R/W	0

Register Description (continued)

Table 26. Config 100 Register (Per Port) [Register 18h]

Bit(s)	Name	Description	R/W	Default
15	BPSCR	1—Disable scrambler/descrambler. 0—Enable scrambler/descrambler. This bit is initialized to the logic level of BPSCR pin at powerup or reset.	R/W	Pin
14	BP4B5B	1—Disable 4B/5B encoder/decoder. 0—Enable 4B/5B encoder/decoder. This bit is initialized to the logic level of BP4B5B pin at powerup or reset.	R/W	Pin
13	Reserved	Reserved.	RO	0h
12	BPALIGN	1—Pass unaligned data to MII. 0—Pass aligned data to MII. This bit is initialized to the logic level of BPALIGN pin at powerup or reset.	R/W	Pin
11	Enable FEFI	1—Enable FEFI. 0—Disable FEFI. This bit enables/disables far-end fault indicator function for 100Base-FX and 10Base-T operation. It is initialized to 1 if the logic level of the FOSEL pin and the FEFI_EN/10HDEN/LEDFD pin are both high at powerup or reset. After reset, this bit is writable if and only if the FOSEL register (bit 14 of register 17h) is set.	R/W	Pin
10	Enable CIM	1—Enable CIM. 0—Disable CIM. This bit enables/disables carrier integrity monitor function for repeater operation. It is initialized to 1 only if both NDRPTR and CIMEN pins indicates logic 1 during powerup or reset.	R/W	Pin
9	Force Good Link 100	1—Force good link in 100 Mbits/s mode. 0—Normal operation.	R/W	0h
8:6	Reserved	Reserved.	RO	00
5	Accept Halt	1—Passes HALT symbols to the repeater core. 0—Normal operation.	R/W	0h
4	Load Seed	1—Loads the scrambler seed. 0—Normal operation. Setting this bit loads the user seed stored in register 19h into the 100Base-X scrambler. The content of this bit returns to 0 after the loading process is completed and no transmit is active.	R/W, SC	0h
3	Burst Mode	1—Burst mode. 0—Normal operation. Setting this bit expands the 722 µs scrambler time-out period to 2,000 µs.	R/W	0h
2:0	Reserved	Reserved.	RO	0h

Register Description (continued)

Table 27. PHY Address Register (Per Port) [Register 19h]

Bit(s)	Name	Description	R/W	Default
15:11	Reserved	Reserved.	RO	0h
10:5	User Seed	User-modifiable seed data. When the load seed bit (bit 4 of register 18h) is set, bits 10 through 0 of this register are loaded into the 100Base-X scrambler. A description is given in the symbol encoder section.	R/W	21h
4:1	PHY Address 4 Through 1	These 4 bits, together with PHY address 0, store the part address used by the serial management interface. PHY address of 00000 has the special function of isolating the part from the MII. These bits are initialized to the logic levels of PHY[4:1] pins at powerup or reset.	R/W	Pin
0	PHY Address 0	The least significant bit of PHY address. After powerup or reset, this bit is initialized to 0 for port 0 and 1 for port 1.	R/W	0/1

Table 28. Config 10 Register (Per Port) [Register 1Ah]

Bit(s)	Name	Description	R/W	Default
15	10 Mbits/s Serial Mode	1—10 Mbits/s serial mode. 0—10 Mbits/s nibble mode. During 10Base-T operation, this bit determines whether the MII will be operating in nibble mode or serial mode. It is initialized to 0h at powerup and reset unless the logic level of FOSEL pin is 0 and SER10 pin is 1.	RO	Pin
14	Force 10 Meg Good Link	1—Force 10 Mbits/s good link. 0—Normal operation.	R/W	0h
13	Reserved	Reserved.	R/W	1h
12	SQE_EN	1—Signal quality error test enabled. 0—Default SQE is disabled.	R/W	0h
11	Low Squelch Select	1—Low squelch level selected. 0—Normal squelch level selected.	R/W	0h
10	Jabber Disable	1—Jabber function disabled. 0—Normal operation.	R/W	0h
9:7	Reserved	Reserved.	RO	0h
6	Powerdown Mode	1—Powers down the PHY core completely. The part comes out of this mode after a reset is asserted and deasserted. 0—Normal operation.	R/W	0h
5:4	Reserved	Reserved.	RO	0h
3	Autopolarity Disable	1—Disable autopolarity function. 0—Enable autopolarity function.	R/W	0h
2:0	Reserved	Reserved.	RO	0h

Register Description (continued)

Table 29. Status 100 Register (Per Port) [Register 1Bh]

Bit(s)	Name	Description	R/W	Default
15	Isolate Status	1—PHY is isolated (CIM). 0—Normal operation.	RO, LH	0h
14	Reserved	Reserved.	RO	0h
13	PLL Lock Status	1—100 Mbits/s PLL locked. 0—100 Mbits/s PLL not locked.	RO	0h
12	False Carrier Status	1—False carrier detected. 0—Normal operation.	RO, LH	0h
11:0	Reserved	Reserved.	RO	0h

Table 30. Status 10 Register (Per Port) [Register 1Ch]

Bit(s)	Name	Description	R/W	Default
15	Polarity	1—Polarity of cable is swapped. 0—Polarity of cables is correct.	RO	0h
14:0	Reserved	Reserved	RO	0h

Table 31. Interrupt Mask Register (Per Port) [Register 1Dh]

Bit(s)	Name	Description	R/W	Default
15	False Carrier Status	0—Enable interrupt. 1—Disable interrupt.	R/W	0h
14	Receiver Error Counter Full	0—Enable interrupt. 1—Disable interrupt.	R/W	0h
13	Isolate Error Counter Full	0—Enable interrupt. 1—Disable interrupt.	R/W	0h
12	Remote Fault	0—Enable interrupt. 1—Disable interrupt.	R/W	0h
11	Autoneg. Complete	0—Enable interrupt. 1—Disable interrupt.	R/W	0h
10	Link Up	0—Enable interrupt. 1—Disable interrupt.	R/W	0h
9	Link Down	0—Enable interrupt. 1—Disable interrupt.	R/W	0h
8	Data Recovery 100 Lock Up	0—Enable interrupt. 1—Disable interrupt.	R/W	0h
7	Data Recovery Lock Down	0—Enable interrupt. 1—Disable interrupt.	R/W	0h
6	Reserved	Reserved.	RO	0h
5:0	Reserved	Reserved.	RO	0h

Register Description (continued)

Table 32. Interrupt Status Register (Per Port) [Register 1Eh]

Bit(s)	Name	Description	R/W	Default
15	False Carrier Counter Full	1—False carrier counter has rolled over. 0—False carrier counter has not rolled over.	RO, LH	0h
14	Receiver Error Counter Full	1—Receive error counter has rolled over. 0—Receive error counter has not rolled over.	RO, LH	0h
13	Isolate Counter Full	1—Isolate counter has rolled over. 0—Isolate counter has not rolled over.	RO, LH	0h
12	Remote Fault	1—Remote fault observed by PHY. 0—Remote fault not observed by PHY.	RO, LH	0h
11	Autonegotiation Complete	1—Autonegotiation has completed. 0—Autonegotiation has not completed.	RO, LH	0h
10	Link Up	1—Link is up. 0—No change on link status.	RO, LH	0h
9	Link Down	1—Link has gone down. 0—No change on link status.	RO, LH	0h
8	Data Recovery 100 Lock Up	1—Data recovery has locked. 0—Data recovery is not locked.	RO, LH	0h
7	Data Recovery 100 Lock Down	1—Data recovery is not locked. 0—Data recovery has locked.	RO, LH	0h
6	Reserved	Reserved.	RO	0h
5:0	Reserved	Reserved.	RO	0h

Absolute Maximum Ratings (T_A = 25 °C)

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 33. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Ambient Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{stg}	–65	150	°C
Maximum Supply Voltage	—	—	3.46	V
Voltage on MII Input Pins with Respect to Ground	—	–0.5	5.25	V
Voltage on Any Other Pin with Respect to Ground	—	–0.5	3.46	V

Table 34. Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage	—	3.135	3.3	3.46	V
Power Dissipation*:					
100 Mbits/s TX	P_D	—	—	140	mA
100 Mbits/s FX	P_D	—	—	120	mA
10 Mbits/s	P_D	—	—	150	mA
Autonegotiating	P_D	—	—	30	mA

* Power dissipations are specified at 3.3 V and 25 °C. This is the power dissipated by each port of the LU3X32FT.

Electrical Characteristics

Table 35. dc Characteristics

Parameter	Symbol	Conditions	Min	Max	Unit
Recommended Power Supply	V_{DD} V_{SS}	— —	3.0 0.0	3.8 0.0	V V
Supply Current—100Base-TX (per port)	I_{DD}	V_{DD} = 3.3 V, V_{SS} = 0.0 V Full-Duplex Traffic	—	148	mA
Supply Current—10Base-TX (per port)	I_{DD}	V_{DD} = 3.3 V, V_{SS} = 0.0 V Full-Duplex Traffic	—	156	mA
Supply Current—Autonegotiation Mode (per port)	I_{DD}	V_{DD} = 3.3 V, V_{SS} = 0.0 V No Link	—	70	mA
Supply Current—100Base-FX (per port)	I_{DD}	V_{DD} = 3.3 V, V_{SS} = 0.0 V Full-Duplex Traffic	—	120	mA
TTL Input High Voltage	V_{IH}	V_{DD} = 3.3 V, V_{SS} = 0.0 V	2.0	—	V
TTL Input Low Voltage	V_{IL}	V_{DD} = 3.3 V, V_{SS} = 0.0 V	—	0.8	V
TTL Output High-voltage MII Pins	V_{OH}	V_{DD} = 3.3 V, V_{SS} = 0.0 V	2.4	—	V
TTL Output Low-voltage MII Pins	V_{OL}	V_{DD} = 3.3 V, V_{SS} = 0.0 V	—	0.4	V
TTL Output High-voltage LED Pins	V_{OH2}	V_{DD} = 3.3 V, V_{SS} = 0.0 V I_{OH} = 10mA	3.0	—	V
TTL Output Low-voltage LED Pins	V_{OL2}	V_{DD} = 3.3 V, V_{SS} = 0.0 V I_{OH} = 10mA	—	0.3	V
PECL Input High Voltage	V_{IHPECL}	—	V_{DD}–1.16	V_{DD}–0.88	V
PECL Input Low Voltage	V_{ILPECL}	—	V_{DD}–1.81	V_{DD}–1.47	V
PECL Output High Voltage	V_{OHPECL}	—	V_{DD}–1.02		V
PECL Output Low Voltage	V_{OLPECL}	—	—	V_{DD}–1.62	V
Oscillator Input (25 MHz)	X_{IN}	—	–50	50	ppm
Input Capacitance	MII C_{IN}	—	—	8	pF

Clock Timing

Table 36. System Clock [Xin]

Symbol	Description	Min	Max	Unit
t1	Clock High Pulse Width	17	23	ns
t2	Clock Low Pulse Width	17	23	ns
t3	Clock Period	40	40	ns

Note: Specified at ±50 ppm.

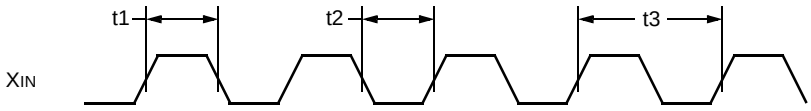

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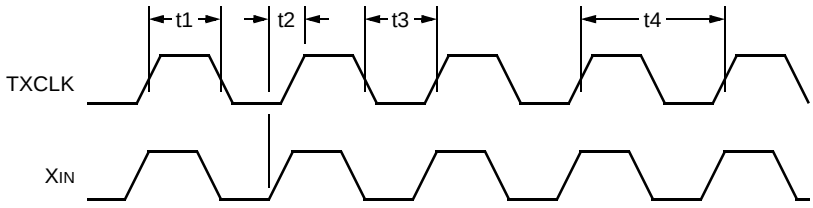
Figure 6. System Clock [XIN]

Clock Timing (continued)

Table 37. Transmit Clock (Input and Output)

Symbol	Description	Min	Max	Unit
t1	TXCLK High Pulse Width (100 Mbits/s)	14	26	ns
	TXCLK High Pulse Width (10 Mbits/s nibble)	140	260	ns
	TXCLK High Pulse Width (10 Mbits/s serial)	35	65	ns
t2	Xin Rise to TXCLK Rise (100 Mbits/s)	14	—	ns
	Xin Rise to TXCLK Rise (10 Mbits/s nibble)	28	—	ns
t3	TXCLK Low Pulse Width (100 Mbits/s)	14	26	ns
	TXCLK Low Pulse Width (10 Mbits/s nibble)	140	260	ns
	TXCLK Low Pulse Width (10 Mbits/s serial)	35	65	ns
t4	TXCLK Period (100 Mbits/s)	40	40	ns
	TXCLK Period (10 Mbits/s nibble)	400	400	ns
	TXCLK Period (10 Mbits/s serial)	100	100	ns

* Specified at ±100 ppm.



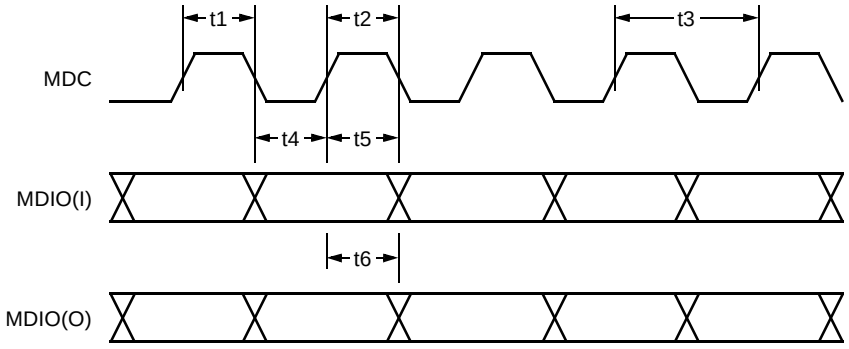
5-7913(F)

Figure 7. Transmit Clock (Input and Output)

Clock Timing (continued)

Table 38. Management Clock

Symbol	Description	Min	Max	Unit
t1	MDC High Pulse Width	200	—	ns
t2	MDC Low Pulse Width	200	—	ns
t3	MDC Period	400	—	ns
t4	MDIO(I) Setup to MDC Rising Edge	10	—	ns
t5	MDIO(I) Hold Time from MDC Rising Edge	10	—	ns
t6	MDIO(O) Valid from MDC Rising Edge	0	300	ns



5-7914(F)

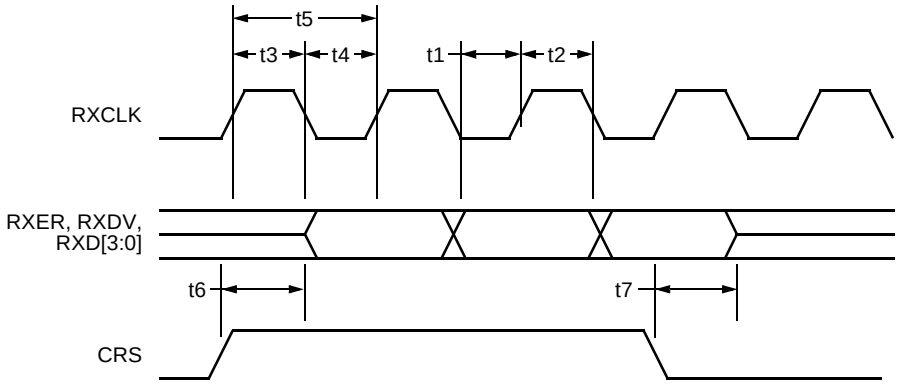
Figure 8. Management Clock

Clock Timing (continued)

Table 39. MII Receive Timing

Symbol	Description	Min	Max	Unit
t1	RXER, RXDV, RXD[3:0] Setup to RXCLK Rise	10	—	ns
t2	RXER, RXDV, RXD[3:0] hold after RXCLK Rise	10	—	ns
t3	RXCLK High Pulse Width (100 Mbits/s)	14	26	ns
	RXCLK High Pulse Width (10 Mbits/s MII)	140	260	ns
	RXCLK High Pulse Width (10 Mbits/s Serial)	35	65	ns
t4	RXCLK Low Pulse Width (100 Mbits/s)	14	26	ns
	RXCLK Low Pulse Width (10 Mbits/s MII)	140	260	ns
	RXCLK Low Pulse Width (10 Mbits/s Serial)	35	65	ns
t5	RXCLK Period (100 Mbits/s)	40	40	ns
	RXCLK Period (10 Mbits/s MII)	400	400	ns
	RXCLK Period (10 Mbits/s Serial)	100	100	ns
t6	MIIENA Assertion to RX Valid	10	50	ns
t7	MIIENA Deassertion to RX 3-state*	140	—	ns

* Load = TBD.



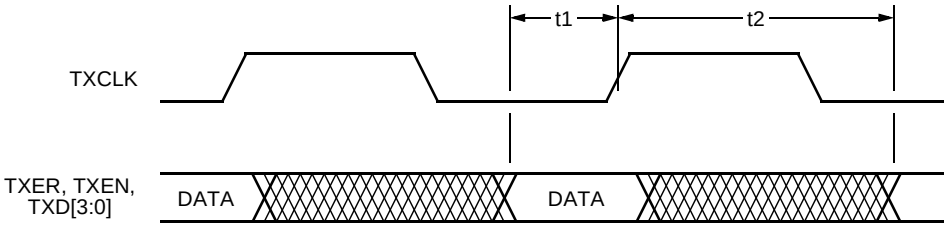
5-7915(F).a

Figure 9. MII Receive Timing

Clock Timing (continued)

Table 40. MII Transmit Timing

Symbol	Description	Min	Max	Unit
t1	TXER, TXEN, TXD[3:0] Setup to TXCLK Rise	10	—	ns
t2	TXER, TXEN, TXD[3:0] Delay after TXCLK Rise	0	25	ns



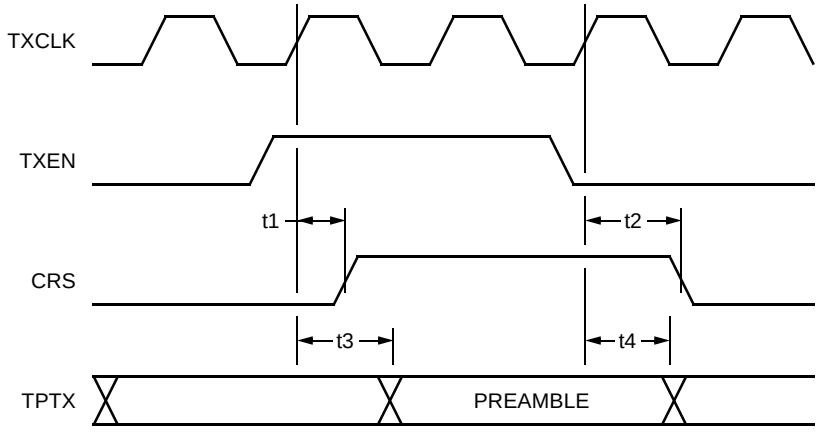
5-7916(F)

Figure 10. MII Transmit Timing

Clock Timing (continued)

Table 41. Transmit Timing

Symbol	Description	Min	Max	Unit
t1	TXEN Sampled to CRS High (100 Mbits/s)	0	4	bits
	TXEN Sampled to CRS High (10 Mbits/s)	—	1.5	bits
t2	TXEN Sampled to CRS Low (100 Mbits/s)	0	16	bits
	TXEN Sampled to CRS Low (10 Mbits/s)	—	16	bits
t3	Transmit Latency (100 Mbits/s)	6	14	bits
	Transmit Latency (10 Mbits/s)	4	—	bits
t4	Sampled TXEN Inactive to End of Frame (100 Mbits/s)	—	17	bits
	Sampled TXEN Inactive to End of Frame (10 Mbits/s)	—	5	bits



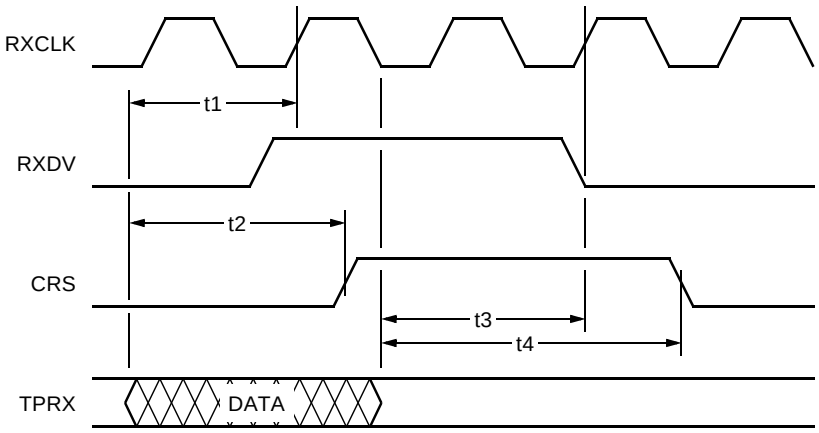
5-7917(F)

Figure 11. Transmit Timing

Clock Timing (continued)

Table 42. Receive Timing

Symbol	Description	Min	Max	Unit
t1	Receive Frame to Sampled Edge of RXDV (100 Mbits/s)	—	15	bits
	Receive Frame to Sampled Edge of RXDV (10 Mbits/s)	—	22	bits
t2	Receive Frame to CRS High (100 Mbits/s)	—	13	bits
	Receive Frame to CRS High (10 Mbits/s)	—	5	bits
t3	End of Receive Frame to Sampled Edge of RXDV (100 Mbits/s)	—	12	bits
	End Receive Frame to Sampled Edge of RXDV (10 Mbits/s)	—	4	bits
t4	End of Receive Frame to CRS Low (100 Mbits/s)	13	24	bits
	End of Receive Frame to CRS Low (10 Mbits/s)	—	4.5	bits



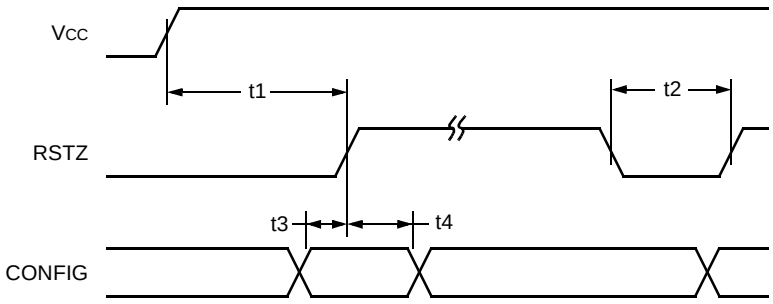
5-7918(F)

Figure 12. Receive Timing

Clock Timing (continued)

Table 43. Reset and Configuration Timing

Symbol	Description	Min	Max	Unit
t1	Power On to Reset High	0.5	—	ms
t2	Reset Pulse Width	0.5	—	ms
t3	Configuration Pin Setup	0.5	—	ms
t4	Configuration Pin Hold	0.5	—	ms



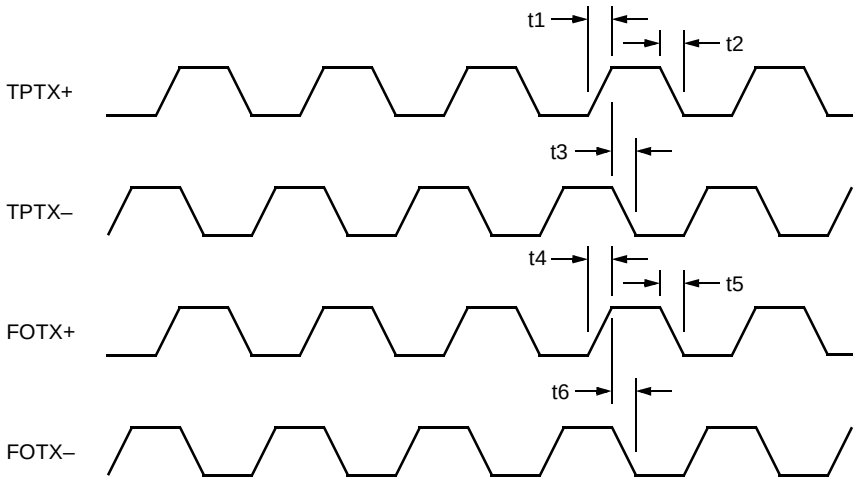
5-7919(F)

Figure 13. Reset and Configuration Timing

Clock Timing (continued)

Table 44. PMD Characteristics

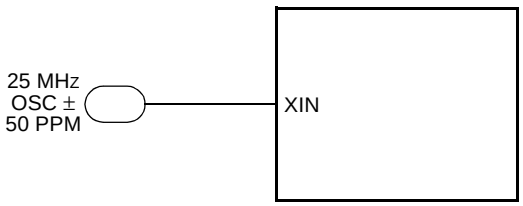
Symbol	Description	Min	Max	Unit
t1	TPTX+/TPTX– Rise Time	3.0	5.0	ns
t2	TPTX+/TPTX– Fall Time	3.0	5.0	ns
t3	TP Skew	0	500	ps
t4	FOTX+/FOTX– Rise Time	1.4	—	ns
t5	FOTX+/FOTX– Fall Time	1.4	—	ns
t6	FO Skew	0	200	ps



5-7920(F)

Figure 14. PMD Characteristics

Clock Timing (continued)



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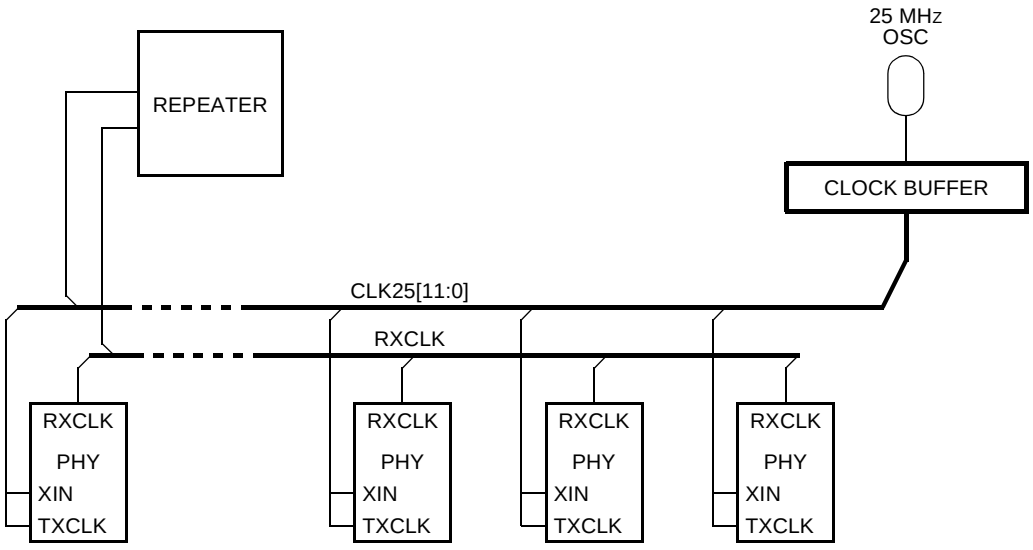

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Figure 15. Connection Diagrams (Frequency References)

Clock Timing (continued)

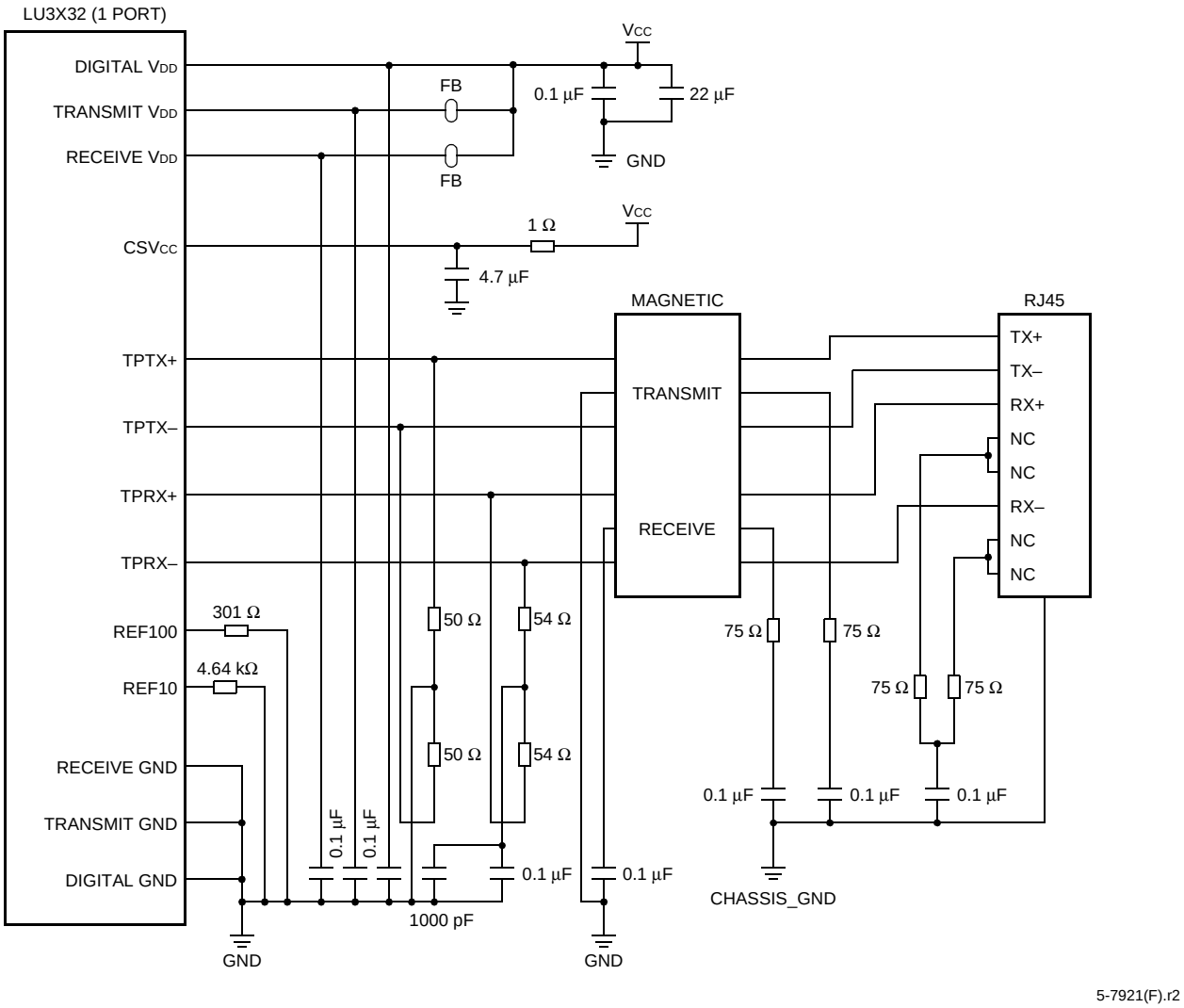
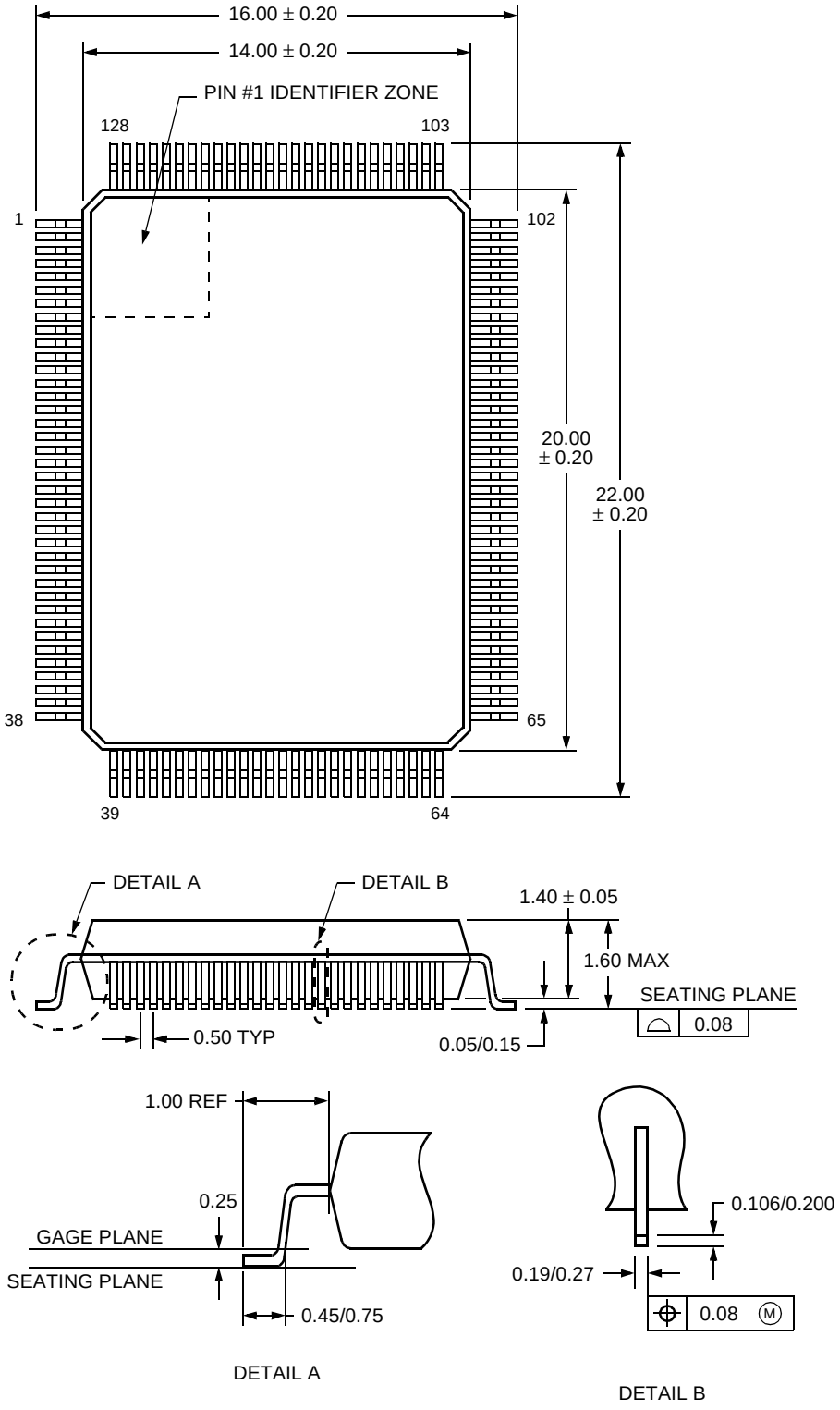


Figure 16. Connection Diagrams (10/100BTX Operation)

Outline Diagram

128-Pin TQFP

Dimensions are in millimeters.



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