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10Gb/s Multi-Protocol Processor

LiASIC 10Gb/s Multi-Protocol Processor
For SONET/SDH, POS, and 10GbE applications

Network Elements' LiASIC, the industry's first 10Gb/s multi-protocol processor, previously available only in the award-winning LiMPM module, is now available as an independent ASIC product. The LiASIC is designed to support 10Gb/s SONET/SDH OC-192/STM-64, 10Gb/s Packet-over-SONET (POS), 10 Gigabit Ethernet (10GbE) LAN, 10GbE WAN, and Ethernet-over-SONET (EOS) optical networking applications.

Network Elements' LiASIC is set apart from the competition by rich multi-protocol processing, low power dissipation (typically <7 watts), advanced packet filtering, and flexible SONET overhead processing. The LiASIC incorporates an OIF SPI-4 phase 2 interface for transferring system-side packets, an OIF SFI-4/802.3 XSBI interface for connecting to PHY modules, an 802.3 XGMII interface for connecting to PCS/PMD modules, and a 16-bit control interface.

In SONET mode, the LiASIC provides full section and line termination for concatenated or channelized streams. In POS mode, the LiASIC additionally provides PPP/HDLC encapsulation and supports packets up to 64KB. Configured for 10GbE, the LiASIC provides MAC, 64/66 PCS and WIS functionality. In all packet modes, the LiASIC offers advanced packet filtering and built-in-test features.

Innovative optical networking products provide maximum integration, speed and functionality while reducing time-to-market for networking equipment vendors.

FEATURES

- Supports SONET/SDH, POS, 10GbE LAN, 10GbE WAN, EOS
- Highly configurable
- SONET section and line termination
- Internal loopback on both line and system sides
- Hardware SONET overhead bus for insertion and capture
- Built-in data generation capabilities
- Packet counters for Ethernet, HDLC and RMON
- Software API
- 16-bit OIF SPI-4 phase 2 system interface
- 16-bit OIF SFI-4/802.3XSBI stream interface
- 32-bit 802.3 XGMII packet interface
- Glueless controller interface
- Full complement of evaluation boards (see LiMPM Toolkit)

Egress Side

- Ethernet FCS computation
- PPP/HDLC encapsulation, HDLC CRC computation
- 64/66 and EOS coding for MAC packets
- SONET framing and overhead insertion
- B1, B2, B3 processing

Ingress Side

- Powerful packet filtering capabilities
- SONET framing/mapping
- Section/line/path monitor and capture
- PPP/HDLC/POS processing
- EOS, 64/44, MAC processing

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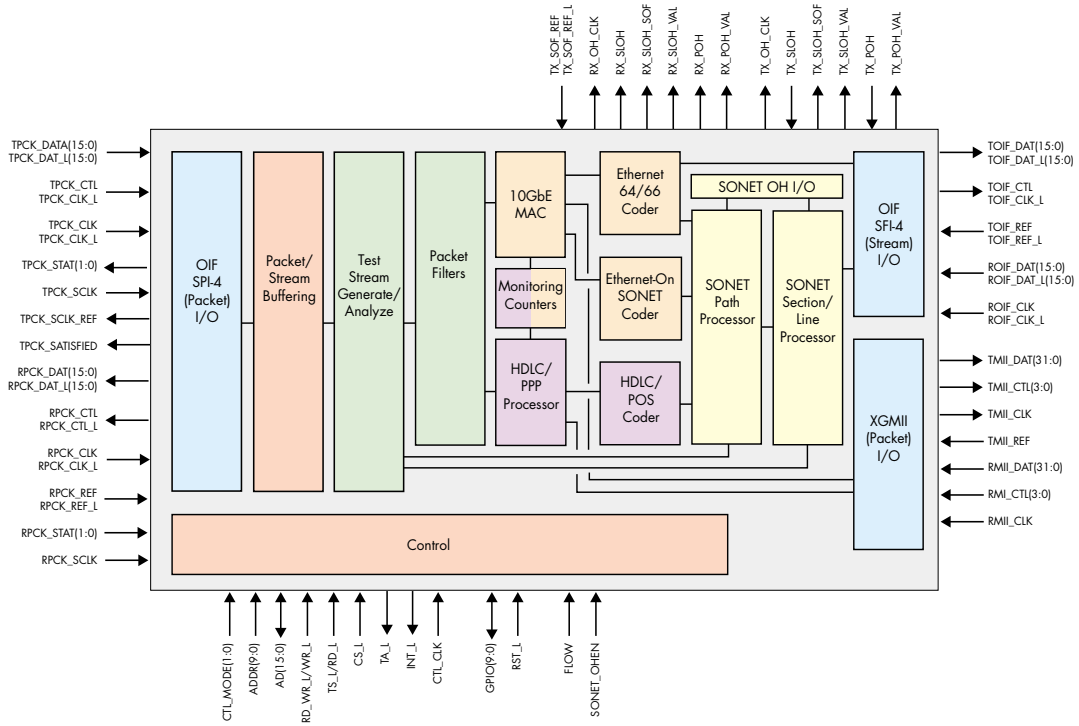
To speed the time-to-market, Network Elements offers the industry's most comprehensive Application Programming Interface (API) for use with the LiASIC. The API, written in ANSI C for maximum portability, provides a high-level interface to the ASIC's functionality, eliminating the need for designers to learn the complexities of bit-level assignments.



Network Elements' 10Gb/s LiASIC Block Diagram

About Network Elements

Network Elements is leading the drive to 10Gb/s optical networks through innovations in modular integration, high-speed optics, high-speed electronics, and wirespeed protocol processing ASICs. These products address the core, metropolitan area, edge and server markets, providing the highest levels of performance and integration. Network Elements' products enable new classes of optical networking equipment based on flexible, scalable and configurable architectures. For more information visit www.nei.com.

For More Information

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