256K x 8 Bit FLASH and 128K x 8 Bit SRAM Low Voltage Combo Memory

FEATURES

- Both FLASH and RAM in one chip
- Single Operating Voltage Range: 2.7 - 3.3V
- Fast Access Time
  - FLASH: 70 ns (Max.)
  - SRAM : 15/70 ns (Max.)
- Low Power Dissipation:
  - Standby: 30 µW (Typ.)
  - Operating: 30 mW (Typ.)
- Sector Erase Capability (4 KB sectors)
- Fast Sector Erase and Byte Program:
  - Sector Erase Time: 10 ms typical
  - Chip Erase Time: 80 ms typical
  - Byte Program Time: 10 µs typical
  - Chip Re-write Time: 3 second typical
- Fully Static Operation
- Minimum 100,000 program/erase cycle
- Three state Outputs
- JEDEC Standard 40 Pin TSOP package or 32 Pin TSOP package

GENERAL DESCRIPTION

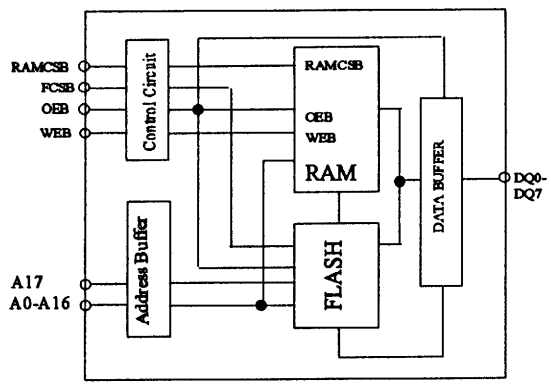
The LX59CF2010 is a combination memory chip that consists of 2 Megabit FLASH Memory organized as 256K words by 8 bits and a 1Megabit Static Random Access Memory (SRAM) organized as 128K words by 8 bits. This monolithic FLASH/SRAM combo device is totally command set compatible with the JEDEC single-power-supply FLASH standard and is packaged in JEDEC standard 40 pin TSOP.

The device is fabricated using Linvex's advanced CMOS low power process technology and SST's SUPERFLASH™ technology.

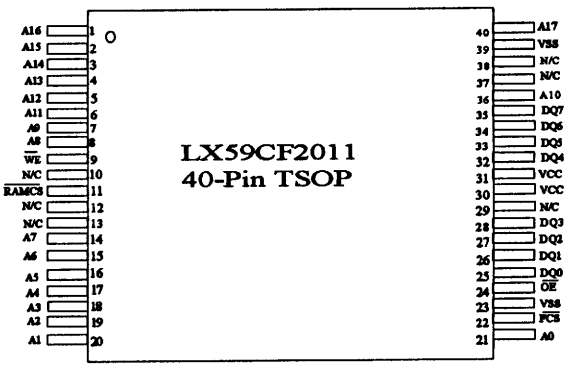
The LX59CF2010 has an output enable input for precise control of the data outputs. There are two (2) separate chip enable inputs for selection of either SRAM or FLASH and to minimize current drain in the power-down mode.

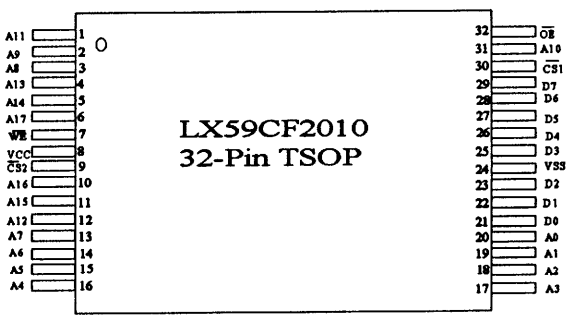
The LX59CF2010 is particularly well suited for use in low voltage (2.7 - 3.3 V) applications such as GPS, cellular phones, PDA, and other handheld applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)





Pin Name	Pin Function
A_0 - A_{17}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{CS}$ 1/FCSB	FLASH Chip Enable Input
$\overline{CS}$ 2/RAMCSB	RAM Chip Enable Input
DQ0-DQ7	Data Inputs / Outputs
V_{DD}	Power (2.7 V - 3.3 V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	-0.5 to V_{CC} +0.5	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 to 4.0	V
Power Dissipation (package capability)	P_D	1.0	W
Storage Temperature	T_{stg}	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{solder}	240 °C, 3 sec (Lead Only)	-
Short Circuit Current	I_{OS}	50	mA

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A = 0 TO 70 °C)

Item	Symbol	Min.	Max.	Unit
Supply Voltage	V_{DD}	2.7	3.3	V
Ground	V_{SS}	0	0	V
Input High Voltage	V_{IH}	2.2	V_{DD} + 0.5	V
Input Low Voltage	V_{IL}	-0.3	0.3	V

DC AND OPERATING CHARACTERISTICS (Ta = 0 to 70 °C)

Item	Symbol	Test Conditions	VCC=3.0V ± 0.3		Units
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{DD}	-1	1	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ =V_{IH} or $\overline{OE}$ =V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$=V_{SS} to V_{DD}	-1	1	µA
FLASH Operating Supply Current	I_{CC1}	$\overline{CS}$ 1=V_{IL}, $\overline{CS}$ 2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, $I_{I/O}$=0 mA	-	15.00 + 1.1(f)	mA
RAM Operating Current	I_{CC2}	$\overline{CS}$ 1=V_{IH}, $\overline{CS}$ 2=V_{IL}, $I_{I/O}$=0 mA	-	5.0 + 1(f)	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ ≥ V_{DD}-0.2V V_{IN} ≤ 0.2V, V_{IN} ≥ V_{DD}-0.2V	-	30	µA
Output Low Voltage	V_{OL}	I_{OL}= 0.1 mA at 3.3 V		0.4	V
Output High Voltage	V_{OH}	I_{OH}= -0.1 mA at 3.3 V	2.2	-	V
High Voltage for A_9	VH	$\overline{CS}$ = $\overline{OE}$ =V_{IL}, $\overline{WE}$ =V_{IH}	11.4	12.6	V
High Current for A_9	IH	$\overline{CS}$ = $\overline{OE}$ =V_{IL}, $\overline{WE}$ =V_{IH}, A_9=V_{HMAX}		200	µA

NOTE: $\overline{CS}$ = $\overline{CS}$ 1 & $\overline{CS}$ 2, $\overline{CS}$ 1 = FLASHCSB, $\overline{CS}$ 2 = RAMCSB, f=1/cycle time (MH_Z).

CAPACITANCE *(f=1MHz, Ta = 25 °C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input / Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	12	pF

TEST CONDITIONS (Ta= 0 TO 70 °C)

Parameter	Value
	V_{DD} = 3.0 V
Input Pulse Level	0 to 3V
Input Rise and Fall Time (10% to 90% V_{DD})	5 ns

CL=35pF*

Output Load

C_L*

*: Including scope and jig capacitance

1. SRAM Operation (CS1 = ECSB = VIH)

READ CYCLE

V_{DD}=3.0 V ± 0.3 Worse Case		Unit
Min	Max	
15		ns
	15	ns
	15	ns
	7	ns
3		ns
3		ns
0	7	ns
0	7	ns
3		ns

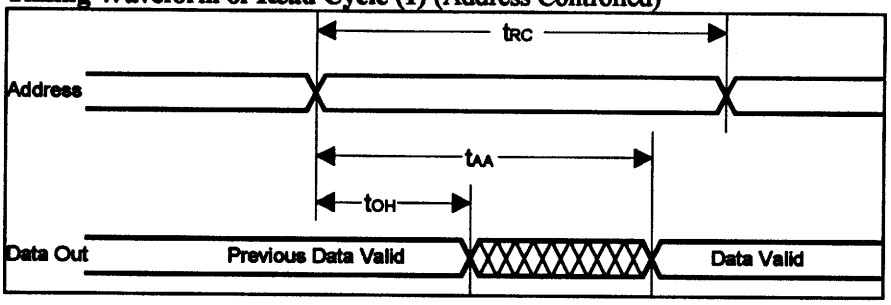
Parameter	Symbol
Read Cycle Time	t_{RC}
Address Access Time	t_{AA}
Chip Select to Output	t_{CO}
Output Enable to Valid Output	t_{OE}
Chip Select to Low-Z Output	t_{LZ}
Output Enable to Low-Z Output	t_{OLZ}
Chip Disable to High-Z Output	t_{HZ}
Output Disable to High-Z Output	t_{OHZ}
Output Hold from Address Change	t_{OH}

WRITE CYCLE

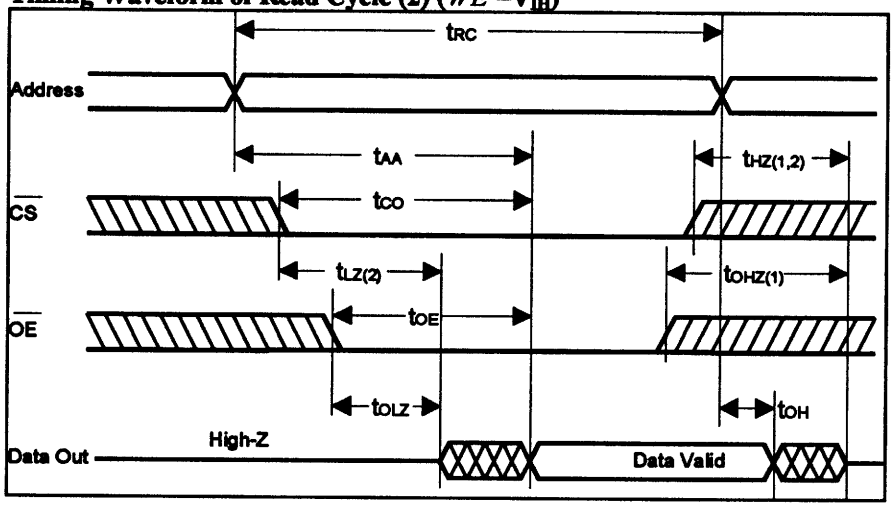
Parameter	Symbol	V_{CC}=3.0V± 0.3		Unit
		Min	Max	
Write Cycle Time	t_{WC}	15		ns
Chip Select to End of Write	t_{CW}	12		ns
Address Valid to End of Write	t_{AW}	12		ns
Address Set-up Time	t_{AS}	0		ns
Write Pulse Width	t_{WP}	12		ns
Write Recovery Time	t_{WR}	0		ns
Write to Output High-Z	t_{WHZ}	0	7	ns
Data to Write Time Overlap	t_{DW}	8		ns
Data Hold from Write Time	t_{DH}	0		ns
End Write to Output Low-Z	t_{OW}	3		ns

TIMING DIAGRAMS

Timing Waveform of Read Cycle (1) (Address Controlled)



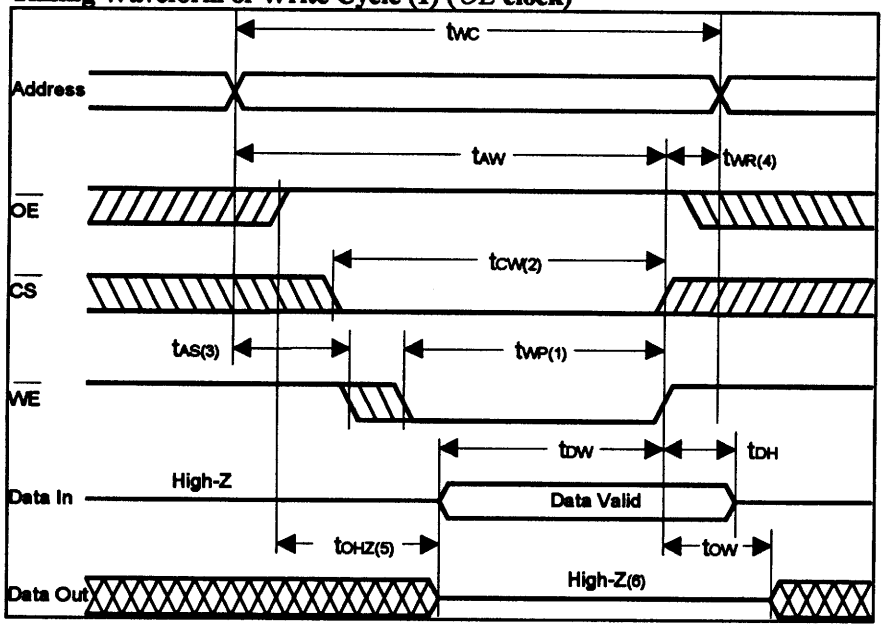
Timing Waveform of Read Cycle (2) ($\overline{WE}$ =V_{IH})



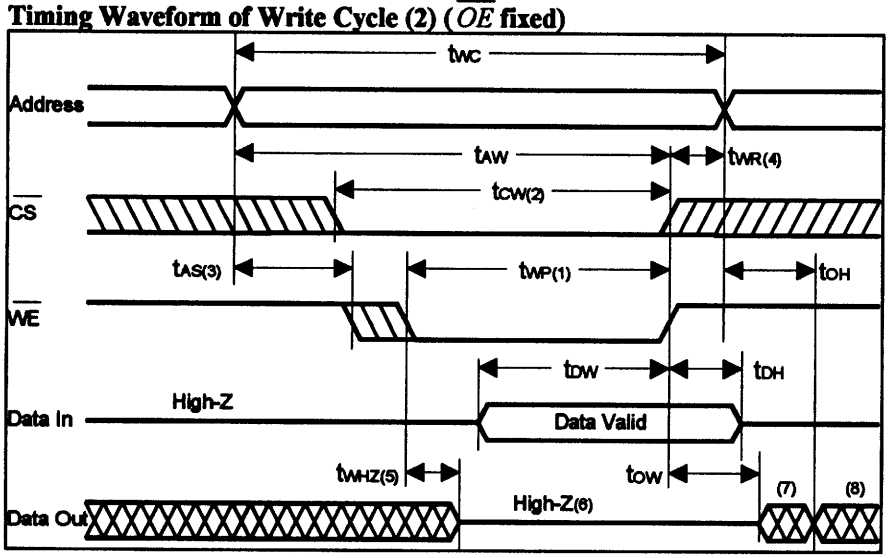
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are referenced to the V_{OH} or V_{OL}.
2. At any given temperature and voltage condition t_{HZ}(max) is less than t_{LZ}(min) both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.
4. Address valid prior to or coincident with $\overline{CS}$ 2 transition Low.

Timing Waveform of Write Cycle (1) ($\overline{OE}$ clock)



Timing Waveform of Write Cycle (2) ($\overline{OE}$ fixed)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ 2 and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ 2 going low and $\overline{WE}$ going low: A write end at the earliest transition among $\overline{CS}$ 2 going high and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS}$ 2 going low to end of write.
3. t_{AS} is measured from address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
5. if $\overline{OE}$, $\overline{WE}$ are in the read mode during this period, the I/O pins are in the outputs Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS}$ 2 goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
7. D_{OUT} is the same phase of the latest written data in this write cycle.
8. D_{OUT} is the read data of new address
9. $\overline{CS}$ 1= FCSB = V_{IH}

II. FLASH Operation ($\overline{CS}_2$ = RAMCSB = VIH)

HARDWARE AND SOFTWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the LX59CF2010 in the following ways: (a) V_{DD} sense— if V_{DD} is below 2.0V (typical), the Erase/Program functions are inhibited. (b) Erase/ Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CS}1$ high or $\overline{WE}$ high inhibits Erase/Program cycles. (c) Noise filter— pulses of less than 5ns (typical) on the $\overline{WE}$ or $\overline{CS}1$ inputs will not initiate a program cycle. (d) After power up the device is in the read mode.

The LX59CF2010 will default to software data protection after power up. A sequence of three (3) byte-loads is used to initiate the program operation, providing optimum protection from inadvertent Write Operations. Any Erase Operation require a sequence of six (6) byte loads. See table 2 for the specified software command codes.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm. In addition, users may wish to use the software product identification mode to identify the part (i.e., using the device code), and have the system software use the appropriate sector size for erase operations. In this manner, the user can have a common board design for 2 Meg to 32 megabit densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size. For details, see Operating Modes (for hardware operation) or Software Product Identification.

BYTE PROGRAM: The LX59CF2010 device is programmed on a byte-by-byte basis. The Program operation consists of three steps. The first step is the three-byte-load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte Program operation, the addresses are latched on the falling edge of eithe $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched on the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. The third step is the internal program operation which is initiated after the rising edge of the fourth $\overline{CE}$ or $\overline{WE}$, whichever occurs first. The Program operation, once intiated, will be completed within 10 μs.

SECTOR ERASE: The Sector Erase mode allows the system to erase the device on a sector by sector basis. The sector architecture is based on uniform sector size of 4KB. The Sector Erase mode is initiated by executing a six-byte-command load sequence for software data protection with sector erase command (30H) and sector address (SA) in the last bus cycle. The end of Erase can be determined using WAIT T_{SE}, or $\overline{Data}$ Polling, or Toggle Bit.

$\overline{DATA}$ POLLING (DQ7) : The LX59CF2010 features $\overline{DATA}$ polling to indicate the end of a erase/program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on DQ7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT (DQ6) : In addition to $\overline{DATA}$ polling the LX59CF2010 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in DQ6 toggling between one and zero. Once the program cycle has completed, DQ6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

CHIP ERASE MODES: The entire device may be erased (i.e., to the "1" state) by executing a 6-byte software code for easy operation. The Erase Operation begins with the rising edge of the sixth $\overline{WE}$ or $\overline{CS}1$, whichever occurs first. During the Erase Operation, the only valid read is Toggle Bit or $\overline{Data}$ Polling. Any commands written during the chip Erase Mode will be ignored.

Table 1: Operation Modes Selection

Mode	$\overline{CS1}$	$\overline{OE}$	$\overline{WE}$	A_9	D/Q	Address
Read	V_{IL}	V_{IL}	V_{IH}	A_{IN}	D_{out}	A_{IN}
Byte Program	V_{IL}	V_{IH}	V_{IL}	A_{IN}	D_{IN}	A_{IN}, See Table 2
Sector Erase	V_{IL}	V_{IH}	V_{IL}	A_{IN}	X	A_{IN}, See Table 2
Standby	V_{IH}	X	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	X	High Z/ D_{out}	X
Write Inhibit	X	X	V_{IH}	X	High Z/ D_{out}	X
Chip Erase	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}	See Table 2
Product Identification Hardware Mode	V_{IL}	V_{IL}	V_{IH}	V_H	Manufacturer Code (54H)	A_{19}-A_1=V_{IL}, A_0=V_{IL}
					Device Code (F2H)	A_{19}-A_1=V_{IL}, A_0=V_{IH}
Software Mode	V_{IL}	V_{IL}	V_{IH}	A_{IN}		See Table 2

Table 2: Software Command Summary

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr(1)	Data	Addr(1)	Data	Addr(1)	Data	Addr(1)	Data	Addr(1)	Data	Addr(1)	Data
Byte Program	5555H	AAH	2AAH	55H	5555H	A0H	BA(3)	Data				
Sector Erase	5555H	AAH	2AAH	55H	5555H	80H	5555H	AAH	2AAH	55H	SA_X(2)	30H
Chip Eraase	5555H	AAH	2AAH	55H	5555H	80H	5555H	AAH	2AAH	55H	5555H	10H
Software ID Entry	5555H	AAH	2AAH	55H	5555H	90H						
Software ID Exit	XXH	F0H	(4)									
Software ID Exit	5555H	AAH	2AAH	55H	5555H	F0H	(4)					

Notes:

(1) Address format A_{14}-A_0 (Hex), Addresses A_{15} and A_{17} are a "Don't Care" for the command sequence.

(2) SA_X for sector erase; uses A_{18}-A_{12} address lines

(3) BA = Program Byte address

(4) Both Software ID Exit operations are equivalent

(5) $\overline{CE}$=$\overline{CS1}$=$\overline{FCS}$

Notes for Software ID Entry Command Sequence

(1) With A_{18}-A_1=0; LTC Manufacturer Code = 54H, is read with A_0=0, LX59CF2010 Device Code=F2H, is read with A0=1.

(2) The device does not remain in Software Product ID Mode if powered down.

Table 3: Recommended System Power-Up Timings

Symbol	Parameter	Maximum	Units
T_{PU}-READ(1)	Power-up to Read Operation	100	µs
T_{PU}-WRITE(1)	Power-up to Write Operation	5	ms

Table 4: Reliability Characteristics

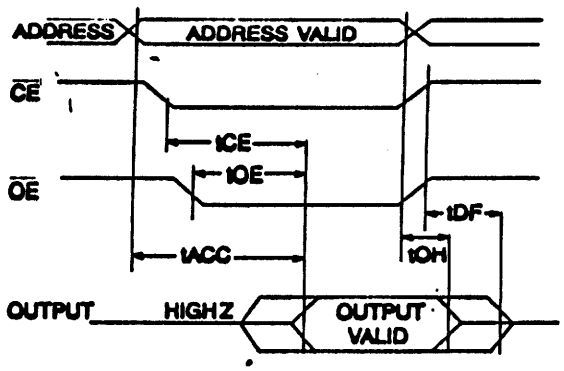
Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}(1)	Endurance	10,000	Cycles	MIL-STD-883, Method 1033
T_{DR}(1)	Data Retention	100	Years	JEDEC Standard A103
V_{ZAP}_HBM(1)	ESD Susceptibility Human Body Model	2000	Volts	JEDEC Standard A114
V_{ZAP}_MM(1)	ESD Susceptibility Machine Model	300	Volts	JEDEC Standard A115
I_{LTH}(1)	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

Note: (1) This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC Read Characteristics

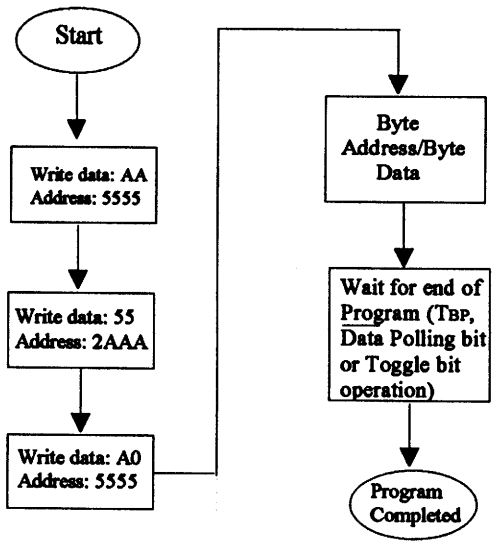
Symbol	Parameter	Min	Max	Units
t_{ACC}	Address to Output Delay		70	ns
t_{CE}	$\overline{CE}$ to Output Delay		70	ns
t_{OE} (1)	$\overline{OE}$ to Output Delay	0	50	ns
t_{DF} (2)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	30	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		ns

AC Read Waveforms



Notes: 1. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC}-t_{OE} after an address change without impact on t_{ACC}.
2. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

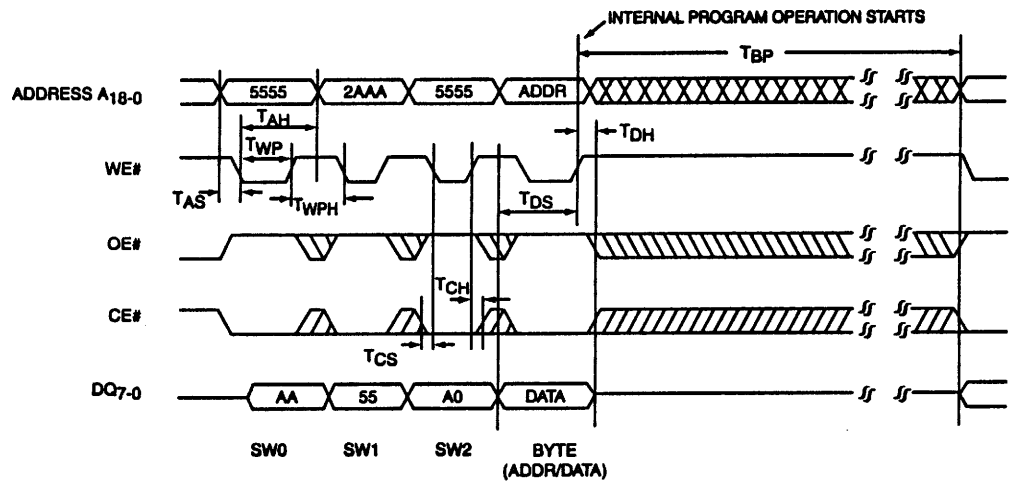
BYTE PROGRAM ALGORITHM



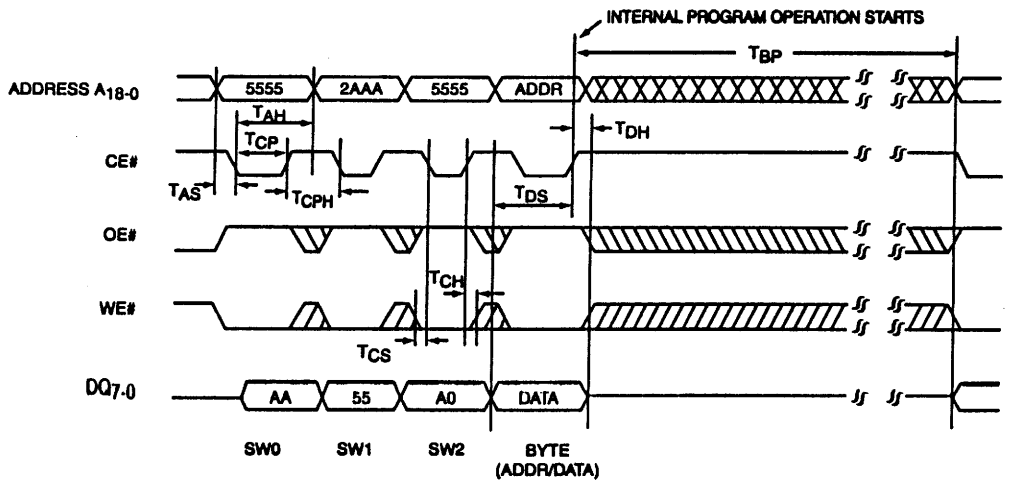
AC Program/Erase Cycle

Symbol	Parameter	Min	Max	Units
T_{BP}	Byte Program time		20	µs
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	40		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	0		ns
T_{CP}	CE# Pulse Width	60		ns
T_{WP}	WE# Pulse Width	60		ns
T_{WPH}	WE# Pulse Width High	40		ns
T_{CPH}	CE# Pulse Width High	40		ns
T_{DS}	Data Setup Time	40		ns
T_{DH}	Data Hold Time	0		ns
T_{IDA}	Software ID Access and Exit Time		150	ns
T_{SE}	Sector Erase		25	ms
T_{SCE}	Chip Erase		100	ms

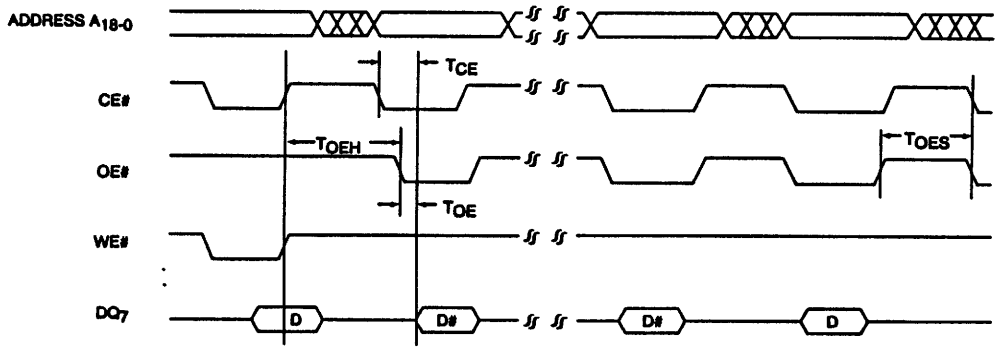
$\overline{WE}$ CONTROLLED PROGRAM CYCLE TIMING DIAGRAM



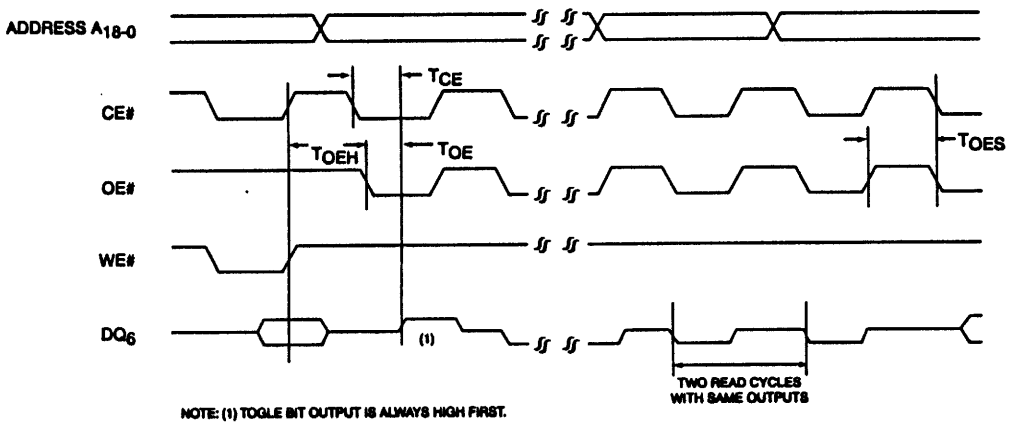
$\overline{CE}$ CONTROLLED PROGRAM CYCLE TIMING DIAGRAM



DATA POLLING TIMING DIAGRAM

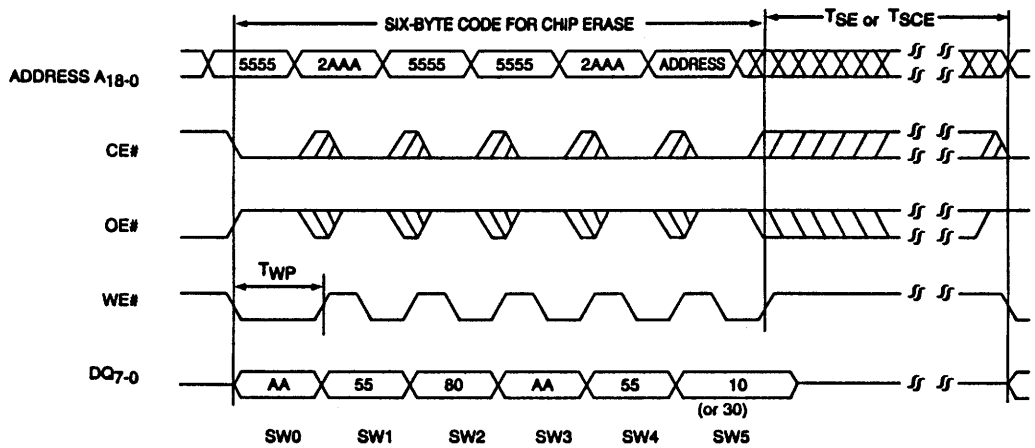


TOGGLE BIT TIMING DIAGRAM



NOTE: (1) TOGLE BIT OUTPUT IS ALWAYS HIGH FIRST.

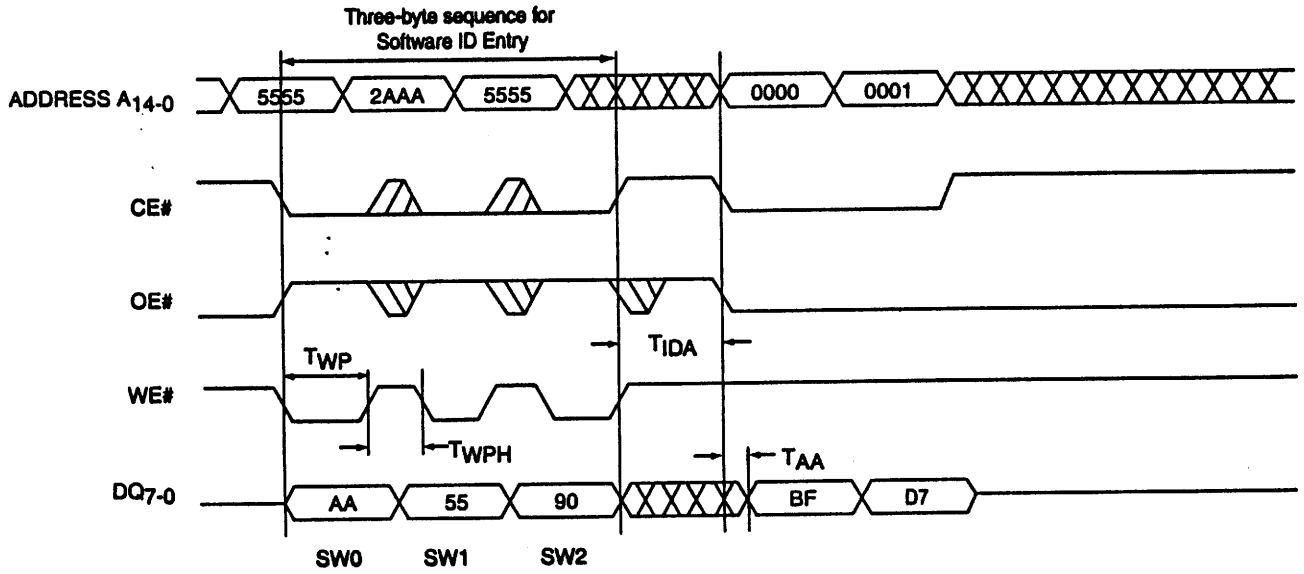
ERASE TIMING DIAGRAM



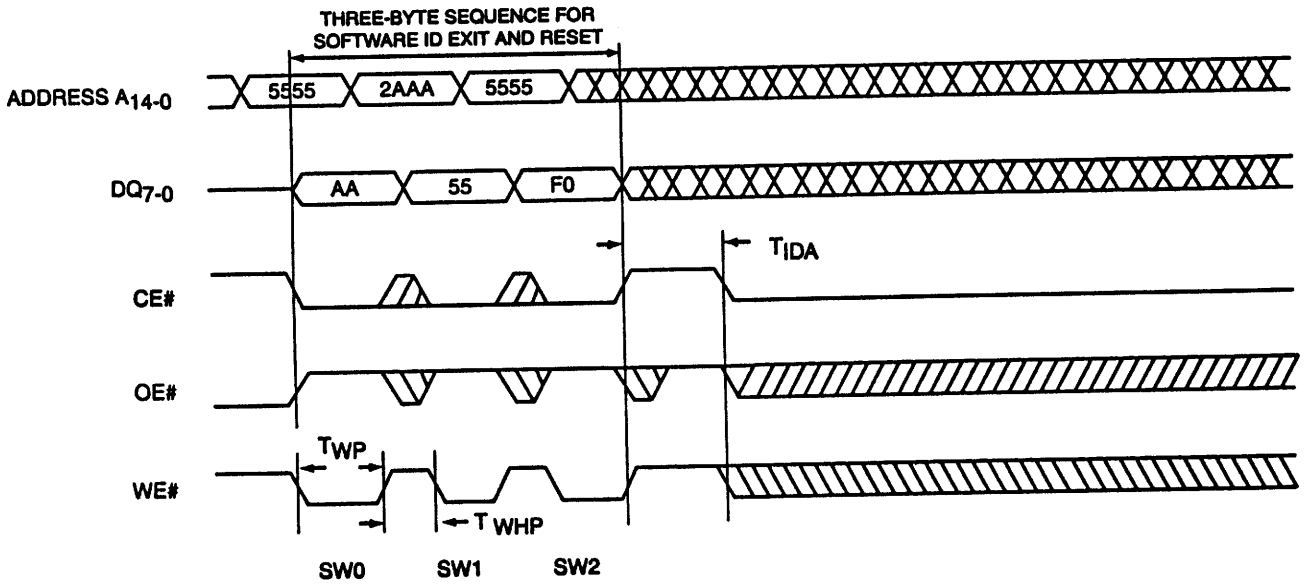
NOTE: 10H FOR CHIP ERASE
30H FOR SECTOR ERASE

ADDRESS: 5555H FOR CHIP ERASE
SECTOR ADDRESS (SA_X) FOR SECTOR ERASE

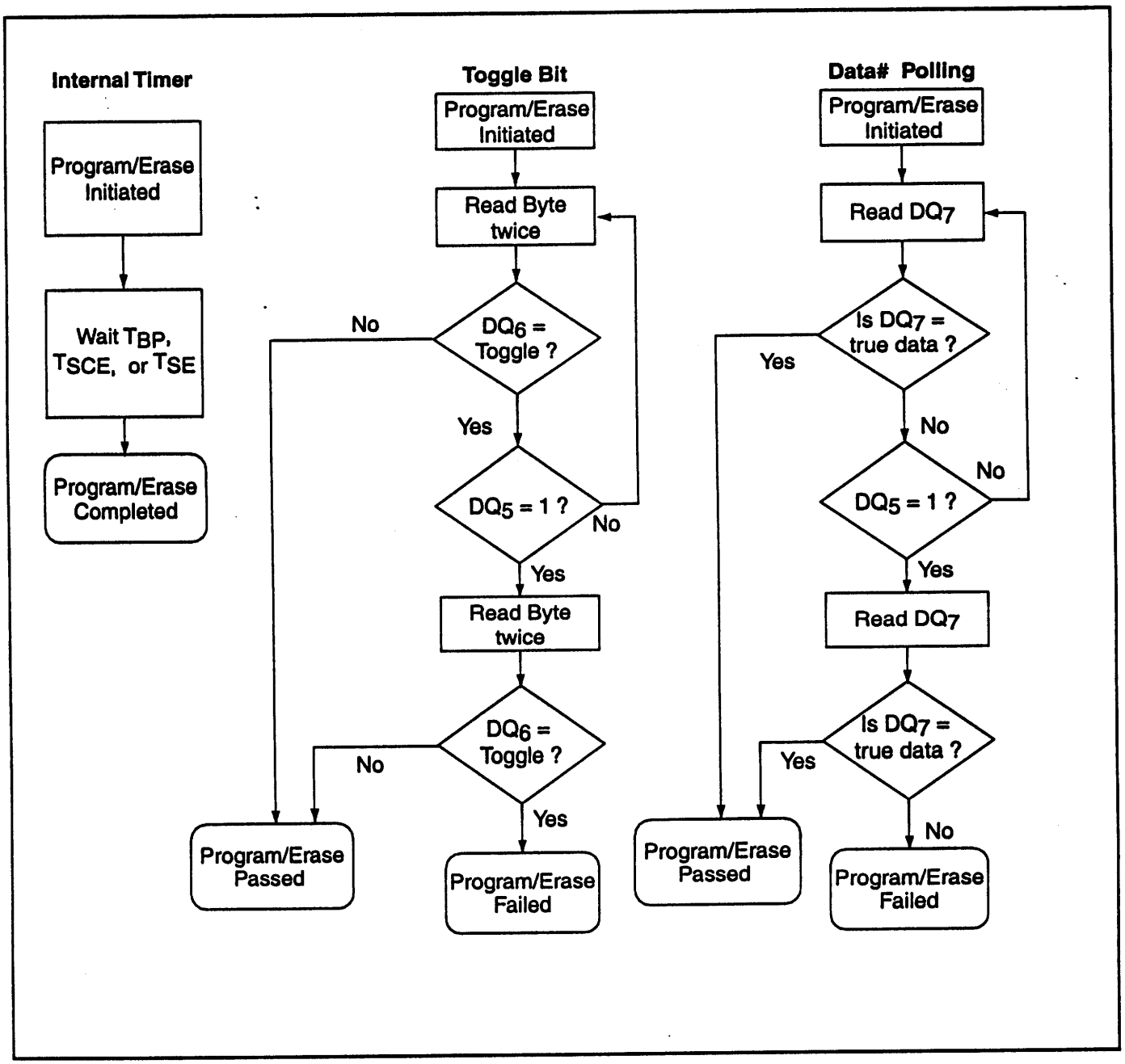
SOFTWARE ID ENTRY AND READ



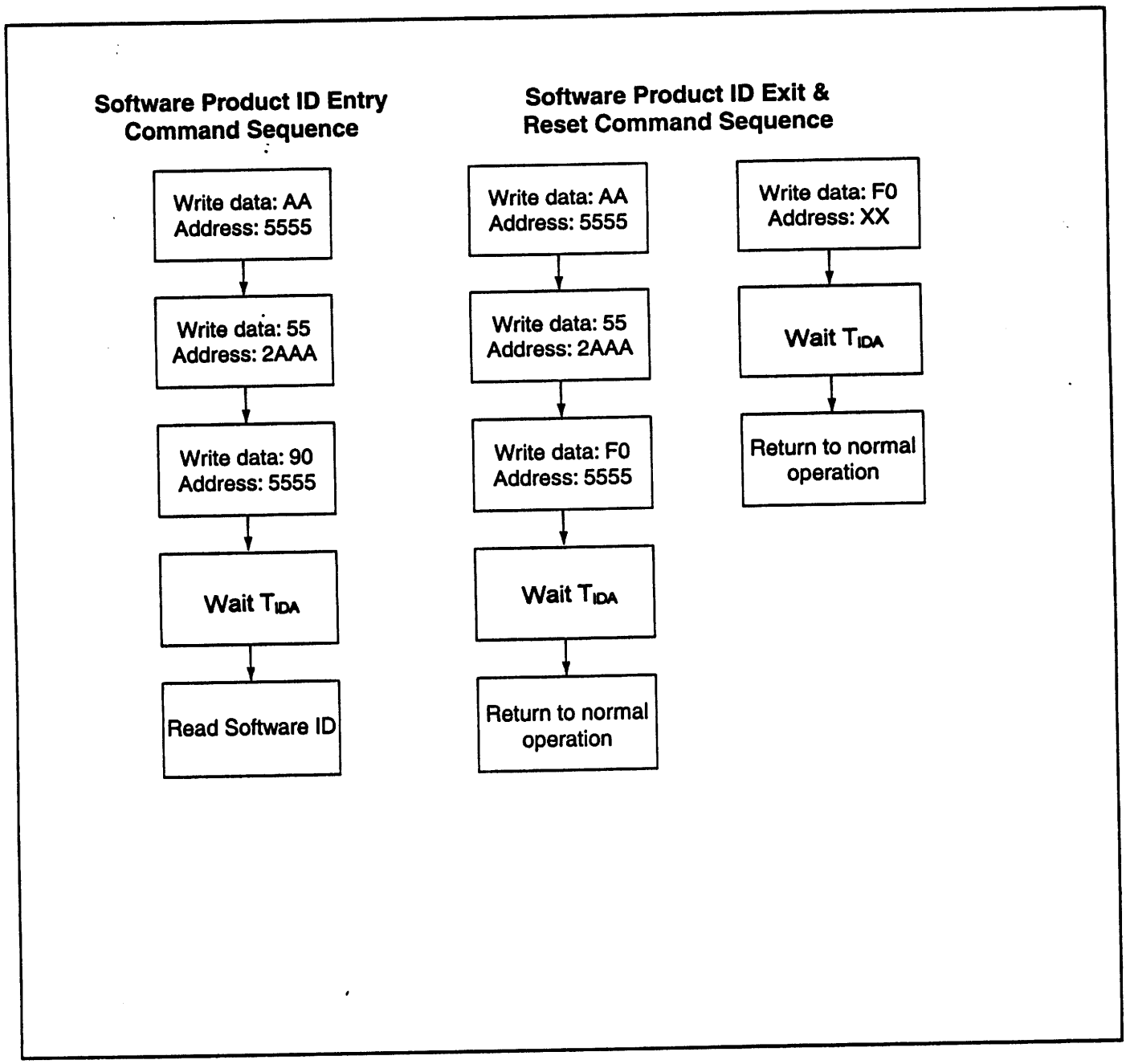
SOFTWARE ID EXIT AND RESET



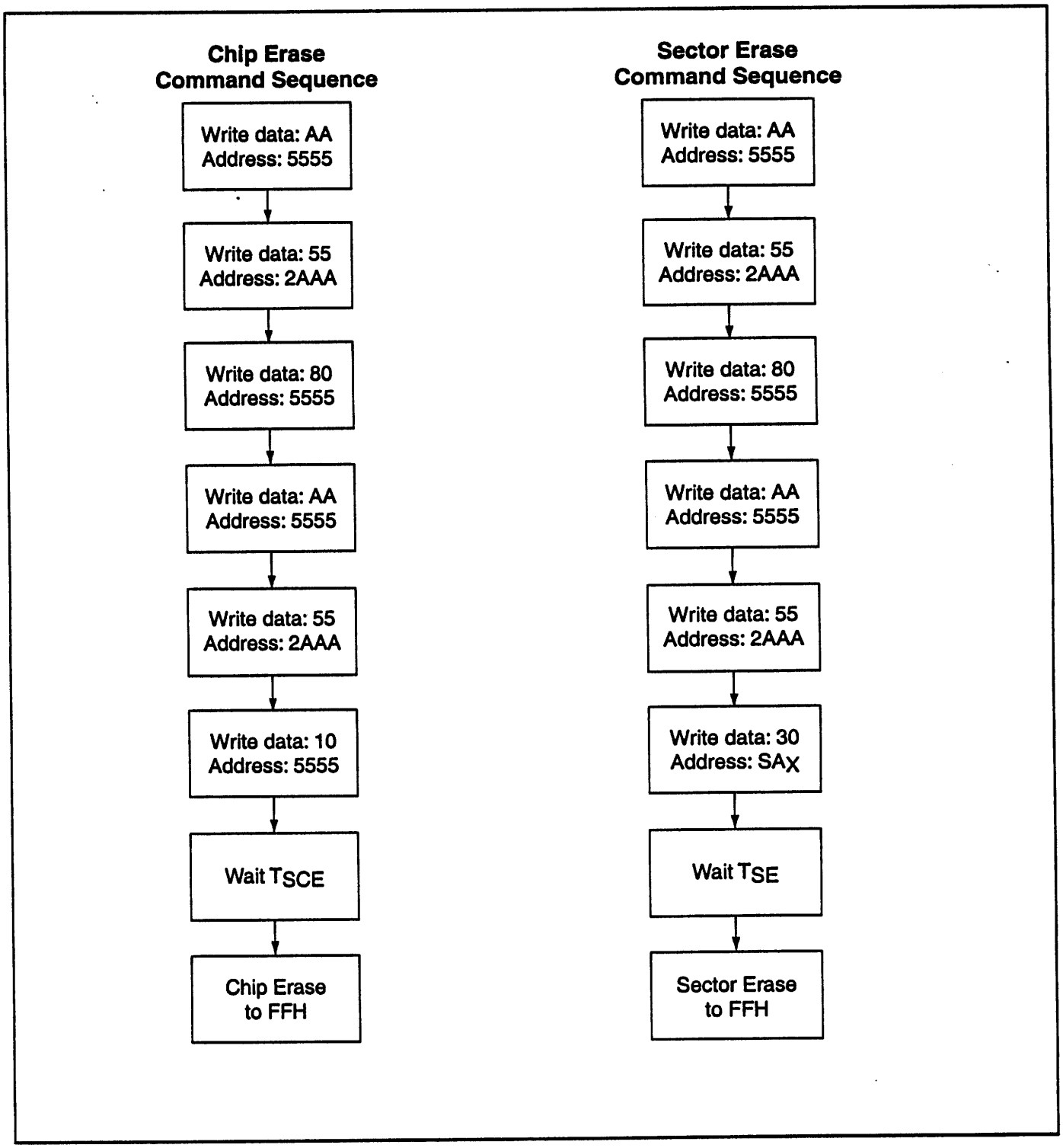
WAIT OPTIONS



SOFTWARE PRODUCT COMMAND FLOWCHARTS



ERASE COMMAND SEQUENCE



Functional Description/Truth Table (40 Pin TSOP)

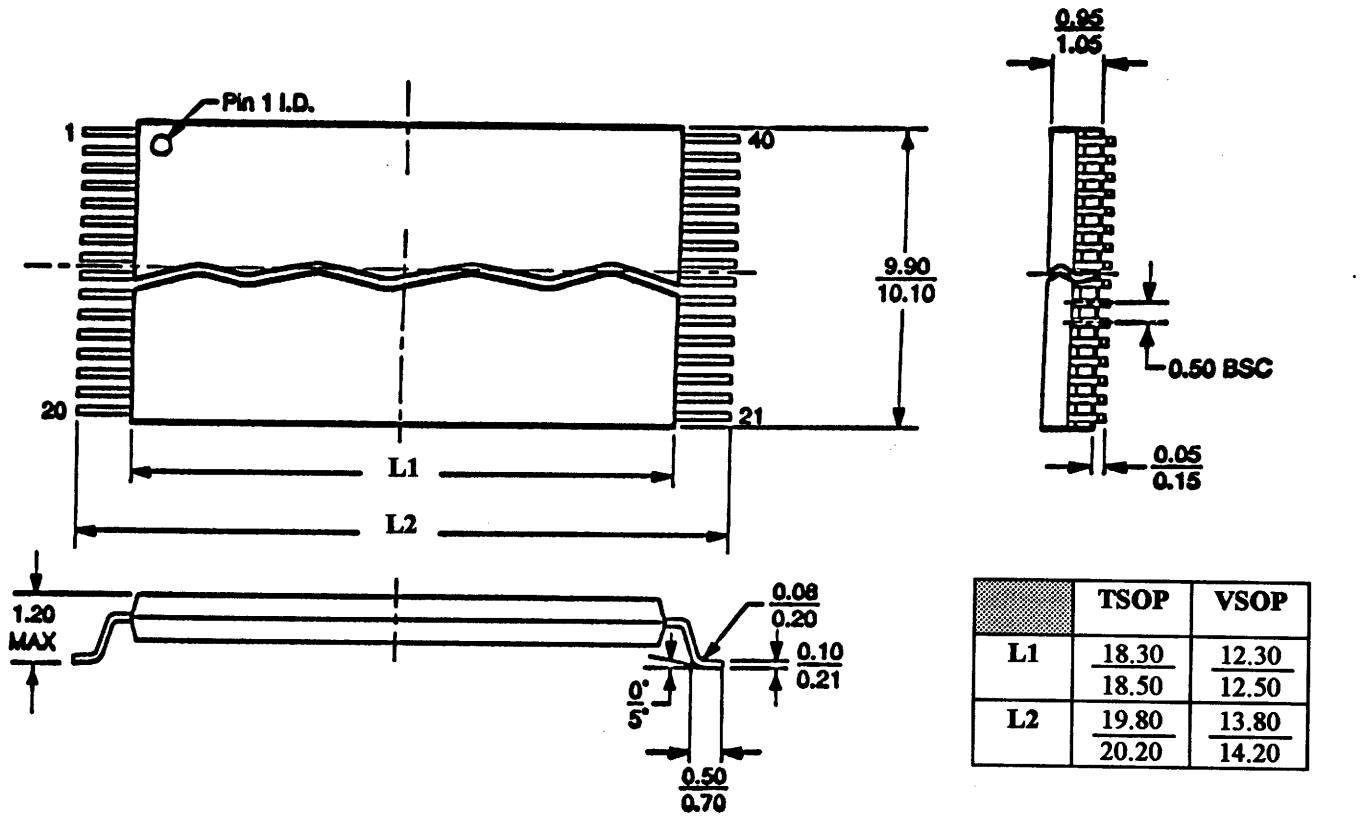
A0-A19	FCSB PIN22	RAMCSB PIN11	$\overline{WE}$	$\overline{OE}$	D0-D7	
X	H	H	X	X	Z	Standby
A0-A17	L	H	X	H	Z	Output Floating
A0-A17	L	H	X	L	Dout	FLASH read
A0-A17	L	H	L	H	Din	FLASH write
Only A0-A16 are vaild *	H	L	X	H	Z	Output Floating
Only A0-A16 are vaild *	H	L	H	L	Dout	RAM read
Only A0-A16 are vaild *	H	L	L	X	Din	RAM write

*A17 must be fixed to "L" or "H"

Note: (1) It is forbidden that FCSB pin and RAMCSB pin will be "0" at same time.
(2) X means Don't Care.
(3) Flash write must follow "Flash" write procedures. (See AC Program/Erase Cycle Characteristic)

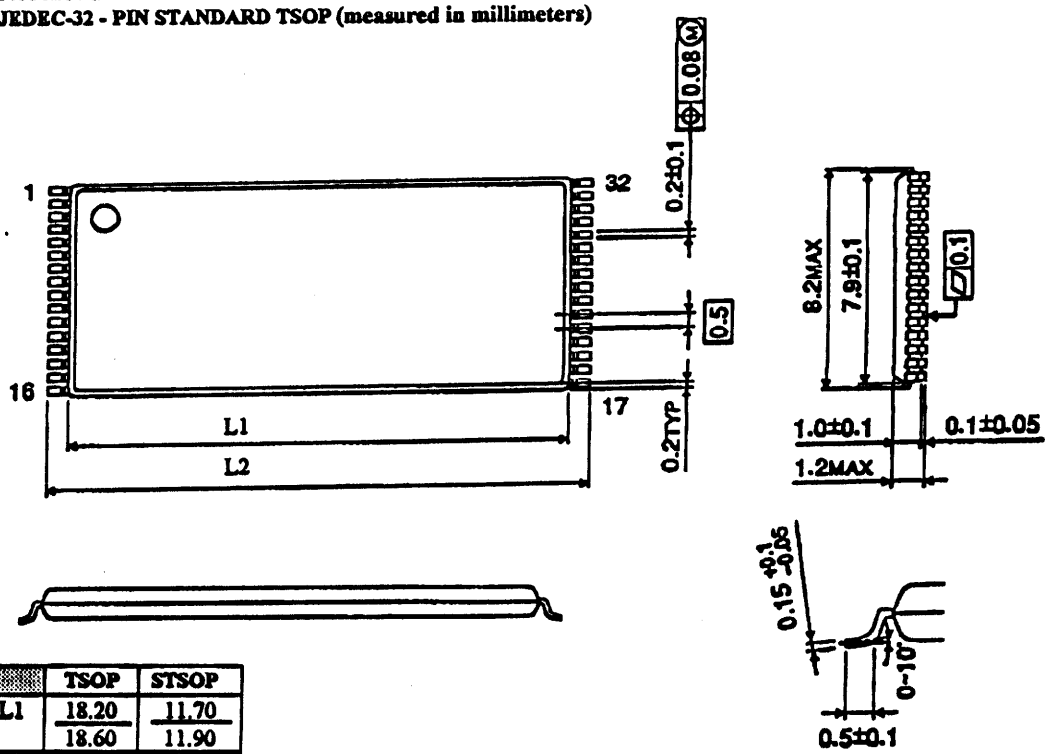
PACKAGE OUTLINES AND DIMENSIONS

JEDEC- 40-PIN STANDARD TSOP (measured in millimeters)



	TSOP	VSOP
L1	18.30 / 18.50	12.30 / 12.50
L2	19.80 / 20.20	13.80 / 14.20

PACKAGE OUTLINES AND DIMENSIONS
JEDEC-32 - PIN STANDARD TSOP (measured in millimeters)



	TSOP	STSOP
L1	18.20 / 18.60	11.70 / 11.90
L2	19.80 / 20.20	13.20 / 13.60

JEDEC-32-PIN STANDARD PLCC (measured in millimeters)

ITEM	MILLIMETERS	INCHES
A	12.44 ± .13	.490 ± .005
B	11.50 ± .13	.453 ± .005
C	14.04 ± .13	.553 ± .005
D	14.98 ± .13	.590 ± .005
E	1.93	.076
F	3.30 ± .25	.130 ± .010
G	2.03 ± .13	.080 ± .005
H	.51 ± .13	.020 ± .005
I	1.27 [Typ.]	.050 [Typ.]
J	.71 [REF]	.028 [REF]
K	.46 [REF]	.018 [REF]
L	10.40/12.94	.410/.510
	(W) (L)	(W) (L)
M	.89R	.035R
N	.25[Typ.]	.010[Typ.]

NOTE: Each lead centerline is located within .25mm[.01 inch] of its true position [TP] at a maximum at maximum material condition.