512K x 8 Bit FLASH and 128K x 8 Bit SRAM Low Voltage Combo Memory

FEATURES

- Both FLASH and RAM in one chip
- Wide Operating Voltage Range: 1.8 - 3.3V
- Fast Access Time
  - 1.8 V Operation: 250 ns (Max.)
  - 3.0 V Operation: 90 ns (Max.)
- Low Power Dissipation:
  - Standby
    - 1.8 V Operation: 1.0 µW (Typ.)
    - 3.0 V Operation: 10 µW (Typ.)
  - Operating
    - 1.8 V Operation: 2.0 mW (Typ.)
    - 3.0 V Operation: 30 mW (Typ.)
- Fully Static Operation
  - No clock or refresh required
- Three state Outputs
- Standard 32 Pin TSOP type 1 package or
- Standard 40 Pin TSOP package

GENERAL DESCRIPTION

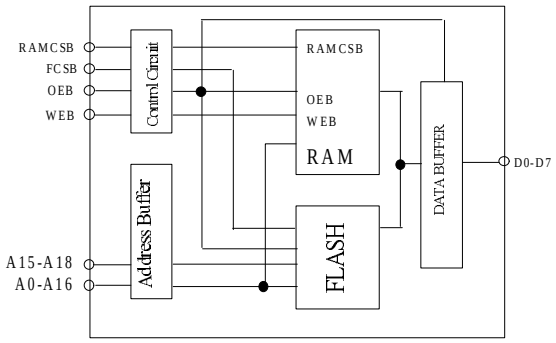
The LX59CF4128 is a combination memory chip consist of 4M-bit FLASH Memory organized as 512K words by 8 bits and a 1-Meg-bit Static Random Access Memory organized as 128K words by 8 bits. Output Enable Input ($\overline{OE}$) is pin-shared with $\overline{CS}$ 2 (RAM Enable Input) signal for the standard 32 pin TSOP package or separately in 40-pin TSOP package.

The device is fabricated using Linvex's advanced CMOS low power process technology.

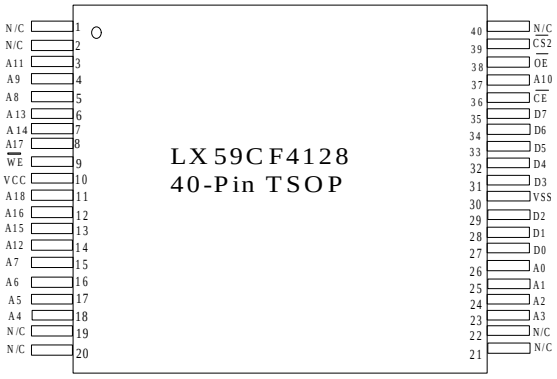
The LX59CF4128 has an output enable input for precise control of the data outputs. It also has two (2) seperate chip enable inputs for selection of either RAM or FLASH and minimize current drain during power-down mode.

The LX59CF4128 is particularly well suited for use in low voltage (1.8 - 3.3 V) operation such as GPS, cellular phones, PDA and other handheld applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



Pin Name	Pin Function
A_0 - A_{17}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{CS}$ 1/FCSB	FLASH Chip Enable Input
$\overline{CS}$ 2/RAMCSB	RAM Chip Enable Input
D0-D7	Data Inputs / Outputs
V_{CC}	Power (1.8 v - 3.3 v)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	-0.5 to V_{CC} +0.5	V
Voltage on Vcc Supply Relative to V_{SS}	V_{CC}	-0.5 to 4.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	-65 to 150	^{O}C
Operating Temperature	T_A	-20 to 70	^{O}C
Soldering Temperature and Time	T_{solder}	260 ^{O}C, 10 sec (Lead Only)	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A = 0 TO 70 ^{O}C)

Item	Symbol	Min.	Max.	Unit
Supply Voltage	V_{CC}	1.8	3.3	V
Ground	V_{SS}	0	0	V
Input High Voltage- 1.8 v	V_{IH}	1.4	V_{CC} + 0.5	V
Input High Voltage - 3.0 v	V_{IH}	2.4	V_{CC} + 0.5	V
Input Low Voltage - 1.8 v	V_{IL}	-0.3	0.3	V
Input Low Voltage - 3.0 v	V_{IL}	-0.3	0.3	V

DC AND OPERATING CHARACTERISTICS (Ta = 0 to 70 °C)

Item	Symbol	Test Conditions	VCC=1.8V		VCC=3.0 V± 0.3		Units
			Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}	-500	500	-500	500	nA
Output Leakage Current	I_{LO}	$\overline{CS}$ =V_{IH} or $\overline{OE}$ =V_{IH} or $\overline{WE}$ = V_{IL},$V_{I/O}$=V_{SS} to V_{CC}	-500	500	-500	500	nA
FLASH Operating Supply Current	I_{CC1}	$\overline{CS}$ 1=V_{IL}, $\overline{CS}$ 2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, $I_{I/O}$=0 mA	-	-	-	15.00 + 1.1(f)	mA
RAM Operating Current	I_{CC2}	$\overline{CS}$ 1=V_{IH}, $\overline{CS}$ 2=V_{IL}, $I_{I/O}$=0 mA	-	-	-	5.0 + 1(f)	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ ≥ V_{CC}-0.2V V_{IN} ≤ 0.2V,V_{IN} ≥ V_{CC}-0.2V	-	-	-	30	µA
Output Low Voltage	V_{OL}	I_{OL}= 1.0 mA at 3.3 V		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -0.5 mA at 3.3 V	0.8	-	2.2	-	V

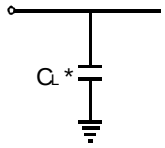
NOTE: $\overline{CS}$ = $\overline{CS}$ 1 & $\overline{CS}$ 2, $\overline{CS}$ 1 = FLASHCSB, $\overline{CS}$ 2 = RAMCSB, f=1/cycle time

CAPACITANCE *(f =1MHz, Ta = 25 °C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input / Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

TEST CONDITIONS (Ta=-20 TO 70 °C)

Parameter	Value	
	V_{CC} = 1.8 V	V_{CC} = 3.0 V
Input Pulse Level	0 to 3V	0 to 3V
Input Rise and Fall Time (10% to 90% VCC)	5 ns	5 ns
Input and Output Timing Reference Levels	0.90 V	1.5 V
Output Load	CL=100pF	CL=100pF



* Including scope and jig capacitance

I. SRAM Operation ($\overline{CS}$ 1 = FCSB = VIH)

READ CYCLE

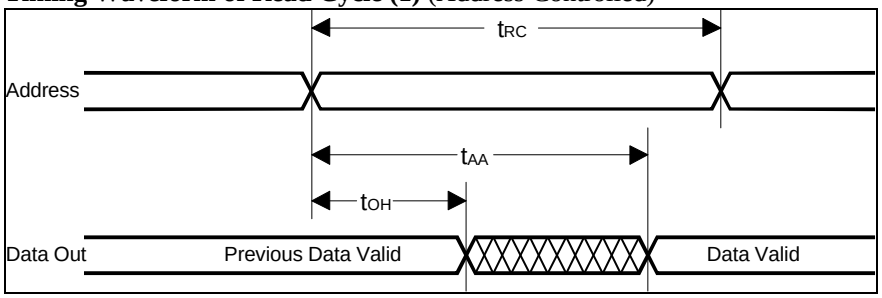
Parameter	Symbol	Vcc=1.8 V Worse Case		Vcc=3.0 V ± 0.3 Worse Case		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	250		90		ns
Address Access Time	t_{AA}		250		90	ns
Chip Select to Output	t_{CO}		250		90	ns
Output Enable to Valid Output	t_{OE}		150		60	ns
Chip Select to Low-Z Output	t_{LZ}	12		10		ns
Output Enable to Low-Z Output	t_{OLZ}	12		10		ns
Chip Disable to High-Z Output	t_{HZ}	0	30	0	20	ns
Output Disable to High-Z Output	t_{OHZ}	0	30	0	20	ns
Output Hold from Address Change	t_{OH}	5		5		ns

WRITE CYCLE

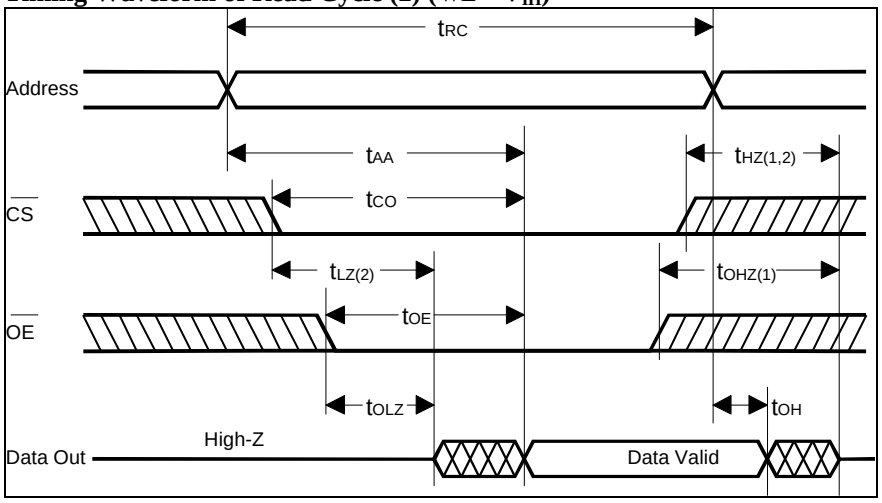
Parameter	Symbol	Vcc=1.8V		Vcc=3.0V± 0.3		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	250		90		ns
Chip Select to End of Write	t_{CW}	200		70		ns
Address Valid to End of Write	t_{AW}	200		70		ns
Address Set-up Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	200		70		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to Output High-Z	t_{WHZ}	-	40	0	25	ns
Data to Write Time Overlap	t_{DW}	125		50		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Output Low-Z	t_{OW}	10		5		ns

TIMING DIAGRAMS

Timing Waveform of Read Cycle (1) (Address Controlled)



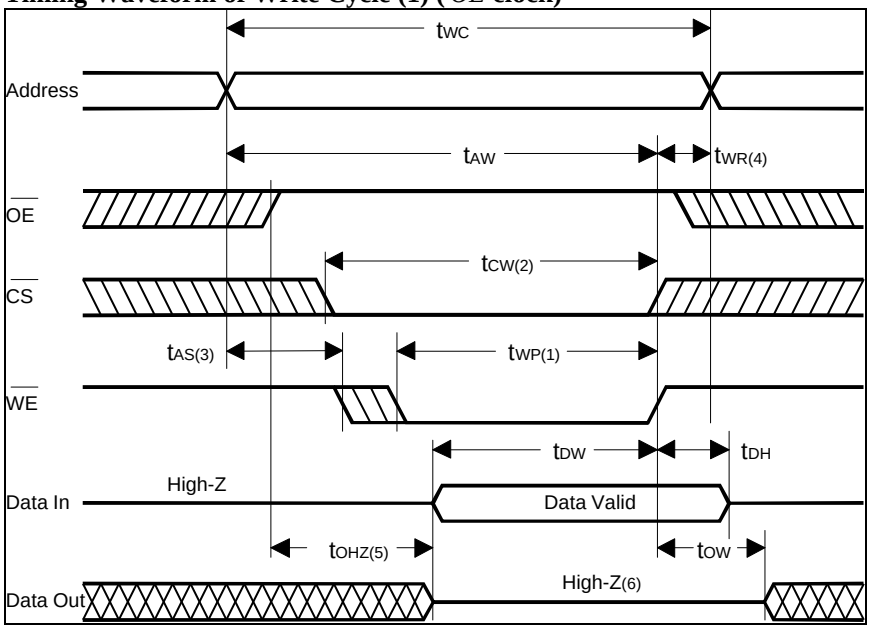
Timing Waveform of Read Cycle (2) ($\overline{WE}$ =V_{IH})



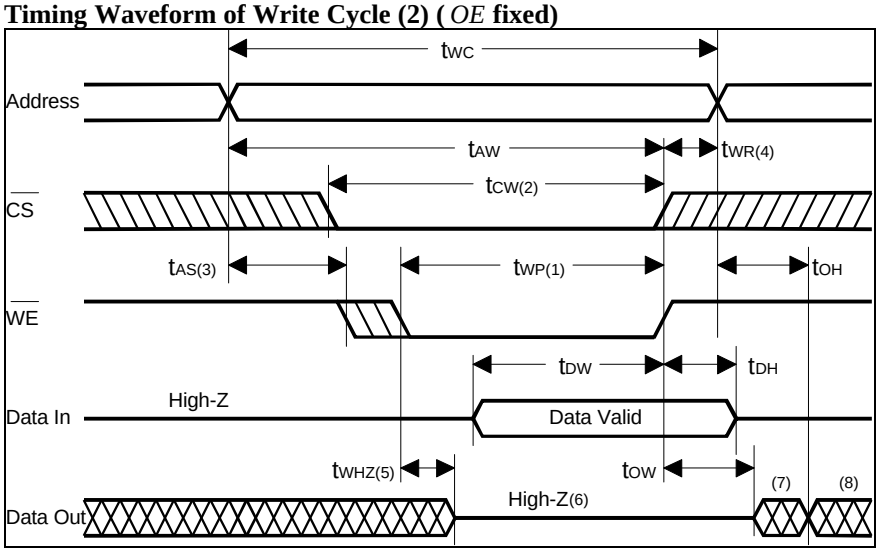
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are referenced to the V_{OH} or V_{OL}.
2. At any given temperature and voltage condition t_{HZ}(max) is less than t_{LZ}(min) both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.
4. Address valid prior to or coincident with $\overline{CS}$ 2 transition Low.

Timing Waveform of Write Cycle (1) ($\overline{OE}$ clock)



Timing Waveform of Write Cycle (2) ($\overline{OE}$ fixed)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ 2 and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ 2 going low and $\overline{WE}$ going low: A write end at the earliest transition among $\overline{CS}$ 2 going high and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS}$ 2 going low to end of write.
3. t_{AS} is measured from address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
5. if $\overline{OE}$, $\overline{WE}$ are in the read mode during this period, the I/O pins are in the outputs Low-Z state. Inputs of opposite phase of the
6. If $\overline{CS}$ 2 goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
7. D_{OUT} is the same phase of the latest written data in this write cycle.
8. D_{OUT} is the read data of new address
9. $\overline{CS}$ 1= FCSB = IH

II. FLASH Operation ($\overline{CS}_2$ = RAMCSB = V_{IH})

HARDWARE AND SOFTWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the LX59CF4128 in the following ways: (a) VCC sense— if VCC is below 2.0V (typical), the program function is inhibited. (b) Program inhibit— holding any one of OE low, CE high or WE high inhibits program cycles. (c) Noise filter— pulses of less than 15 ns (typical) on the WE or CE inputs will not initiate a program cycle. (d) After power up the device is in the read mode and in the software data protect mode.

The LX59CF4128 will default to software data protection after power up. A sequence of seven consecutive reads at specific addresses will unprotected the device. The address sequence is 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 041AH. The address bus is latched on the rising edge of OE or CE, whichever occurs first. A similar seven read sequence of 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 041AH will protect the device. Also refer to Figures 10 and 11 for the 7 read cycle sequence Software Data Protection. The I/O pins can be in any state (i.e., high, low, or tristate).

INPUT LEVELS: While operating with a 2.7V to 3.6V power supply, the address inputs, I/O lines, and control inputs (OE, CE and WE) may be driven from 0 to Vcc+0.6V without adversely affecting the operation of the device.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations. In this manner, the user can have a common board design for 256K to 4-megabit densities and, with each density's sector size in a memory map, have the system software apply the appropriate sector size. For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both methods of identification.

DATA POLLING (I/O7) : The LX59CF4128 features DATA polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. DATA polling may begin at any time during the program cycle.

TOGGLE BIT (I/O6) : In addition to DATA polling the LX59CF4128 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

CHIP ERASE MODES: The entire device may be erased by using a 6-byte software code for easy operation. Please see Software Chip Erase application note for details.

Table 1: Operation Modes Selection

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{out}	A_{IN}
Byte Program	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 2
Sector Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 2
Standby	V_{IH}	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/ D_{out}	X
Write Inhibit	X	X	V_{IH}	High Z/ D_{out}	X
Software Chip Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	See Table 2
Product Identification Hardware Mode	V_{IL}	V_{IL}	V_{IH}	Manufacturer Code (54H)	A_{18}-A_1=V_{IL}, A_0=V_{IL}
				Device Code (F4H)	A_{18}-A_1=V_{IL}, A_0=V_{IH}
Software Mode	V_{IL}	V_{IH}	V_{IL}		See Table 2
SDP Enable & Disable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 2
Reset	V_{IL}	V_{IH}	V_{IL}		See Table 2

Table 2: Software Command Summary

Command Summary	Required Cycle(s)	Setup Command Cycle			Execute Command Cycle			SDP[5]
		Type[1]	Addr[2,3]	Data[4]	Type[1]	Addr[2,3]	Data[4]	
Sector_ Erase	2	W	X	20H	W	SA	D0H	N
Byte_Program	2	W	X	10H	W	PA	PD	N
Chip_ Erase	2	W	X	30H	W	X	30H	N
Reset	1	W	X	FFH				Y
Read_ID	3	W	X	90H	R	Pg12	Pg12	Y
Software_ Data_Protect	7	R	Pg12					
Software_Data_ Unprotect	7	R	Pg12					

Notes:

1. Type definition: W = Write, R = Read, X = don't care
2. Addr (Address) definition: SA = Sector Address = A_{18} - A_8, sector size = 256 bytes; A_7-A_0 = X for this command.
3. Addr (Address) definition: PA = Program Address = A_{18} -A_0.
4. Data Definition: PD = Program Data, H = number in hex
5. SDP = Software Data Protect mode using 7 Read Cycle Sequence.
   a) Y = the operation can be executed with protection enabled
   b) N = the operation cannot be executed with protection enabled

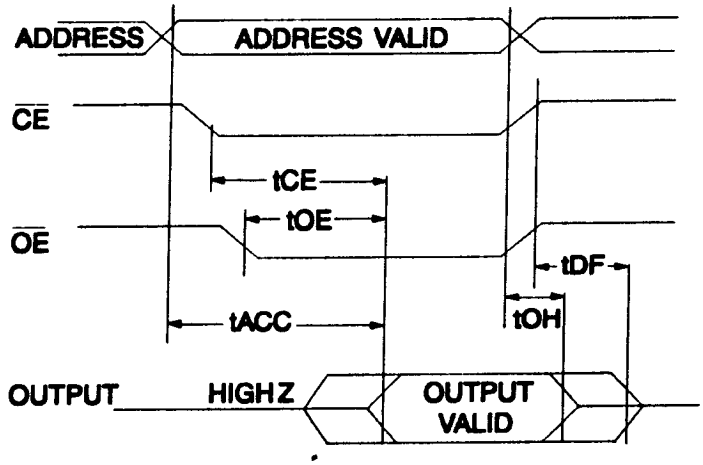
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to Vcc			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to Vcc			1	µA
I_{SB1}	Vcc Standby Current CMOS	$\overline{CE}$ = Vcc - 0.3V to Vcc	Com.		20	µA
			Ind.		50	µA
I_{SB2}	Vcc Standby Current TTL	$\overline{CE}$ = 2.0V to Vcc			1	mA
I_{CC}	Vcc Active Current	f = 5 MH_Z; I_{OUT} = 0 mA; Vcc=3.6V			15	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL}= 1.6mA; Vcc= 3.0V			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -100µA; Vcc=3.0V		2.4		V

AC Read Characteristics

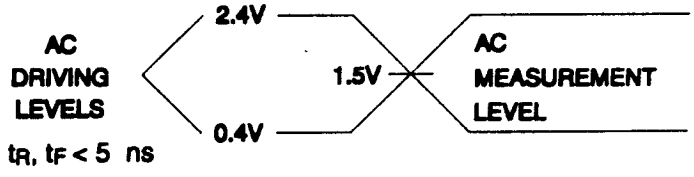
Symbol	Parameter	Min	Max	Units
t_{ACC}	Address to Output Delay		90	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		90	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	60	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	30	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		ns

AC Read Waveforms

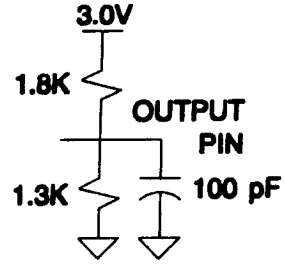


Notes: 1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

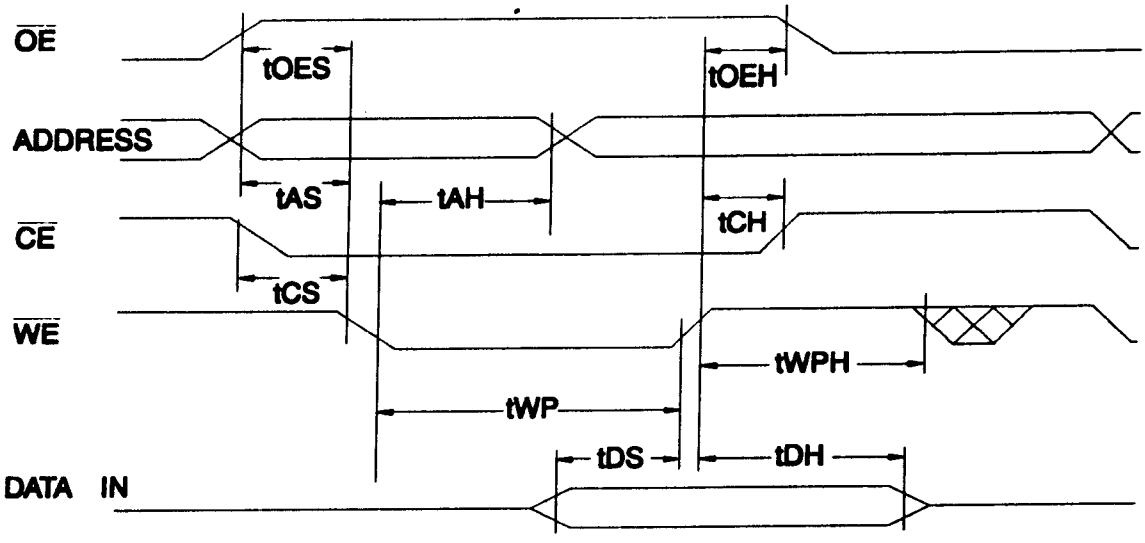
Note: 1. These parameters are characterized and not 100% tested.

AC Byte Load Characteristics

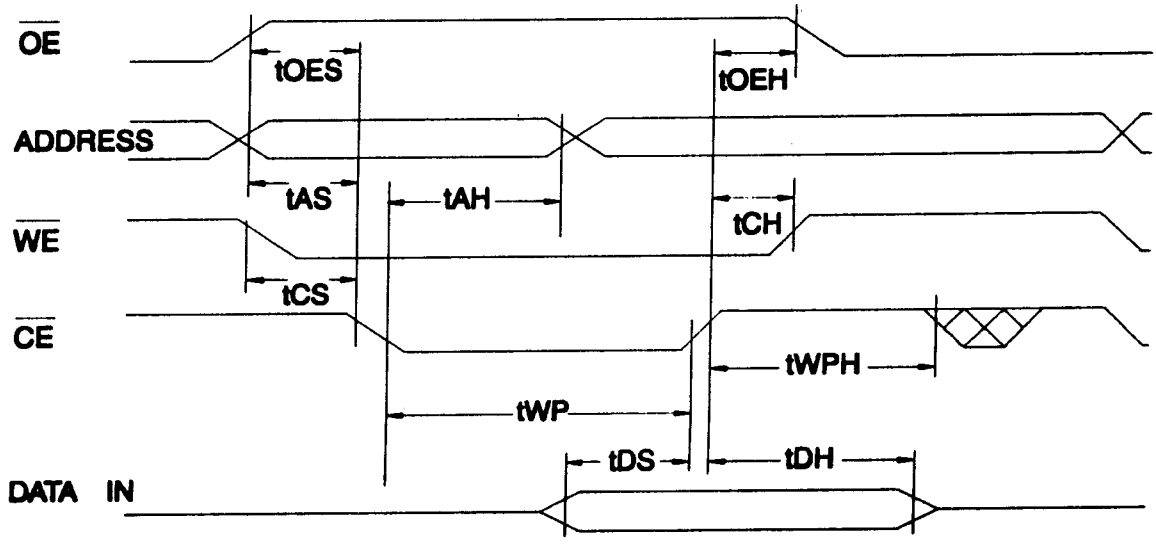
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		n
t_{AH}	Address Hold Time	10		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		n
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	70		ns
t_{DS}	Data Set-up Time	60		n
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		n
t_{WPH}	Write Pulse Width High	70		ns

AC Byte Load Waveforms [1, 2]

$\overline{WE}$ Controlled



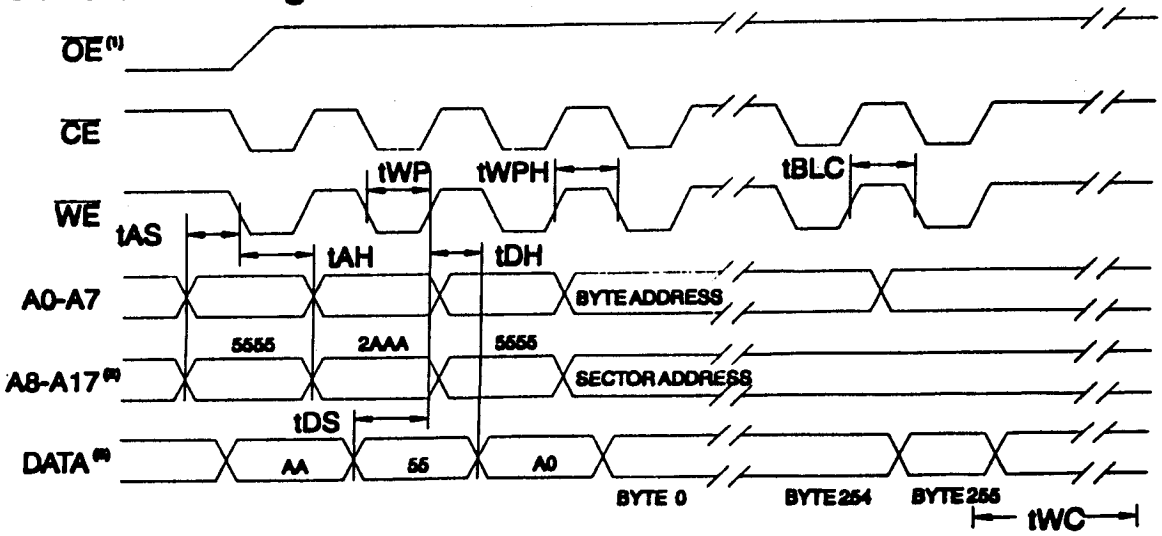
$\overline{CE}$ Controlled



Program Cycle Characteristics

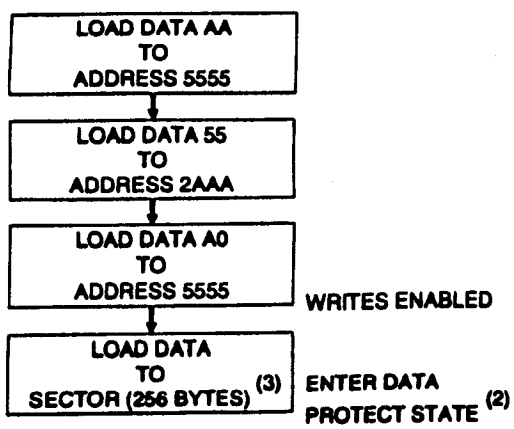
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		20	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	200		ns
t_{BLC}	Byte Load Cycle Time		100	µs
t_{WPH}	Write Pulse Width High	200		ns

Software Protected Program Waveform



Notes: 1. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
2. A8 through A17 must specify the sector address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
3. Data in bytes not loaded within a sector being programmed may be altered by the program operation; therefore, all bytes within a sector must be loaded.

Programming Algorithm (1)



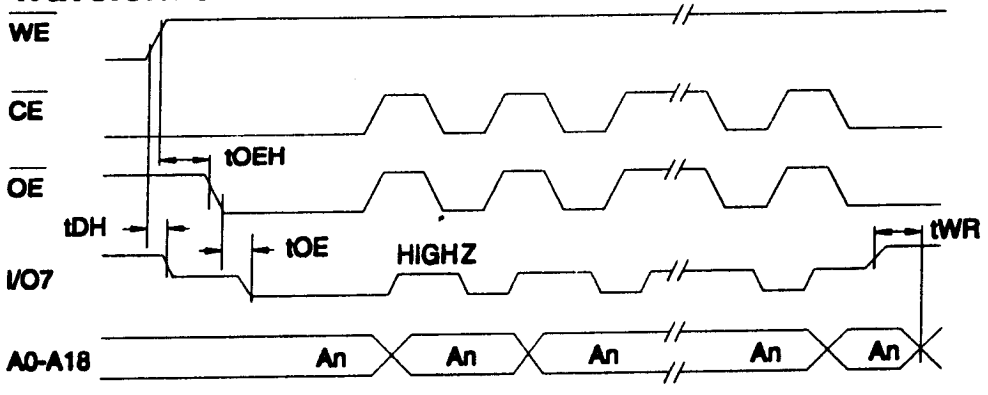
Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be re-activated at end of program cycle.
3. 256-bytes of data MUST BE loaded.

$\overline{\text{Data}}$ Polling Characteristics (1, 2)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			n
t_{OEH}	$\overline{OE}$ Hold Time	10			n
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

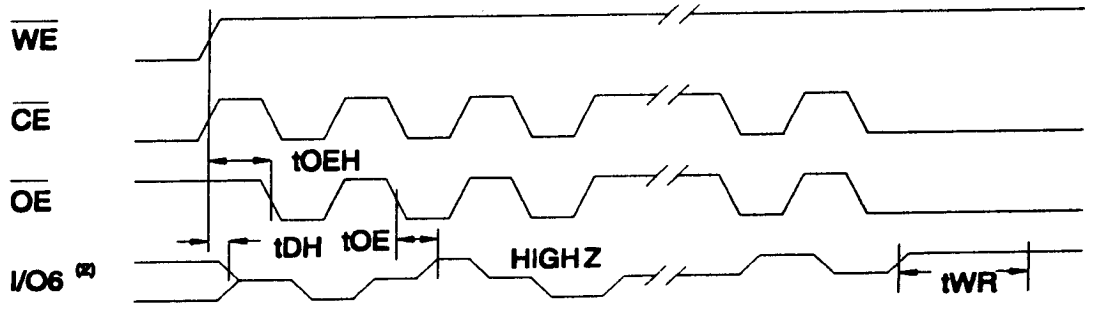


Toggle Bit Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			n
t_{OEH}	$\overline{OE}$ Hold Time	10			n
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

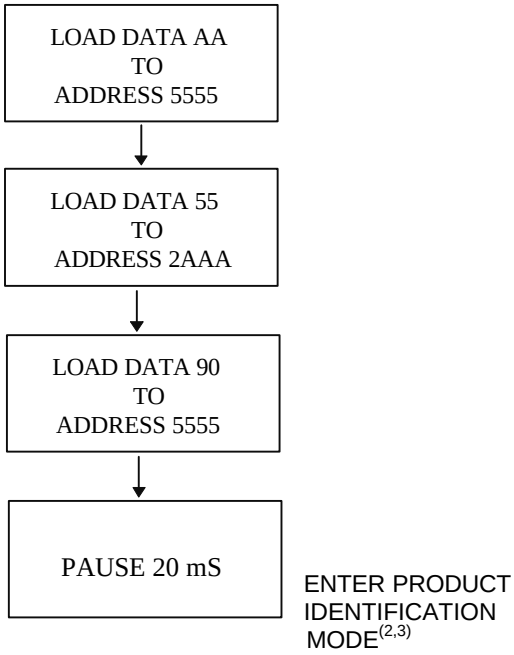
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms (1, 3)

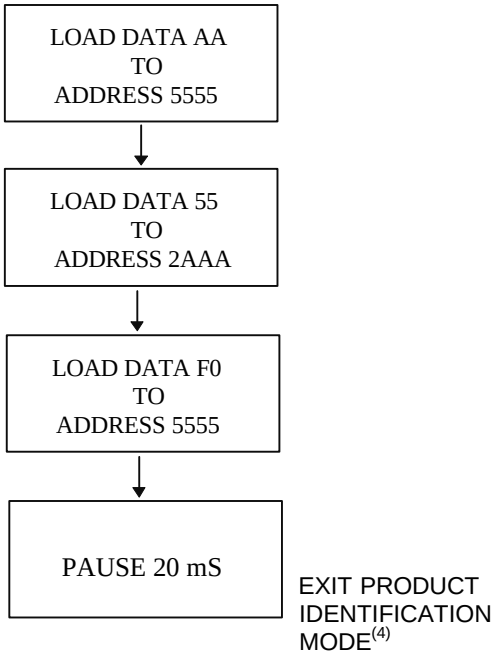


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry (1)



Software Product Identification Exit (1)



Notes for software product identification:

1. Data Format: I/O7-I/O0 (Hex);
   Address Format: A14-A0 (Hex).
2. A1-A17 = V_{IL}.
   Manufacture Code is read for A0=V_{IL};
   Device Code is read for A0=V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code is 54H, The Device Code is F4H

Functional Description/Truth Table (32 Pin TSOP)

A0=A18	FCSB	RAMCSB/$\overline{OE}$ (PIN 32)	$\overline{WE}$	D0-D7	
X	H	H	X	Z	Standby
A0-A18	L	$\overline{OE}$ (L)	H	Dout	Flash read
A0-A18	L	$\overline{OE}$ (H)	L	Din	Flash write
Only A0-A16 are vaild *	H	RAMCSB (L)	H	Dout	RAM read
Only A0-A16 are vaild *	H	RAMCSB (L)	L	Din	RAM write

***** A17 - A18 must be fixed to "L" or "H"

Note: (1) $\overline{OE}$ & $\overline{CS}$2 are pin-shared
(2) It is forbidden that FCSB pin and RAMCSB pin will be "0" at same time.
(3) X means Don't Care.
(4) Flash write must follow "Flash" write procedures.

Functional Description/Truth Table (40 Pin TSOP)

A0=A18	FCSB	RAMCSB	$\overline{WE}$	$\overline{OE}$	D0-D7	
X	H	H	X	X	Z	Standby
A0-A18	L	H	X	H	Z	Output Floating
A0-A18	L	H	X	L	Dout	FLASH read
A0-A18	L	H	L	X	Din	FLASH write
Only A0-A16 are vaild *	H	L	H	H	Z	Output Floating
Only A0-A16 are vaild *	H	L	H	L	Dout	RAM read
Only A0-A16 are vaild *	H	L	L	X	Din	RAM write

*****A17-A18 must be fixed to "L" or "H"

Note: (1) It is forbidden that FCSB pin and RAMCSB pin will be "0" at same time.

(2) X means Don't Care.

(3) Flash write must follow "Flash" write procedures.