LX62VL1001

CMOS SRAM

128K x 8 Bit Very-Low Voltage Operating Static Ram

FEATURES

- **Extended Operating Voltage**:
  1.8 V to 3.6 V
- **Fast Access Time**

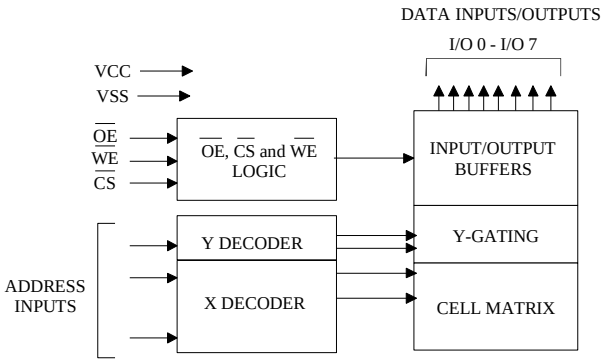
LX62VL1001-15	LX62VL1001-70
1.8V : ≤ 80ns	1.8V : ≤ 200ns
3.0V : ≤ 15ns	3.0V : ≤ 70ns

- **Low Power Dissipation Standby / Operating**
  1.8V: .15mW / 10 mW (Typ.)
  2.5V: .20mW / 15 mW (Typ.)
  3.3V: .33mW / 20 mW (Typ.)
- **Fully Static Operation**
  No clock or refresh required
- **Three state Outputs**
- **Standard Pin configuration**
  LX62VL1001SC : 32-PIN SOP (525 mil)
  LX62VL1001PC : 32-PIN PDIP (600 mil)
  LX62VL1001TC : 32-PIN TSOP (Type I)

GENERAL DESCRIPTION

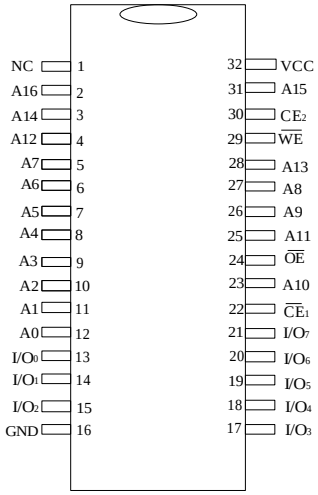
The LX62VL1001 is a 1,048,576 bit Static Random Access Memory organized as 131,072 words by 8 bits.
The device is fabricated using Linvix's low power, advanced CMOS process and high-speed but low power circuit technology.
The LX62VL1001 has an output enable input for precise control of the data outputs. It also has two (2) chip enable inputs for memory expansion(CE_1) and minimum current power-down mode (CE_2).
The LX62VL1001 is particularly well suited for use in low voltage (1.8 - 3.0 V) operation and battery back-up applications or in standard 3.3 V systems.

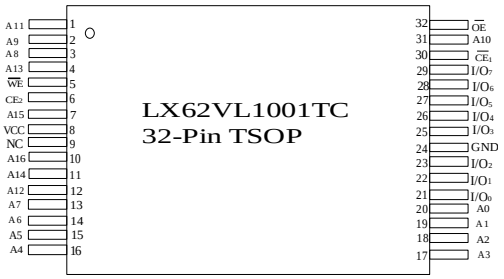
FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0 - A_{16}	Address Inputs
$\overline{WE}$	Write Enable Input
CE_1 , CE_2	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O_0 - I/O_7	Data Inputs / Outputs
V_{CC}	Power (1.8 v - 3.6 v)
V_{SS}	Ground
NC	No Connection

PIN CONFIGURATION (TOP VIEW)





ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	-0.5 to V_{CC} +0.5	V
Voltage on Vcc Supply Relative to V_{SS}	V_{CC}	-0.5 to 4.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	-65 to 150	^{O}C
Operating Temperature	T_A	-20 to 70	^{O}C
Soldering Temperature and Time	T_{solder}	260 ^{O}C, 10 sec (Lead Only)	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A = -20 TO 70 ^{O}C)

Item	Symbol	Min.	Max.	Unit
Supply Voltage	V_{CC}	1.8	3.6	V
Ground	V_{SS}	0	0	V
Input High Voltage	V_{IH}	.7 Vcc	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-0.3	.3 Vcc	V

DC AND OPERATING CHARACTERISTICS (T_A = -20 TO 70 ^{O}C)

Item	Symbol	Test Conditions	VCC=1.8V		VCC=2.5V		VCC=3.3V		Units
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}	-1	1	-1	1	-1	1	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ =V_{IH} or $\overline{OE}$ =V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}	-1	1	-1	1	-1	1	µA
DC Operating Supply Current	I_{CC}	$\overline{CS}$ =V_{IL}, V_{IN}=V_{IH} or V_{IL}, $I_{I/O}$=0 mA	-	1.0	-	1.5	-	2.0	mA
Average Operating Current	I_{CC}	200/70/15 ns Cycle $\overline{CS}$ =V_{IL}, $I_{I/O}$=0 mA	-	50	-	80	-	100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ =V_{IH}	-	300	-	300	-	300	µA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC}-0.2V V_{IN} ≤ 0.2V, V_{IN} ≥ V_{CC}-0.2V	-	25	-	30	-	40	µA
Output Low Voltage	V_{OL}	I_{OL}= 2.1 mA at 3.3 V only		.2 Vcc		.2 Vcc		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -0.5 mA at 3.3 V only	.8 Vcc	-	.8 Vcc		2.2	-	V

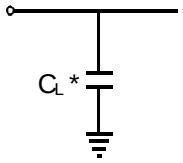
Note: $\overline{CS}$ is defined as $\overline{CE_1}$ and CE_2 in one chip select condition

CAPACITANCE *(f =1MHz, Ta = 25 °C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF
Input / Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	10	pF

TEST CONDITIONS (Ta=-20 TO 70 °C)

Parameter	Value		
	V_{CC} = 1.8 V	Vcc = 2.5 V	V_{CC} = 3.3V
Input Pulse Level	.8 Vcc to 0	.8 Vcc to 0	3.0 to 0
Input Rise and Fall Time	5 ns	3 ns	3 ns
Input and Output Timing Reference Levels	Vcc / 2	Vcc / 2	1.5 V
Output Load	CL=30pF	CL = 30pF	CL=30pF



* Including scope and jig capacitance

READ CYCLE

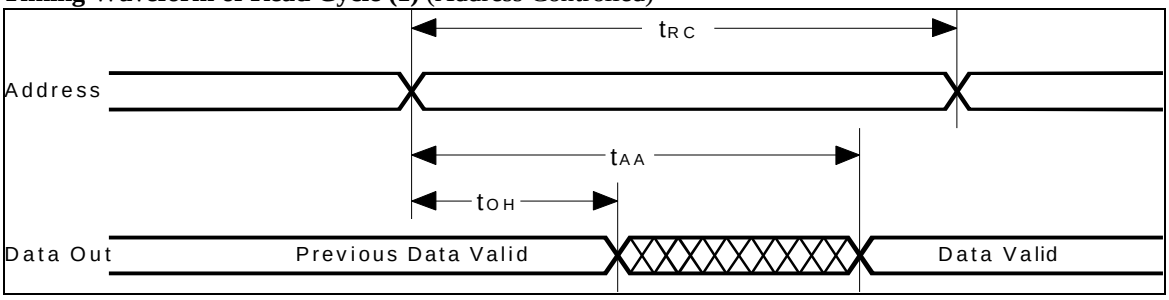
Parameter	Symbol	Vcc=1.8 V		LX62VL1001-70 Vcc=3.0V± .3V		LX62VL1001-15 Vcc=3.0V± .3V		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200		70		15		ns
Address Access Time	t_{AA}		200		70		15	ns
Chip Select to Output	t_{CO}		200		70		15	ns
Output Enable to Valid Output	t_{OE}		120		45		7	ns
Chip Select to Low-Z Output	t_{LZ}	50		10		3		ns
Output Enable to Low-Z Output	t_{OLZ}	50		10		3		ns
Chip Disable to High-Z Output	t_{HZ}	0	80	0	15		7	ns
Output Disable to High-Z Output	t_{OHZ}	0	80	0	15		7	ns
Output Hold from Address Change	t_{OH}	30		10		3		ns

WRITE CYCLE

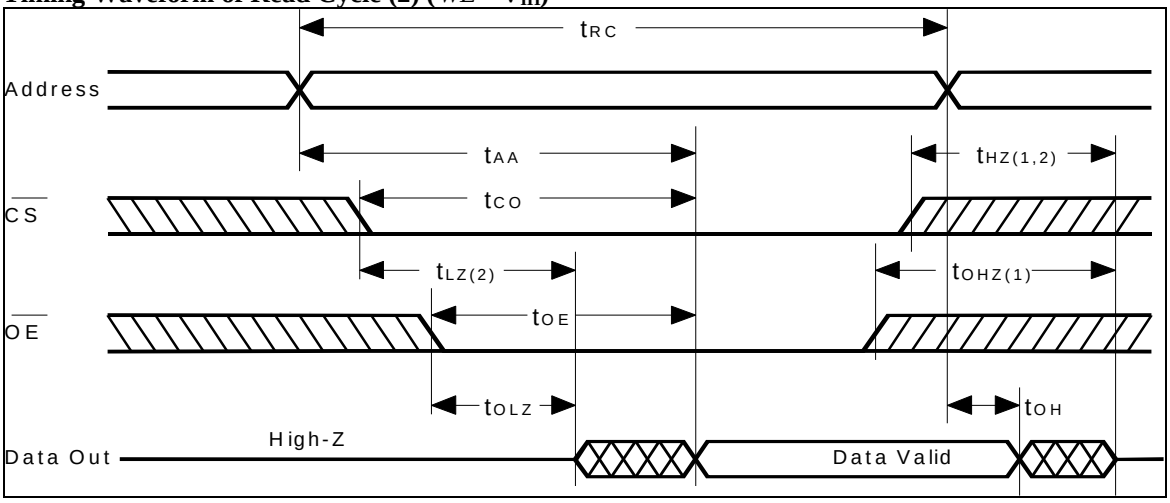
Parameter	Symbol	Vcc=1.8 V		LX62VL1001-70 Vcc=3.0V± 0.3V		LX62VL1001-15 Vcc=3.0V±0.3V		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	200		70		15		ns
Chip Select to End of Write	t_{CW}	120		60		12		ns
Address Valid to End of Write	t_{AW}	120		60		12		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	120		50		12		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WHZ}	0	60	0	30		7	ns
Data to Write Time Overlap	t_{DW}	100		30		8		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	25		10		3		ns

TIMING DIAGRAMS

Timing Waveform of Read Cycle (1) (Address Controlled)



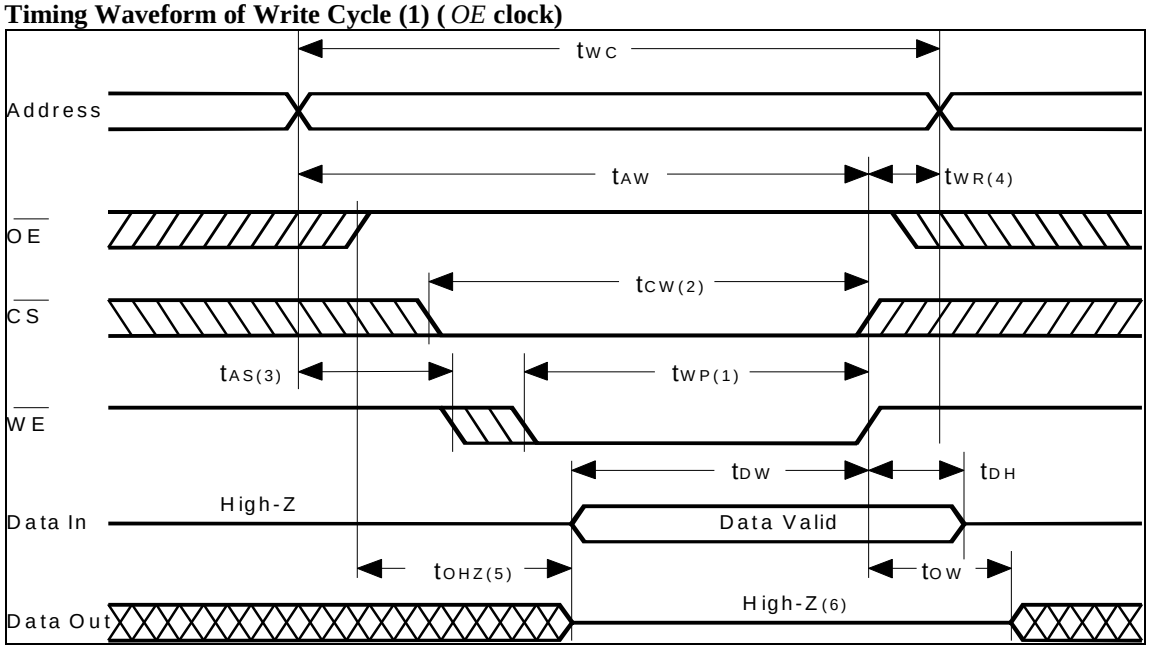
Timing Waveform of Read Cycle (2) ($\overline{WE}$ =V_{IH})



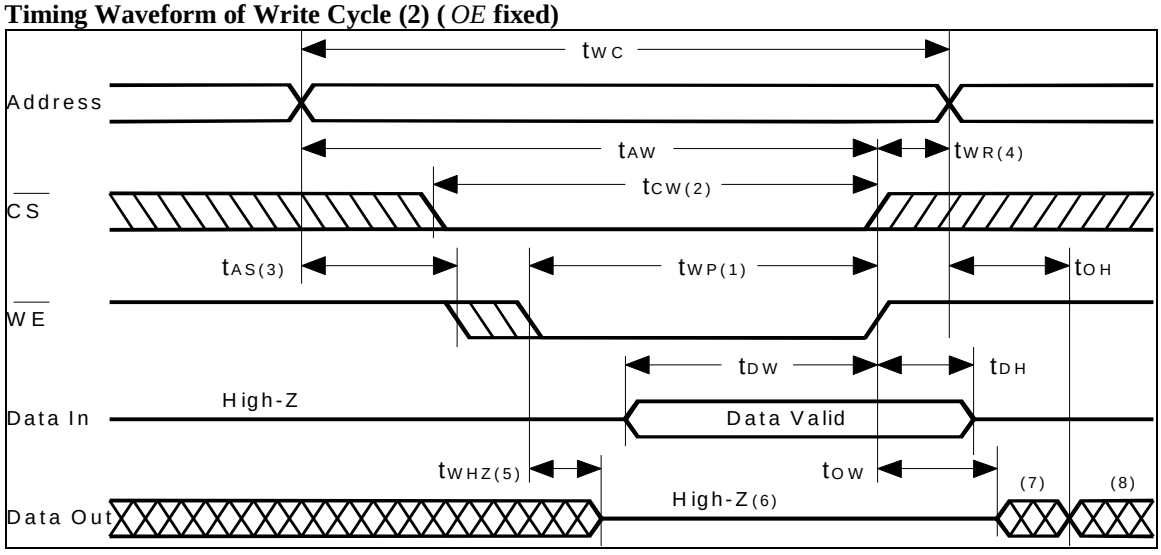
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are referenced to the V_{OH} or V_{OL}.
2. At any given temperature and voltage condition t_{HZ}(max) is less than t_{LZ}(min) both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.
4. $\overline{CS}$ is defined as $\overline{CE_1}$ and CE_2 function. Function description is given in Page 6.
5. Address valid prior to or coincident with $\overline{CS}$ transition Low.

Timing Waveform of Write Cycle (1) ($\overline{OE}$ clock)



Timing Waveform of Write Cycle (2) ($\overline{OE}$ fixed)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write end at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
5. if $\overline{OE}$, $\overline{WE}$ are in the read mode during this period, the I/O pins are in the outputs Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
7. D_{OUT} is the same phase of the latest written data in this write cycle.
8. D_{OUT} is the read data of new address

Functional Description

	$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
	H	X	X	X	Power Down	High-Z	I_{SB},I_{SB1}
	X	L	X	X	Power Down	High-Z	I_{SB},I_{SB1}
	L	H	H	H	Output Disable	High-Z	I_{CC}
CS	L	H	H	L	Read	D_{OUT}	I_{CC}
	L	H	L	X	Write	D_{IN}	I_{CC}

Note: 1. X means Don't Care

2. $\overline{CS}$ is defined as CE_1 and CE_2 in one chip select condition

PACKAGE OUTLINES AND DIMENSIONS