256K x 8 Bit ROM and 256K X 8 Bit SRAM Low Voltage Combo Memory

FEATURES

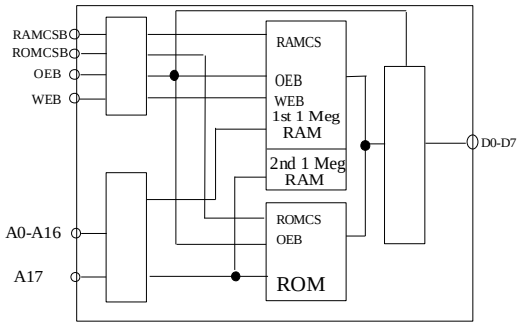
- Both ROM and RAM in one chip
- Wide Operating Voltage Range: 1.8 - 3.3V
- Fast Access Time
  - 1.8 V Operation: ≤ 300 ns
  - 3.0 V Operation: ≤ 150 ns
- Low Power Dissipation:
  - Standby
    - 1.8 V Operation: .20µW (Typ.)
    - 3.0 V Operation: 2.0µW (Typ.)
  - Operating
    - 1.8 V Operation: 6 mW (Typ.)
    - 3.0 V Operation: 30 mW (Typ.)
- Fully Static Operation
  - No clock or refresh required
- Three state Outputs
- Standard 32 Pin TSOP type 1 package

LX50CM2256 TC-120 (120 ns)

GENERAL DESCRIPTION

The LX50CM2256 is a combination memory chip consist of 2M-bit Read Only Memory organized as 256K words by 8 bits and a 2 Mega-bit Static Random Access Memory organized also as 256K words by 8 bits.
The device is fabricated using Linvex's advanced CMOS low power process technology.
The LX50CM2256 has an output enable input for precise control of the data outputs. It also has two (2) sepreate chip enable inputs for selection of either RAM or ROM and minimize current drain during power-down mode.
Address A17 is used to select either the 1st 1 Meg SRAM or 2nd 1 Meg SRAM in a "Double-Deck" ™ arrangement.
The LX50CM2256 is particularly well suited for use in low voltage (1.8 - 3.3 V) operation such as pager and other handheld applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

Pin Name	Pin Function
A_0 - A_{17}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{CS}$ 1/ROMCSB	ROM Enable Input
$\overline{CS}$ 2/RAMCSB	RAM Enable Input
D0-D7	Data Inputs / Outputs
V_{CC}	Power (1.8 v - 3.3 v)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS

tem	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	-0.5 to V_{CC} +0.5	V
Voltage on Vcc Supply Relative to V_{SS}	V_{CC}	-0.5 to 4.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	-65 to 150	^{O}C
Operating Temperature	T_A	-20 to 70	^{O}C
Soldering Temperature and Time	T_{solder}	260 ^{O}C, 10 sec (Lead Only)	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A = -20 TO 70 ^{O}C)

Item	Symbol	Min.	Max.	Unit
Supply Voltage	V_{CC}	1.8	3.3	V
Ground	V_{SS}	0	0	V
Input High Voltage- 1.8 v	V_{IH}	1.2	V_{CC} + 0.5	V
Input High Voltage - 3.0 v	V_{IH}	2.4	V_{CC} + 0.5	V
Input Low Voltage - 1.8 v	V_{IL}	-0.3	0.3	V
Input Low Voltage - 3.0 v	V_{IL}	-0.3	0.4	V

DC AND OPERATING CHARACTERISTICS (Ta = -20 to 70 °C)

Item	Symbol	Test Conditions	VCC=1.8V		VCC=3.0 V± 0.3		Units
			Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}	-500	500	-500	500	nA
Output Leakage Current	I_{LO}	$\overline{CS}$ =V_{IH} or $\overline{OE}$ =V_{IH} or $\overline{WE}$ = V_{IL},$V_{I/O}$=V_{SS} to V_{CC}	-500	500	-500	500	nA
ROM Operating Supply Current	I_{CC1}	$\overline{CS}$ 1=V_{IL}, $\overline{CS}$ 2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, $I_{I/O}$=0	-	-	-	8+1.5xf	mA
RAM Operating Current	I_{CC2}	$\overline{CS}$ 1=V_{IH}, $\overline{CS}$ 2=V_{IL}, $I_{I/O}$=0 mA	-	-	-	5+2xf	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ ≥ V_{CC}-0.2V V_{IN} ≤ 0.2V,V_{IN} ≥ V_{CC}-0.2V	-	-	-	10	μA
Output Low Voltage	V_{OL}	I_{OL}= 1.0 mA at 3.3 V		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -0.5 mA at 3.3 V	1.0	-	2.2	-	V

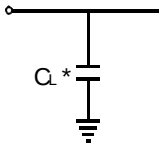
NOTE: $\overline{CS}$ = $\overline{CS}$ 1 & $\overline{CS}$ 2, $\overline{CS}$ 1 = ROMCSB, $\overline{CS}$ 2 = RAMCSB ; f = operating frequency

CAPACITANCE *(f =1MHz, Ta = 25 °C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input / Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

TEST CONDITIONS (Ta=-20 TO 70 °C)

Parameter	Value	
	V_{CC} = 1.8 V	V_{CC} = 3.0 V
Input Pulse Level	1.2 to 0.3 V	2.2 to 0.4 V
Input Rise and Fall Time	5 ns	5 ns
Input and Output Timing Reference Levels	0.90 V	1.5 V
Output Load	CL=35pF	CL=35pF



* Including scope and jig capacitance

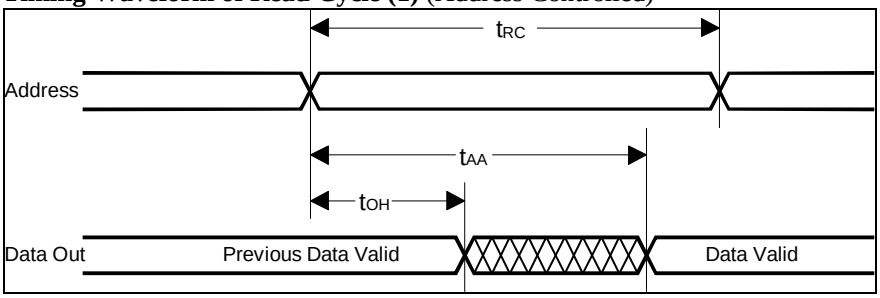
I. ROM Operation ($\overline{CS}_2$ = RAMCSB = VIH)

READ CYCLE

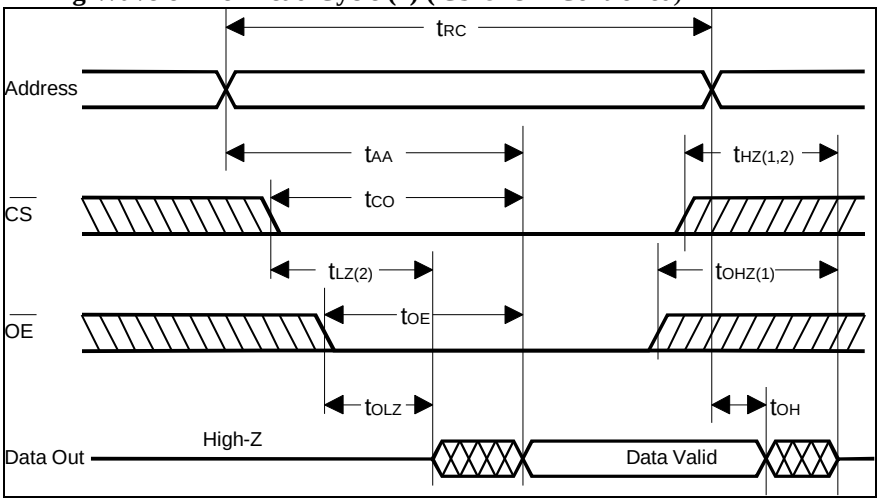
Parameter	Symbol	50CM2256 Vcc=1.8V		50CM2256-120 Vcc=3.0 V ± 0.3		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	350		120		ns
Address Access Time	t_{AA}		350		120	ns
Chip Select to Output	t_{CO}		350		120	ns
Output Enable to Valid Output	t_{OE}		200		80	ns
Chip Select to Low-Z Output	t_{LZ}	20		10		ns
Output Enable to Low-Z Output	t_{OLZ}	20		10		ns
Chip Disable to High-Z Output	t_{HZ}	0	40	0	20	ns
Output Disable to High-Z Output	t_{OHZ}	0	40	0	20	ns
Output Hold from Address Change	t_{OH}	15		10		ns

TIMING DIAGRAMS

Timing Waveform of Read Cycle (1) (Address Controlled)



Timing Waveform of Read Cycle (2) ($\overline{CS}$ **&** $\overline{OE}$ Controlled)



NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are referenced to the V_{OH} or V_{OL}.
2. At any given temperature and voltage condition t_{HZ}(max) is less than t_{LZ}(min) both for a given device and from device to device.
3. $\overline{CS}$ 2/RAMCSB is high for read cycle.
4. Address valid prior to or coincident with $\overline{CS}$ 1 transition Low.

II. SRAM Operation ($\overline{CS}$ 1 = ROMCSB = VIH)

READ CYCLE

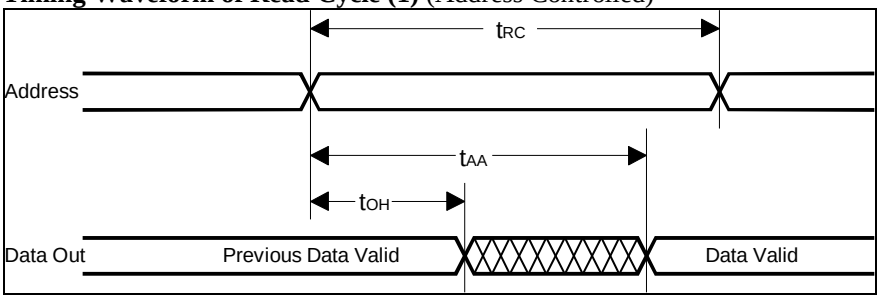
Parameter	Symbol	50CM2256 Vcc=1.8V		50CM2256-120 Vcc=3.0 V ± 0.3		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	350		120		ns
Address Access Time	t_{AA}		350		120	ns
Chip Select to Output	t_{CO}		350		120	ns
Output Enable to Valid Output	t_{OE}		200		60	ns
Chip Select to Low-Z Output	t_{LZ}	20		15		ns
Output Enable to Low-Z Output	t_{OLZ}	20		15		ns
Chip Disable to High-Z Output	t_{HZ}	0	40	0	30	ns
Output Disable to High-Z Output	t_{OHZ}	0	40	0	30	ns
Output Hold from Address Change	t_{OH}	15		10		ns

WRITE CYCLE

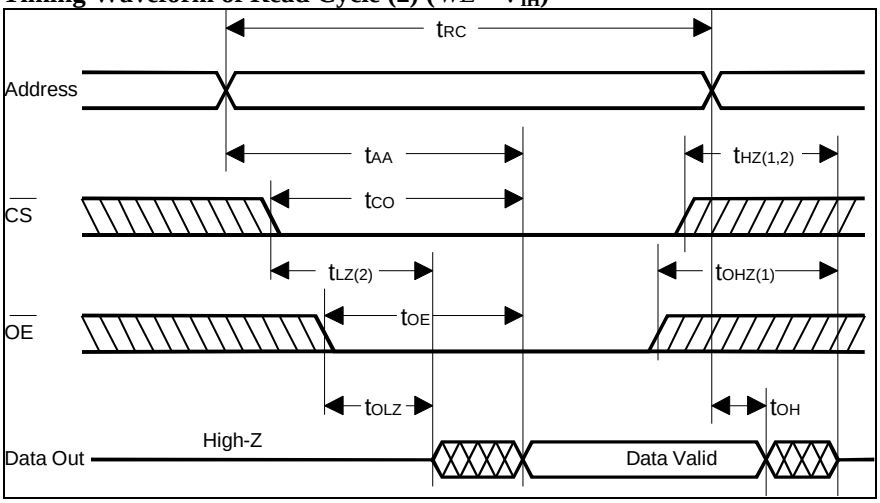
Parameter	Symbol	50CM2256 Vcc=1.8V		50CM2256-120 Vcc=3.0V + 0.3		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	350	—	120		ns
Chip Select to End of Write	t_{CW}	250		100		ns
Address Valid to End of Write	t_{AW}	250		100		ns
Address Set-up Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	220		90		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to Output High-Z	t_{WHZ}	-	95	0	60	ns
Data to Write Time Overlap	t_{DW}	150		80		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Output Low-Z	t_{OW}	15		10		ns

TIMING DIAGRAMS

Timing Waveform of Read Cycle (1) (Address Controlled)



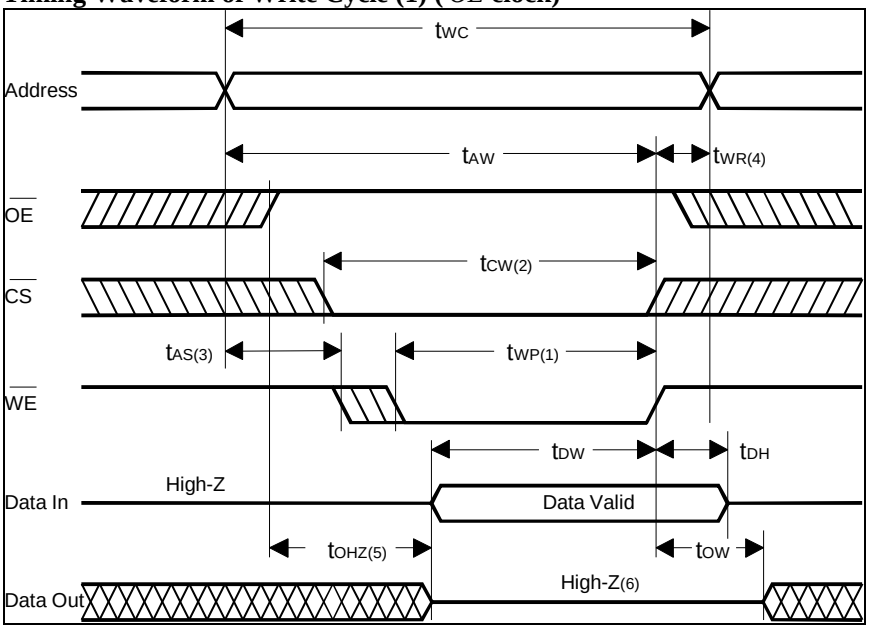
Timing Waveform of Read Cycle (2) ($\overline{WE}$ =V_{IH})



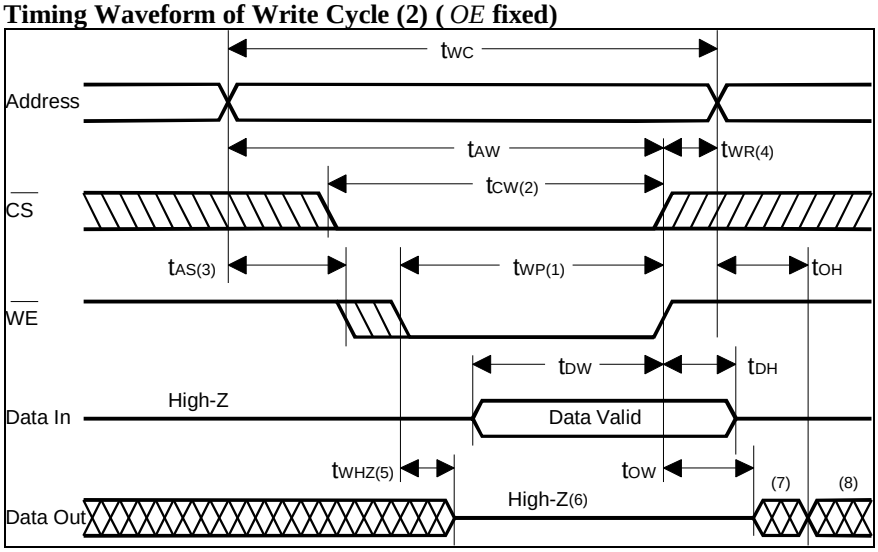
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are referenced to the V_{OH} or V_{OL}.
2. At any given temperature and voltage condition t_{HZ}(max) is less than t_{LZ}(min) both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.
4. Address valid prior to or coincident with $\overline{CS}$ 2 transition Low.

Timing Waveform of Write Cycle (1) ($\overline{OE}$ clock)



Timing Waveform of Write Cycle (2) ($\overline{OE}$ fixed)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ 2 and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ 2 going low and $\overline{WE}$ going low: A write end at the earliest transition among $\overline{CS}$ 2 going high and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS}$ 2 going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
5. if $\overline{OE}$, $\overline{WE}$ are in the read mode during this period, the I/O pins are in the outputs Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS}$ 2 goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
7. D_{OUT} is the same phase of the latest written data in this write cycle.
8. D_{OUT} is the read data of new address
9. $\overline{CS}$ 1= ROMCSB = V_{IH}

Functional Description/Truth Table

A0-A17	A17	ROMCSB	RAMCSB	$\overline{WE}$	$\overline{OE}$	D0-D7	
X	H	H	H	X	X	Z	Standby
A0-A17	_	L	H	X	H	Z	Output Floating
A0-A17	_	L	H	X	L	Dout	ROM read
A0-A16	X	H	L	H	H	Z	Output Floating
A0-A16	L	H	L	H	L	Dout	1st 1 Meg RAM Read
A0-A16	L	H	L	L	X	Din	1st 1 Meg RAM Write
A0-A16	H	H	L	H	L	Dout	2nd 1 Meg RAM Read
A0-A16	H	H	L	L	X	Din	2nd 1 Meg RAM Write

Note: (1) It is forbidden that ROMCSB pin and RAMCSB pin will be "0" at same time.
(2) X means Don't Care.

PACKAGE OUTLINES AND DIMENSIONS

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