256K x 8 Bit ROM and 32K x 8 Bit SRAM Low Voltage Combo Memory

FEATURES

- Both ROM and RAM in one chip
- Wide Operating Voltage Range: 3.0 - 5.0V
- Fast Access Time
  - 3.0 V Operation: 150 ns (Max.)
  - 5.0 V Operation: 70 ns (Max.)
- Low Power Dissipation:
  - Standby
    - 3.0 V Operation: 1.0μW (Typ.)
    - 5.0 V Operation: 10.0μW (Typ.)
  - Operating
    - 3.0 V Operation: 20 mW (Typ.)
    - 5.0 V Operation: 80 mW (Typ.)
- Fully Static Operation
  - No clock or refresh required
- Three state Outputs
- Standard 32 Pin TSOP type 1 package

GENERAL DESCRIPTION

The LX50CM204 is a combination memory chip consist of 2M-bit Read Only Memory organized as 256K words by 8 bits and a 256K-bit Static Random Access Memory organized as 32K words by 8 bits.

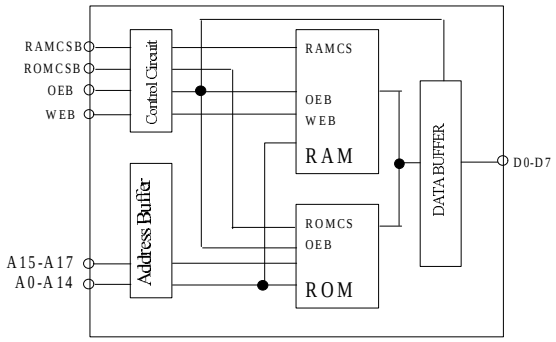
The device is fabricated using Linvex's advanced CMOS low power process technology.

The LX50CM204 has an output enable input for precise control of the data outputs. It also has two (2) sepreate chip enable inputs for selection of either RAM or ROM and minimize current drain during power-down mode.

The LX50CM204 is particularly well suited for use in low voltage (3.0 - 5.0 V) operation such as PCMCIA NETWORK cards, LAN MODEMS and other handheld applications.

PIN CONFIGURATION (TOP VIEW)

FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0 - A_{17}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{CS}$ 1/ROMCSB	ROM Enable Input
$\overline{CS}$ 2/RAMCSB	RAM Enable Input
D0-D7	Data Inputs / Outputs
V_{CC}	Power (3.0 v - 5.0 v)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	-0.5 to V_{CC} +0.5	V
Voltage on Vcc Supply Relative to V_{SS}	V_{CC}	-0.5 to 5.5	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	-65 to 150	^{O}C
Operating Temperature	T_A	-40 to 85	^{O}C
Soldering Temperature and Time	T_{solder}	260 ^{O}C, 10 sec (Lead Only)	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A = 0 TO 70 ^{O}C)

Item	Symbol	Min.	Max.	Unit
Supply Voltage	V_{CC}	3.0	5.25	V
Ground	V_{SS}	0	0	V
Input High Voltage- 3.0 v	V_{IH}	2.4	V_{CC} + 0.5	V
Input High Voltage - 5.0 v	V_{IH}	2.4	V_{CC} + 0.5	V
Input Low Voltage - 3.0 v	V_{IL}	-0.3	0.4	V
Input Low Voltage - 5.0 v	V_{IL}	-0.3	0.4	V

DC AND OPERATING CHARACTERISTICS (Ta = 0 to 70 °C)

Item	Symbol	Test Conditions	VCC=3.0V		VCC=5.0 V± 5%		Units
			Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}	-1.0	1.0	-1.0	1.0	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ =V_{IH} or $\overline{OE}$ =V_{IH} or $\overline{WE}$ = V_{IL},$V_{I/O}$=V_{SS} to V_{CC}	-1.0	1.0	-1.0	1.0	µA
ROM Operating Supply Current	I_{CC1}	$\overline{CS}$ 1=V_{IL}, $\overline{CS}$ 2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, $I_{I/O}$=0 mA	-	-	-	10 + 1.1(f)	mA
RAM Operating Current	I_{CC2}	$\overline{CS}$ 1=V_{IH}, $\overline{CS}$ 2=V_{IL}, $I_{I/O}$=0 mA	-	-	-	7.0 + 1(f)	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ ≥ V_{CC}-0.2V V_{IN} ≤ 0.2V,V_{IN} ≥ V_{CC}-0.2V	-	-	-	30	µA
Output Low Voltage	V_{OL}	I_{OL}= 1.0 mA at 5.0 V		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -0.5 mA at 5.0 V	2.2	-	2.4	-	V

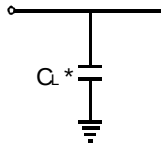
NOTE: $\overline{CS}$ = $\overline{CS}$ 1 & $\overline{CS}$ 2, $\overline{CS}$ 1 = ROMCSB, $\overline{CS}$ 2 = RAMCSB, f=1/cycle time

CAPACITANCE *(f =1MHz, Ta = 25 °C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input / Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

TEST CONDITIONS (Ta= 0 to 70 °C)

Parameter	Value	
	V_{CC} = 3.0 V	V_{CC} = 5.0 V
Input Pulse Level	0 to 3V	0 to 3V
Input Rise and Fall Time (10% to 90% VCC)	5 ns	5 ns
Input and Output Timing Reference Levels	1.5 V	1.5 V
Output Load	CL=100pF	CL=100pF



* Including scope and jig capacitance

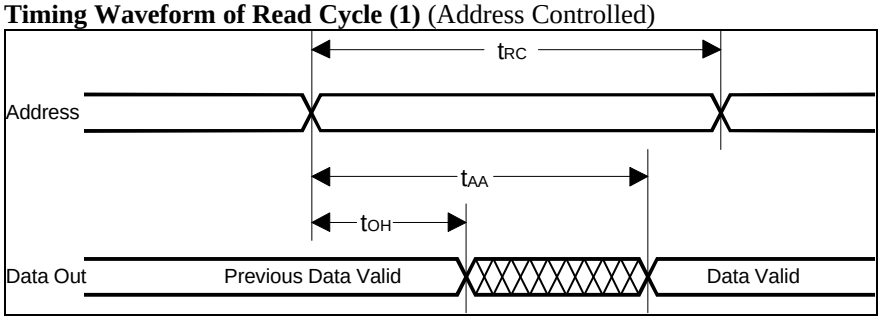
I. ROM Operation ($\overline{CS}_2$ = RAMCSB = VIH)

READ CYCLE

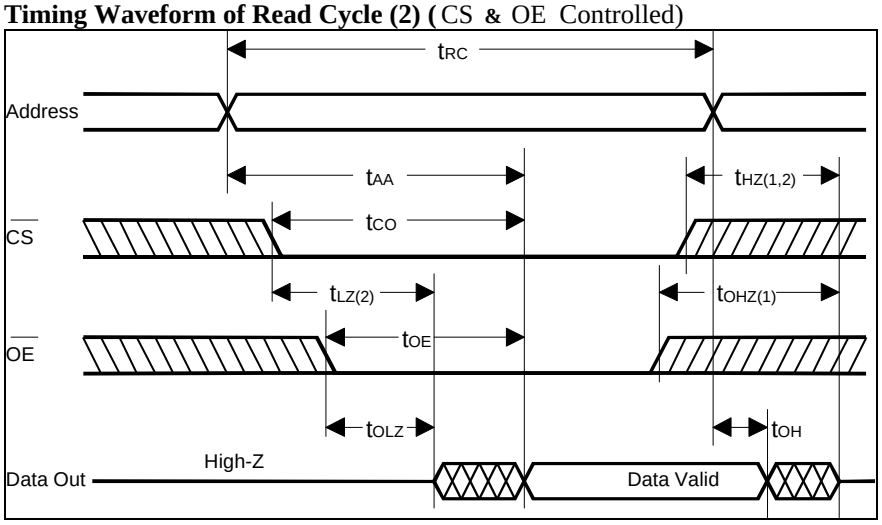
Parameter	Symbol	Vcc=3.0 V Worse Case		Vcc=5.0 V ± 5% Worse Case		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		70		ns
Address Access Time	t_{AA}		150		70	ns
Chip Select to Output	t_{CO}		150		70	ns
Output Enable to Valid Output	t_{OE}		65		45	ns
Chip Select to Low-Z Output	t_{LZ}	20		10		ns
Output Enable to Low-Z Output	t_{OLZ}	20		10		ns
Chip Disable to High-Z Output	t_{HZ}	0	30	0	15	ns
Output Disable to High-Z Output	t_{OHZ}	0	30	0	15	ns
Output Hold from Address Change	t_{OH}	8		7		ns

TIMING DIAGRAMS

Timing Waveform of Read Cycle (1) (Address Controlled)



Timing Waveform of Read Cycle (2) ($\overline{CS}$ **&** $\overline{OE}$ Controlled)



NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are referenced to the V_{OH} or V_{OL}.
2. At any given temperature and voltage condition t_{HZ}(max) is less than t_{LZ}(min) both for a given device and from device to device.
3. $\overline{CS}$ 2/RAMCSB is high for read cycle.
4. Address valid prior to or coincident with $\overline{CS}$ 1 transition Low.

II. SRAM Operation ($\overline{CS}$ 1 = ROMCSB = VIH)

READ CYCLE

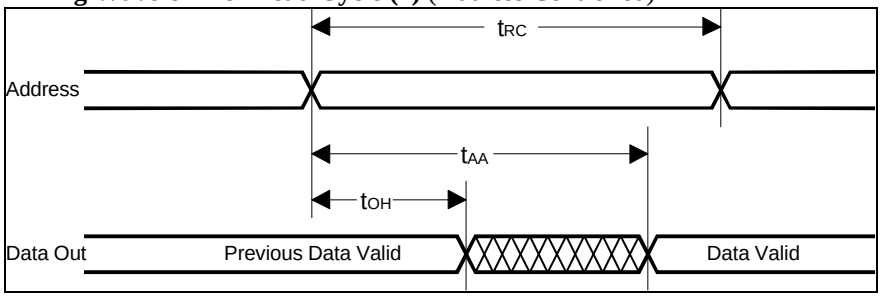
Parameter	Symbol	Vcc=3.0 V Worse Case		Vcc=5.0 V ± 5% Worse Case		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		70		ns
Address Access Time	t_{AA}		150		70	ns
Chip Select to Output	t_{CO}		150		70	ns
Output Enable to Valid Output	t_{OE}		65		45	ns
Chip Select to Low-Z Output	t_{LZ}	20		10		ns
Output Enable to Low-Z Output	t_{OLZ}	20		10		ns
Chip Disable to High-Z Output	t_{HZ}	0	30	0	15	ns
Output Disable to High-Z Output	t_{OHZ}	0	30	0	15	ns
Output Hold from Address Change	t_{OH}	15		10		ns

WRITE CYCLE

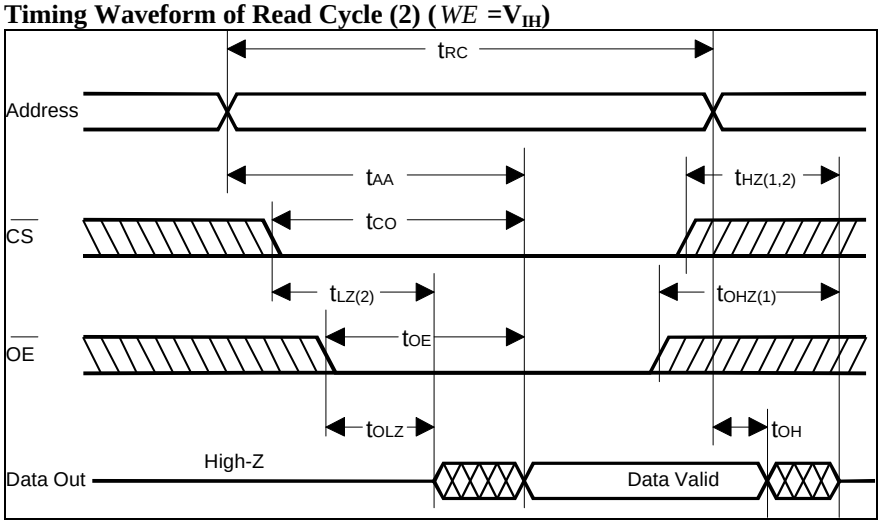
Parameter	Symbol	Vcc=3.0V		Vcc=5.0V± 5%		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	150		70		ns
Chip Select to End of Write	t_{CW}	100		60		ns
Address Valid to End of Write	t_{AW}	100		60		ns
Address Set-up Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	100		50		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to Output High-Z	t_{WHZ}	-	60	0	30	ns
Data to Write Time Overlap	t_{DW}	85		30		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Output Low-Z	t_{OW}	15		10		ns

TIMING DIAGRAMS

Timing Waveform of Read Cycle (1) (Address Controlled)



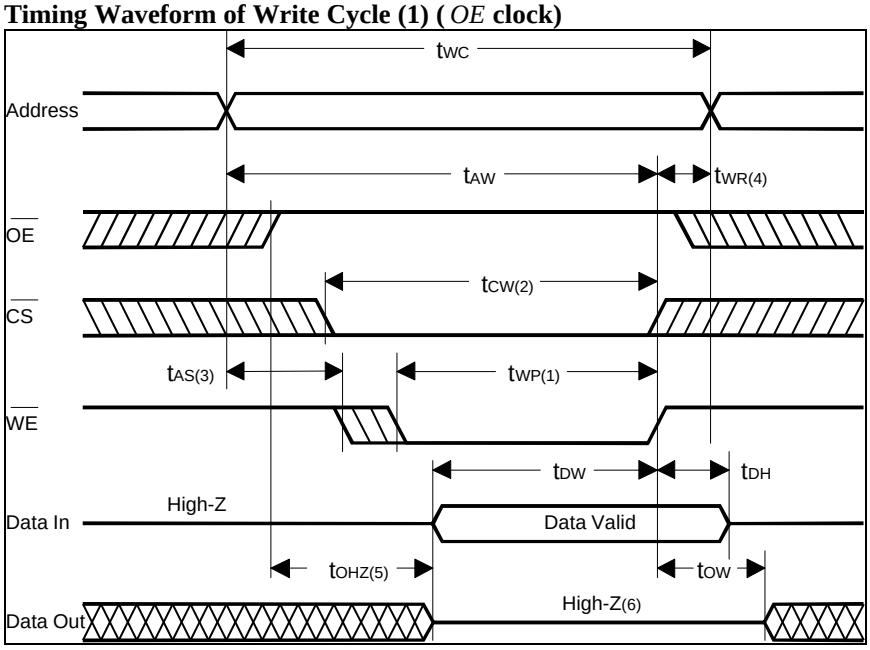
Timing Waveform of Read Cycle (2) ($\overline{WE}$ =V_{IH})



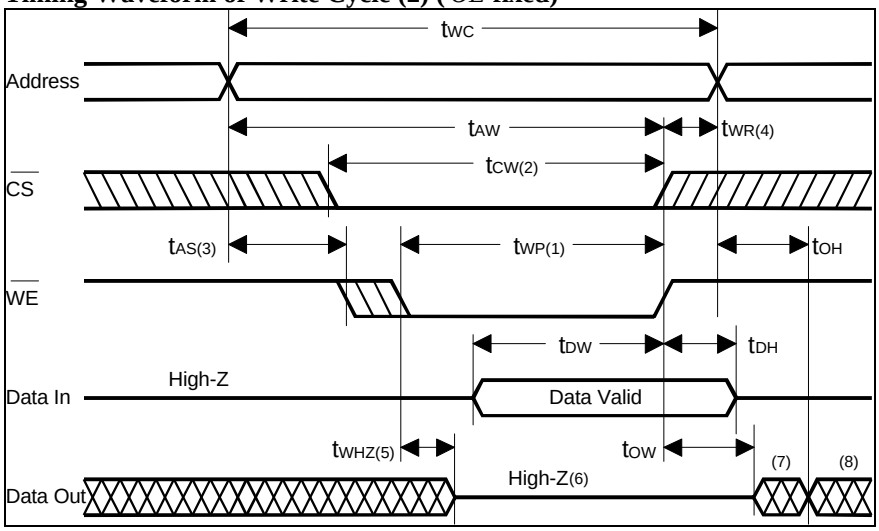
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are referenced to the V_{OH} or V_{OL}.
2. At any given temperature and voltage condition t_{HZ}(max) is less than t_{LZ}(min) both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.
4. Address valid prior to or coincident with $\overline{CS}$ 2 transition Low.

Timing Waveform of Write Cycle (1) ($\overline{OE}$ clock)



Timing Waveform of Write Cycle (2) ($\overline{OE}$ fixed)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ 2 and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ 2 going low and $\overline{WE}$ going low: A write end at the earliest transition among $\overline{CS}$ 2 going high and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS}$ 2 going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
5. if $\overline{OE}$, $\overline{WE}$ are in the read mode during this period, the I/O pins are in the outputs Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS}$ 2 goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
7. D_{OUT} is the same phase of the latest written data in this write cycle.
8. D_{OUT} is the read data of new address
9. $\overline{CS}$ 1= ROMCSB = V_{IH}

Functional Description/Truth Table

A0~A17	ROMCSB	RAMCSB	$\overline{WE}$	$\overline{OE}$	D0-D7	
X	H	H	X	X	Z	Standby
A0-A17	L	H	X	H	Z	Output Floating
A0-A17	L	H	X	L	Dout	ROM read
Only A0-A14 are vaild *	H	L	H	H	Z	Output Floating
Only A0-A14 are vaild *	H	L	H	L	Dout	RAM read
Only A0-A14 are vaild *	H	L	L	X	Din	RAM write

*A15-A17 must be fixed to "L" or "H"

Note: (1) It is forbidden that ROMCSB pin and RAMCSB pin will be "0" at same time.

(2) X means Don't Care.

PACKAGE OUTLINES AND DIMENSIONS

32-PIN PLASTIC TSOP

ITEM	MILLIMETERS	INCHES
A	20.0 ± .20	.780 ± .008
B	18.40 ± .10	.724 ± .004
C	8.20 max.	.323 max.
D	0.15 [Typ.]	.006 [Typ.]
E	.80 [Typ.]	.031 [Typ.]
F	.20 ± .10	.008 ± .004
G	.30 ± .10	.012 ± .004
H	.50 [Typ.]	.020 [Typ.]
I	.45 max.	.018 max.
J	0 ~ .20	0 ~ .008
K	1.00 ± .10	.039 ± .004
L	1.27 max.	.050 max.
M	.50	.020
N	0 ~5°	.500

NOTE: Each lead centerline is located within .25mm[.01 inch] of its true position [TP] at a maximum material condition.