



1M-Bit (128k × 8) Page Mode EEPROM

Features

Single 3.0-Volt Read and Write Operations

CMOS Flash EEPROM Technology

Page-write Endurance Cycles: 10^4
10 Years Data Retention

Low Power Consumption:

Active Current: 20 mA (Max.)
Standby Current: 15 μ A (Max.)

Fast Page-Write Operation

128 Bytes per Page
Page-Write Cycle: 5 ms (typical)
Complete Memory Rewrite: 5 sec. (typical)

Fast Access Time: 150 ns / 200 ns

Latched Address and Data

Automatic Write Timing with Internal V_{PP} Generation

End of Write Detection

Toggle Bit
DATA Polling

Hardware and Software Data Protection

TTL I/O Compatibility

JEDEC Standard Byte-Wide EEPROM Pinouts

Packages Available

LE28CW1001DT :32-pin TSOP (8mm × 20mm) Normal
LE28CW1001DTS :32-pin TSOP (8mm × 14mm) Normal

Product Description

The LE28CW1001D is a 128K×8 CMOS page mode EEPROM manufactured with SANYO's proprietary, high performance CMOS Flash EEPROM Technology. Breakthrough in EEPROM cell design and process architecture attain better reliability and manufacturability compared with conventional approaches. The LE28CW1001D performs write in a 3.0-volt-only power supply environment. Internal erase/program is transparent to the user. The LE28CW1001D conforms to JEDEC standard pinouts for byte-wide memories and is compatible with existing industry standard EPROM, flash EPROM and EEPROM pinouts.

Featuring high performance page write, the LE28CW1001D provides typical byte-write time of 39 μ sec. The entire memory, i.e.128K bytes, can be written in as little as 5 seconds using interface such as Toggle Bit and DATA Polling to indicate the completion of a write cycle. To protect against inadvertent write, the LE28CW1001D has on-chip hardware and software data protection schemes. Designed, manufactured and tested for a wide spectrum of applications, the LE28CW1001D is offered with page-write endurance 10^4 cycles. Data retention is rated at greater than 10 years.

The LE28CW1001D is best suited for application that require reprogrammable nonvolatile storage of program or data memory for laptop computers, desktop computers, medical instruments, laser printers, or copiers. For all system applications, the LE28CW1001D significantly improves performance and reliability, while lowering power consumption, when compared with floppy disk or EPROM approaches. In addition, the EEPROM technology makes convenient and economical updating of codes and control programs on-line possible. The LE28CW1001D improves flexibility while lowering the cost for program and configuration storage applications such as operating systems, BIOS, control programs, software I/O drivers, fonts, or archives.

To meet high density, surface mount requirements, the LE28CW1001D is offered in 32-pin TSOP package.

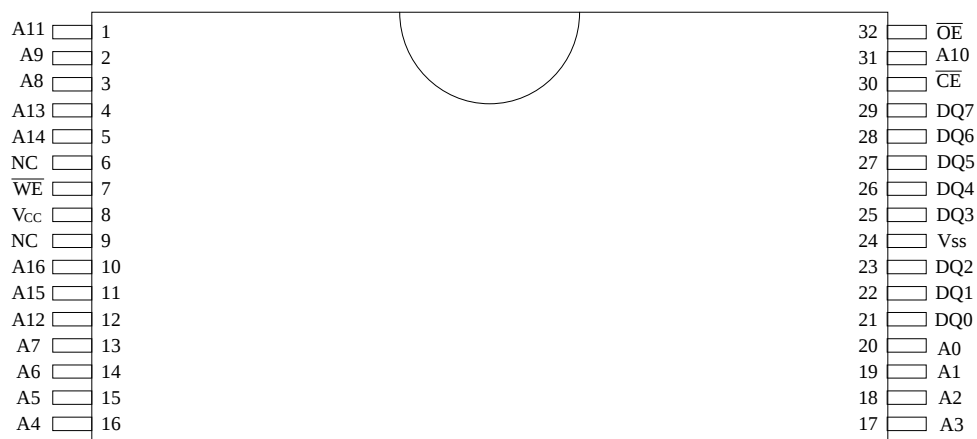
Device Operation

Both the high and medium endurance parts are identical in functionality and features. The LE28CW1001D is compatible to industry standard pinout and functionality.

*This product incorporate technology licensed from Silicon Storage Technology, Inc.
This preliminary specification is subject to change without notice.

LE28CW1001DT/DTS-15/20
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Preliminary Specifications



(Top View)

Figure 1: Pin Assignments for 32-pin TSOP

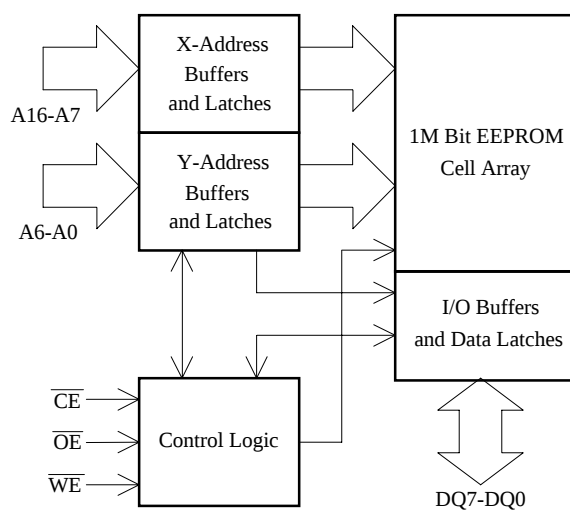


Figure2: Functional Block Diagram of LE28CW1001D

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Table 1: Pin Description

Symbol	Pin Name	Functions
A16-A0	Address Inputs	To provide memory address. Address are internally latched during write cycle.
DQ7-DQ0	Data Input/Output	To output data during read cycle and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when $\overline{OE}$ or $\overline{CE}$ is high.
$\overline{CE}$	Chip Enable	To activate the device when $\overline{CE}$ is low. Deselects and puts the device to standby when $\overline{CE}$ is high.
$\overline{OE}$	Output Enable	To activate the data output buffers. $\overline{OE}$ is active low.
$\overline{WE}$	Write Enable	To activate the write operation. $\overline{WE}$ is active low.
V_{CC}	Power Supply	To provide 2.7V ~ 3.6V.
V_{SS}	Ground	
NC	No Connection	Unconnected pins.

Table 2: Operation Modes Selection

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Standby	V_{IL}	X	X	High-Z	X
Write Inhibit	X	V_{IL}	X	High-Z / D_{OUT}	X
	X	X	V_{IH}	High-Z / D_{OUT}	X
Product Identification	V_{IL}	V_{IL}	V_{IH}	Manufacturer Code (BF)	$A16-A1 = V_{IL}$, $A9 = 12V$, $A0 = V_{IL}$
				Device Code (07)	$A16-A1 = V_{IL}$, $A9 = 12V$, $A0 = V_{IH}$

Table 3: Software Data Protection Command Code

Byte Sequence	To Enable Protection		To Disable Protection	
	Address *	Data	Address *	Data
0 Write	5555H	AAH	5555H	AAH
1 Write	2AAAH	55H	2AAAH	55H
2 Write	5555H	A0H	5555H	80H
3 Write			5555H	AAH
4 Write			2AAAH	55H
5 Write			5555H	20H

* Address format A14-A0 (Hex.)

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Table 4: Software Product ID Entry Command Code and Exit Command Code

Byte Sequence	Product ID Entry		Product ID Exit	
	Address	Data	Address*	Data
0 Write	5555H	AAH	5555H	AAH
1 Write	2AAAH	55H	2AAAH	55H
2 Write	5555H	80H	5555H	F0H
3 Write	5555H	AAH		
4 Write	2AAAH	55H		
5 Write	5555H	60H		

Notes for Software Product ID Command Code:

1. Command Code Address format: A14-A0 (Hex)
2. With A16-A1=0,
SANYO Manufacture Code = BFH is read with A0=0
LE28CW1001D Device Code =07H is read with A0=1
3. The device does not remain in Software product ID Mode if powered down.

Read

The LE28CW1001D product read operation is controlled by $\overline{CE}$ and $\overline{OE}$. The host must set both pins to the low level to acquire the output data. $\overline{CE}$ is used for chip selection. When $\overline{CE}$ is at the high level, the chip will be in the unselected state and only draw the standby current. $\overline{OE}$ is used for output control. The output pins go to the high-impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. See the timing waveforms (Figure 3) for details.

Write

The write operation starts when both $\overline{CE}$ and $\overline{WE}$ are at the low level. The write operation is executed in two stages. The first stage is a byte load cycle in which the host writes to the LE28CW1001D product internal page buffer. The second stage is an internal programming cycle in which the data in the page buffer is written to the nonvolatile memory cell array. In the byte-load cycle, the address is latched on the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs later. The input data is latched on the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. The internal programming cycle starts if either $\overline{WE}$ or $\overline{CE}$ remains high for 200 μ s (tBLCO). Once this programming cycle starts, the operation continues until the programming operation is completely done. This operation executes within 5ms (typical). Figures 4 and 5 show the $\overline{WE}$ and $\overline{CE}$ control write cycle timing diagrams, and Figure 11 shows the flowchart for this operation.

In the page write operation, 128 bytes of data can be written to the LE28CW1001D product internal page buffer before the internal programming cycle. All the data in the page buffer is written to the memory cell array during the 5m (typical) internal programming cycle. Therefore the LE28CW1001D product page write function can rewrite all memory cells in 5 seconds (typical). The host can perform any other activities desired, such as moving data at other locations within the system and preparing the data required for next page write, during the period prior to the completion of the internal programming cycle. In the given page write operation, all the data bytes loaded into the page buffer must be for the same page address specified by address lines A7 through A16. All data was not explicitly loaded into the page buffer is set to FFH.

Figure 4 shows the page write cycle timing diagram. If the host loads the second data byte into the page buffer within the 100 μ s byte load cycle time (tBLC) after the first byte load cycle the LE28CW1001D product stop in the page load cycle thus allowing data to be loaded continuously. The page load cycle terminates if additional data is not loaded into the internal page buffer within 200 μ s (tBLCO) after the previous byte load cycle, as in the case where $\overline{WE}$ does not switch from high to low after the last $\overline{WE}$ rising edge. The data in the page buffer can be rewritten in the next byte load cycle.

The page load period can continue indefinitely as long as host continues to load data into the device within the 100 μ s byte load cycle. The page that is loaded is determined by the page address of the last byte loaded.

Detecting the Write Operation State

The LE28CW1001D product provides two functions for detecting the completion of the write cycle. These functions are used to optimize the system write cycle time. These functions are based on detecting the states of the $\overline{DATA}$ Polling bit (DQ7) and the toggle bit (DQ6).

$\overline{DATA}$ Polling (DQ7)

The LE28CW1001D products output to DQ7 the inverse of the last data loaded during the page and byte load cycles when the internal programming cycle is in progress. The last data loaded will be read from DQ7 when the internal programming cycle completes. Figure 6 shows the $\overline{DATA}$ Polling cycle timing diagram and Figure 12 shows the flowchart for this operation.

Toggle Bit (DQ6)

Data values of 0 and 1 are output alternately for DQ6, that is DQ6 is toggled between 0 and 1, during the internal programming cycle. When the internal programming cycle completes this toggling is stopped and the device becomes ready to execute the next operation. Figure 7 shows the toggle bit timing diagram and Figure 12 shows the flowchart for this operation.

Data Protection

Hardware Data Protection

Noise and glitch protection: The LE28CW1001D does not execute write operations for $\overline{WE}$ or $\overline{CE}$ pulses that are 15 ns or shorter.

Power (V_{CC}) on and cutoff detection: The programming operation is disabled when V_{CC} is 2.5 V or lower.

Write inhibit mode: Writing is disabled when $\overline{OE}$ is low and either $\overline{CE}$ is high or $\overline{WE}$ is high. Use this function to prevent writes from occurring when the power is being turned on or off.

Software Data Protection (SDP)

The LE28CW1001D implements the optional software data protection function recognized by JEDEC. This function requires that a 3-byte load operation to be performed before a write operation data load. The 3-byte load sequence starts a page load cycle without activating any write operation. Thus this is an optimal protection scheme for unintended write cycles triggered by noise associated with powering the chip on or off. Note that the

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LE28CW1001D is shipped with the software data protection disabled.

The software data protection circuit is activated by executing a 3-byte byte load cycle. (See Figure 8). This causes the device to automatically enter data protection mode. After this, write operations require a 3-byte byte load cycle to be executed in advance. A 6-byte write sequence is required to switch the device out of this protection mode. Figure 9 shows the timing diagram. If a write operation is attempted in software protection mode, all device functions are disabled for 200 μ s. Figure 13 shows the flowchart for this operation.

Product Identification

The device identification code is used for recognized the device and its manufacturer. This mode can be used by hardware and software. The hardware operating mode is used to recognize algorithms that match the device when an external programming unit is used. Also, users systems can recognize the product number using software product identification mode. Figure 14 shows the flowchart for this operation. The manufacturer and device codes are the same in both modes.

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Absolute Maximum Ratings at Ta=25°C

Symbol	Parameter	Ratings	Unit	Note
V _{CC max}	Supply voltage	-0.5V ~ 4.6V	V	1
V _{IN}	Input pin voltage	-0.5V ~ V _{CC} + 0.5V	V	1,2
V _{OUT}	DQ pin voltage	-0.5V ~ V _{CC} + 0.5V	V	1,2
V _{A9}	A9 pin voltage	-0.5V ~ 14V	V	1,3
Pd max	Allowable power dissipation	600	mW	1,4
Topr	Operating temperature	0 ~ +70	°C	1
Tstg	Storage temperature	-65 ~ +150	°C	1

- Notes: 1. The device may be destroyed by the application of stresses in excess of the maximum ratings.
2. -1.0V to V_{CC}+1.0V for pulses less than 20ns
3. -1.0V to +14V for pulses less than 20ns
4. Ta=25°C

DC Recommended Operating Range at Ta=0 to +70°C

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply voltage	2.7	3.0	3.6	V
V _{IL}	Input low-level voltage	-0.3		0.6	V
V _{IH}	Input high-level voltage	2.0		V _{CC} + 0.3	V

DC Electrical Characteristics at Ta=0 to +70°C, V_{CC} =2.7V ~ 3.6V

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I _{CCR}	Power Supply Current (Read)			20	mA	$\overline{CE}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$, all DQs open Address inputs= V _{IH} / V _{IL} , f=1/tRC(min.)
I _{CCW}	Power Supply Current (Write)			30	mA	$\overline{CE}=\overline{WE}=V_{IL}$, $\overline{OE}=V_{IH}$
I _{SB1}	Standby V _{CC} Current (TTL input)			1	mA	$\overline{CE}=V_{IH}$, all DQs open Other inputs= V _{IH} / V _{IL}
I _{SB2}	Standby V _{CC} Current (CMOS input)			15	μA	$\overline{CE}=V_{CC} - 0.3V$, all DQs open Other inputs= V _{IH} / V _{IL}
I _{LI}	Input Leakage Current			10	μA	V _{IN} = V _{SS} ~ V _{CC} , V _{CC} = V _{CC max}
I _{LO}	Output Leakage Current			10	μA	V _{IN} = V _{SS} ~ V _{CC} , V _{CC} = V _{CC max}
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 2.1mA, V _{CC} = V _{CC min}
V _{OH}	Output High Voltage	2.4			V	I _{OH} = -400μA, V _{CC} = V _{CC min}

Power-up Timings

Symbol	Parameter	Minimum	Units
t _{PU_READ}	Power-up to Read Operation	10	ms
t _{PU_WRITE}	Power-up to Write Operation	10	ms

Capacitance at Ta=25°C, V_{CC} =2.7V ~ 3.6V, f=1MHz

Symbol	Parameter	Maximum	Units	Test Condition
C _{DQ}	DQ Pin Capacitance	12	pF	V _{DQ} = 0V
C _{IN}	Input Capacitance	6	pF	V _{IN} = 0V

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AC Characteristics at Ta=0 to +70°C, V_{CC} =2.7V ~ 3.6V

AC Condition of Test

Input Rise/Fall Time..... 10 ns

Output Load..... 1 TTL Gate and C_L=100pF

Read Cycle Timing Parameters

Symbol	Parameter	LE28CW1001DT/DTS-15		LE28CW1001DT/DTS-20		Limits
		Min.	Max.	Min.	Max.	
t _{RC}	Read Cycle Time	150		200		ns
t _{CE}	Chip Enable Access Time		150		200	ns
t _{AA}	Address Access Time		150		200	ns
t _{OE}	Output Enable Access Time		90		100	ns
t _{CLZ}	$\overline{CE}$ Low to Active Output	0		0		ns
t _{OLZ}	OE Low to Active Output	0		0		ns
t _{CHZ}	$\overline{CE}$ Low to High-Z Output		50		50	ns
t _{OHZ}	OE Low to High-Z Output		50		50	ns
t _{OH}	Output Hold from Address Change	0		0		ns

Page-Write Cycle Timing Parameters

Symbol	Parameter	Limits			Units
		Min.	Typ.	Max.	
t _{WC}	Write Cycle (erase and program)		5	10	ms
t _{AS}	Address Setup Time	0			ns
t _{AH}	Address Hold Time	100			ns
t _{CS}	$\overline{WE}$ and $\overline{CE}$ Setup Time	0			ns
t _{CH}	$\overline{WE}$ and $\overline{CE}$ Hold Time	0			ns
t _{OES}	$\overline{OE}$ High Setup Time	0			ns
t _{OEH}	$\overline{OE}$ High Hold Time	0			ns
t _{CP}	$\overline{CE}$ Pulse Width	120			ns
t _{WP}	$\overline{WE}$ Pulse Width	120			ns
t _{DS}	Data Setup time	100			ns
t _{DH}	Data Hold time	0			ns
t _{BLC}	Byte Load Cycle Time	0.1		100	μs
t _{BLCO}	Byte Load Cycle Time-out	200			μs

Figure 3: Read Cycle Timing Diagram

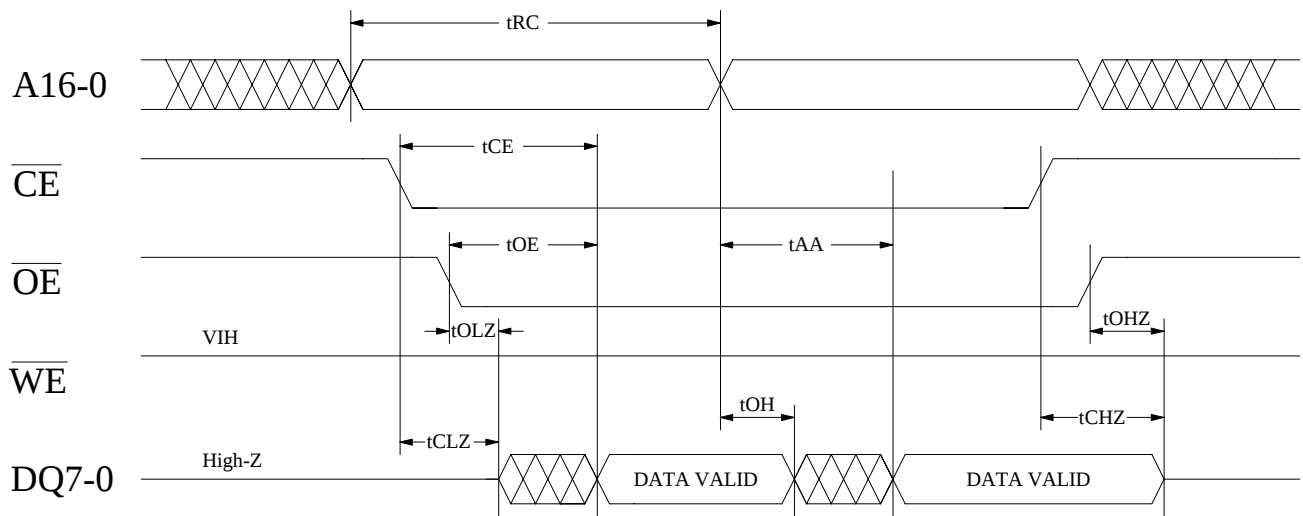
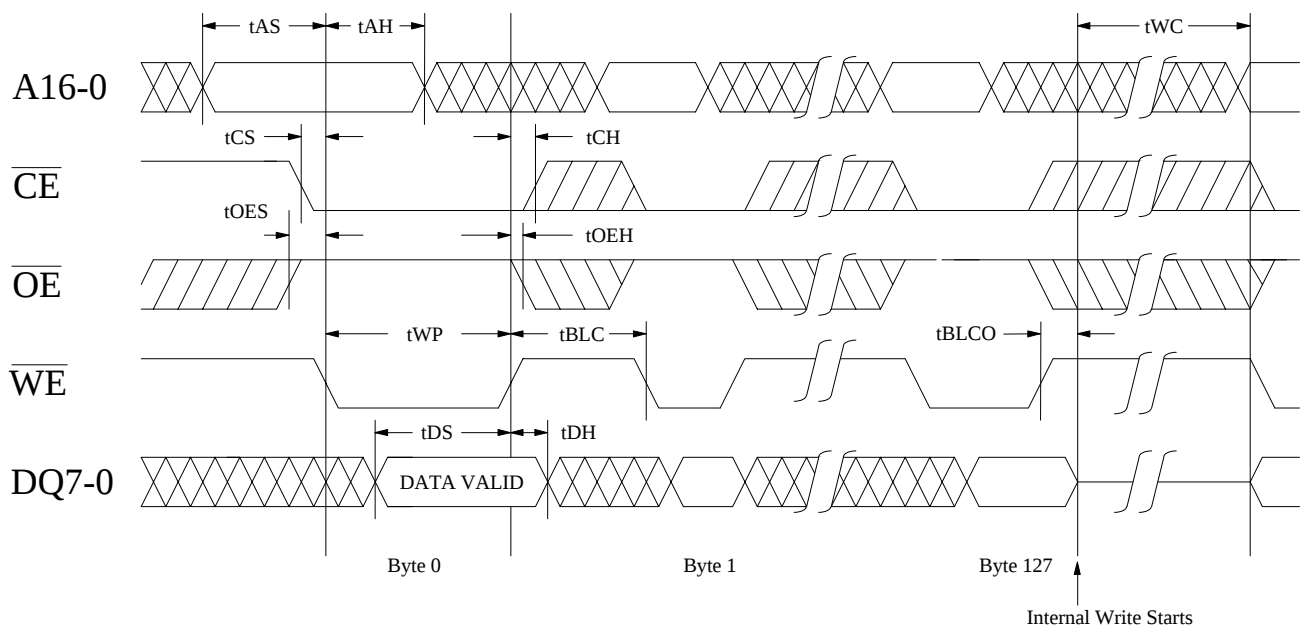


Figure 4: $\overline{WE}$ Controlled Page Write Cycle Timing Diagram



The diagram illustrates the timing for an internal write operation. The signals shown are:

- A16-0**: Address bus, showing a sequence of data bytes (Byte 0, Byte 1, ..., Byte 127) with a break between Byte 1 and Byte 127.
- CE**: Chip Enable, which transitions from high to low at the start of the write sequence and returns to high after the last byte.
- OE**: Output Enable, which is active-low and remains high throughout the write operation.
- WE**: Write Enable, which transitions from high to low at the start of the write sequence and returns to high after the last byte.
- DQ7-0**: Data bus, showing the data being written. A "DATA VALID" period is indicated for the first byte (Byte 0).

Key timing parameters are labeled:

- t_{AS} : Address Setup time before the first data byte.
- t_{AH} : Address Hold time after the last data byte.
- t_{CP} : Command Pulse width (CE low).
- t_{BLC} : Burst Length Count time (WE low).
- t_{BLCO} : Burst Length Count Over time (WE high).
- t_{OES} : Output Enable Setup time (OE high).
- t_{OE} : Output Enable Pulse width (OE low).
- t_{CS} : Command Setup time (CE low).
- t_{CH} : Command Hold time (WE high).
- t_{DS} : Data Setup time before the first data byte.
- t_{DH} : Data Hold time after the last data byte.
- t_{WC} : Write Cycle time (from CE low to CE high).

An arrow at the bottom right indicates "Internal Write Starts" at the beginning of the first data byte.

Figure 7: Toggle Bit Timing Diagram

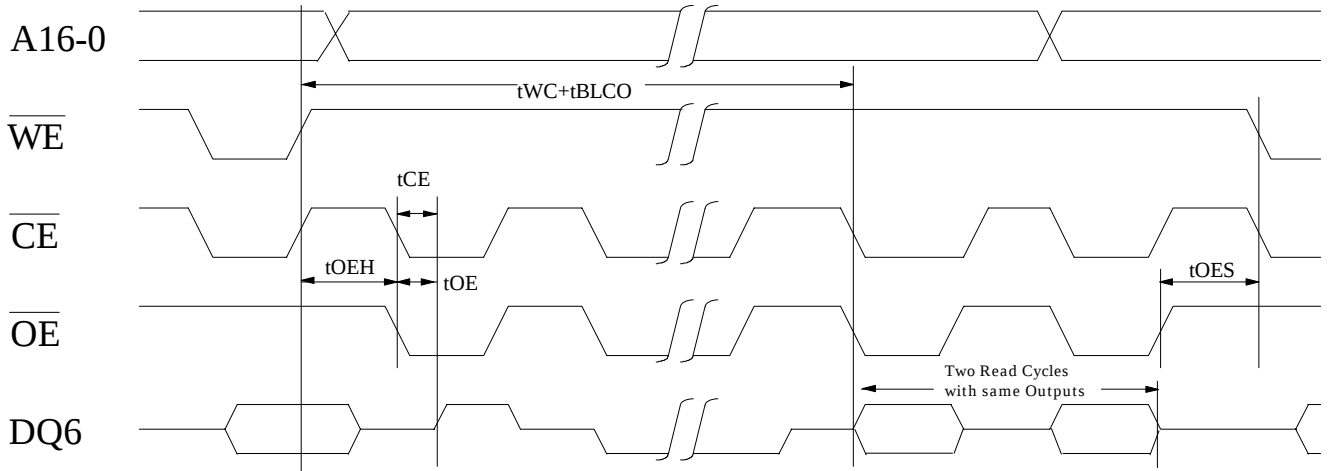
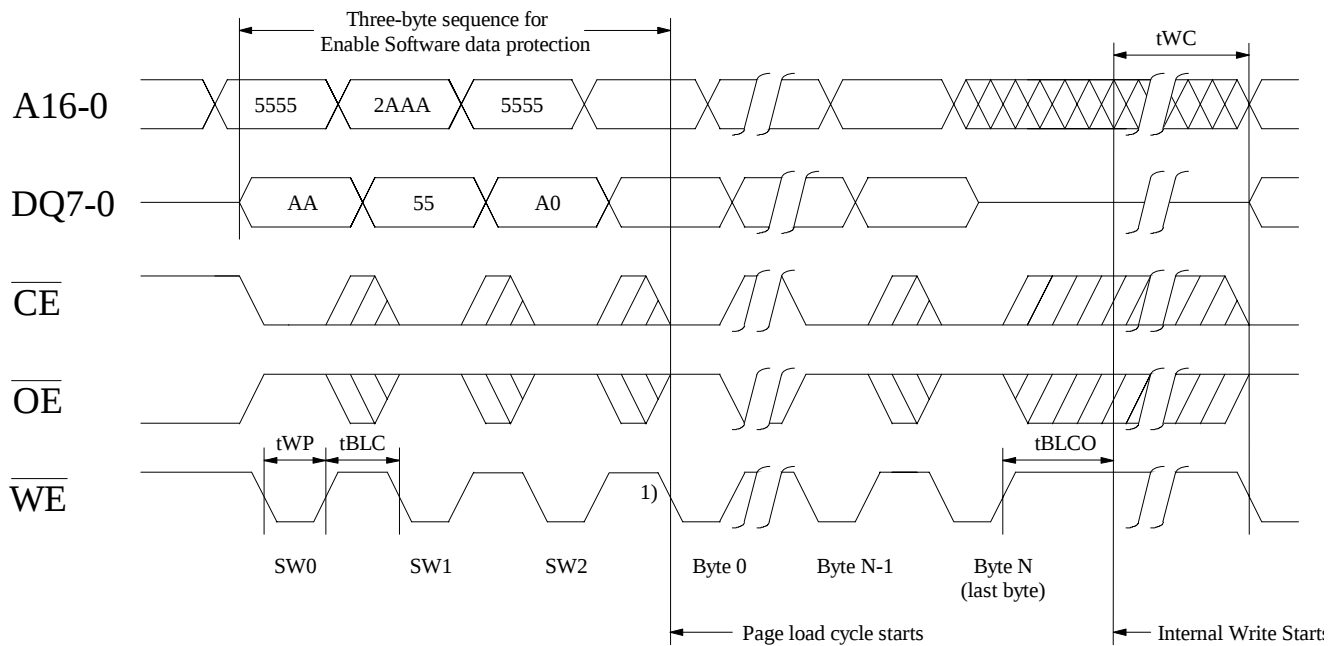


Figure 8: Enable Software Data Protection Page Write Timing Diagram



Note 1): The time between enabling Software Data Protect and the page load must be less than tBLCO

Figure 9: Disable Software Data Protection Timing Diagram

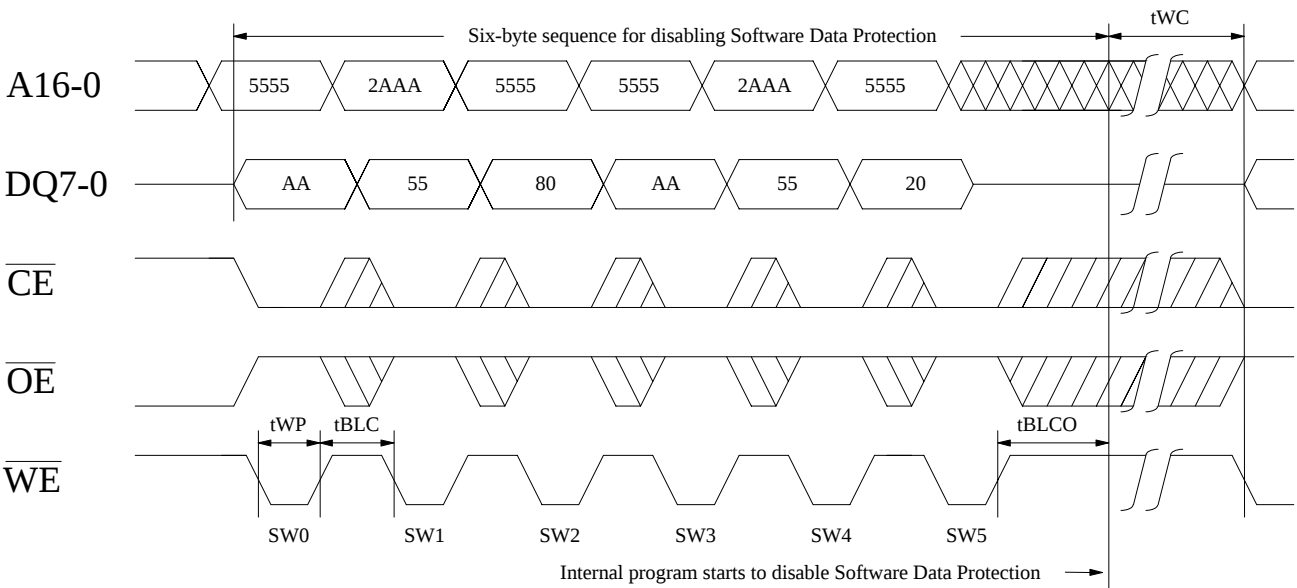
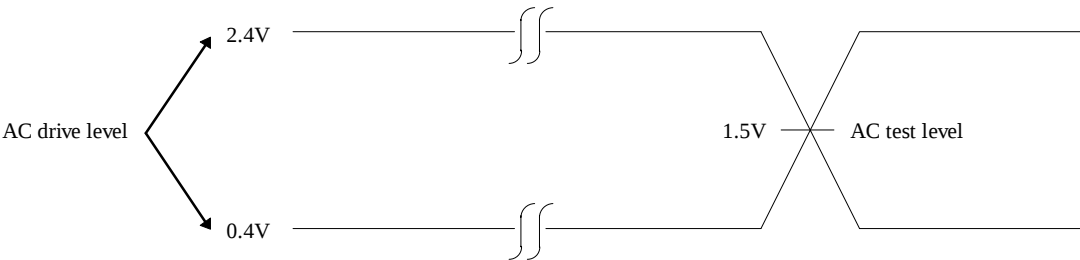


Figure 10: AC Input/Output Reference Waveform



The input rise and fall times (10%↔90%) must not exceed 10ns.

Figure 11: Write Algorithm

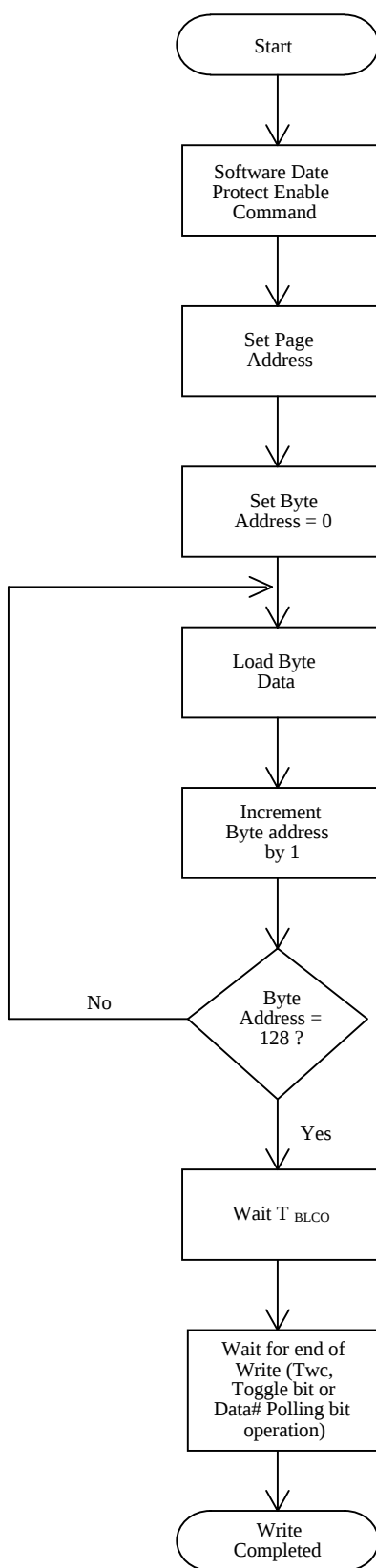


Figure 12: Write Wait Options

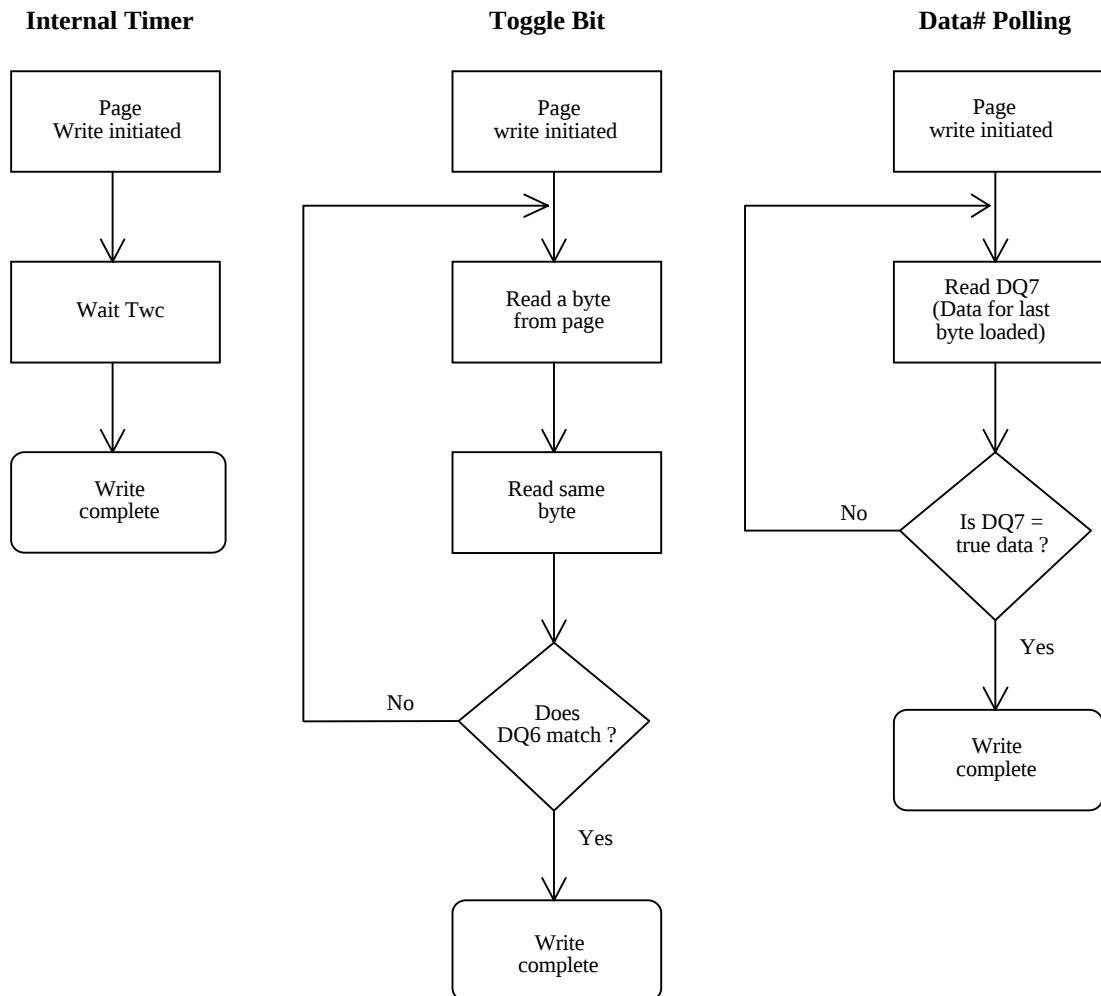


Figure 13: Software Data Protect Disable Command Sequence

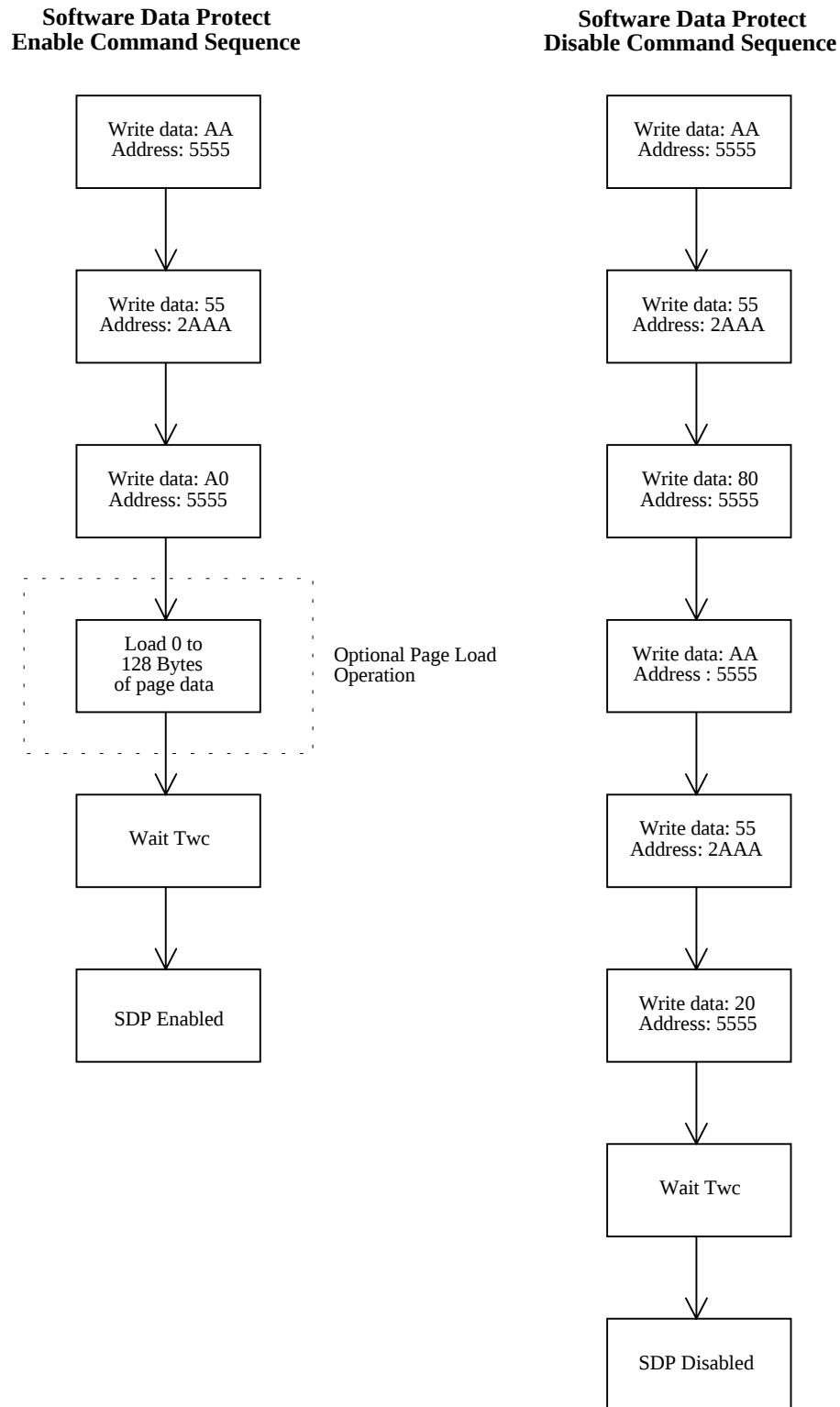
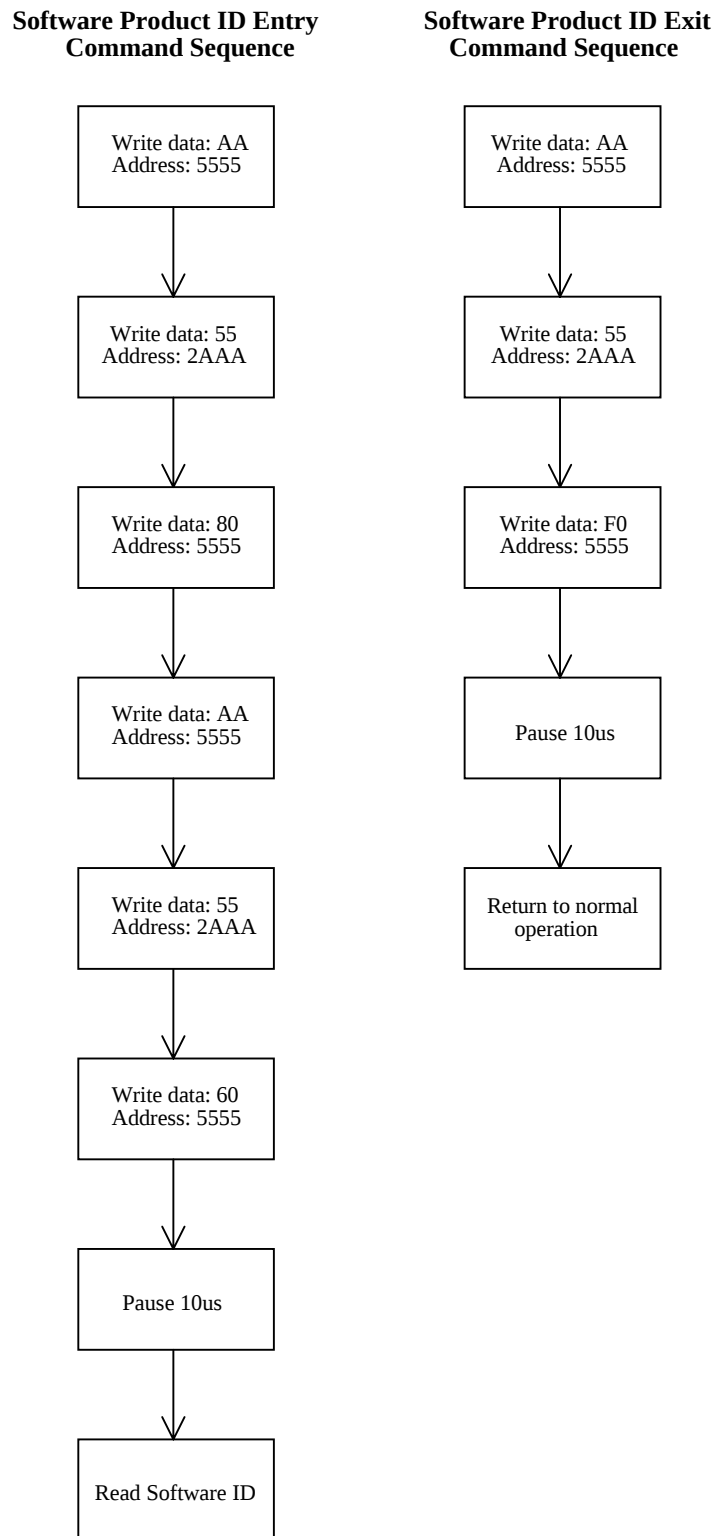


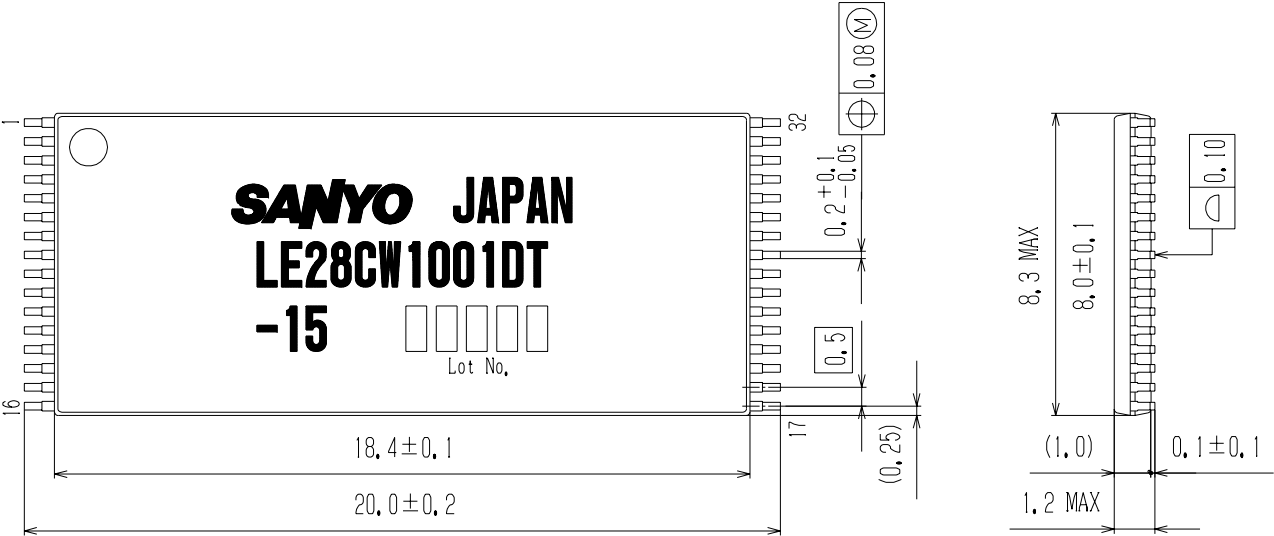
Figure 14: Software Product Command Codes



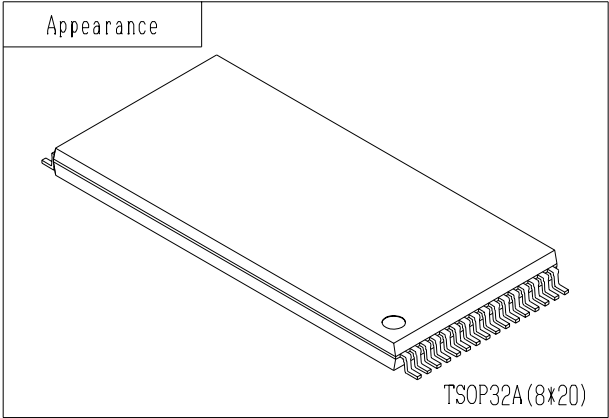
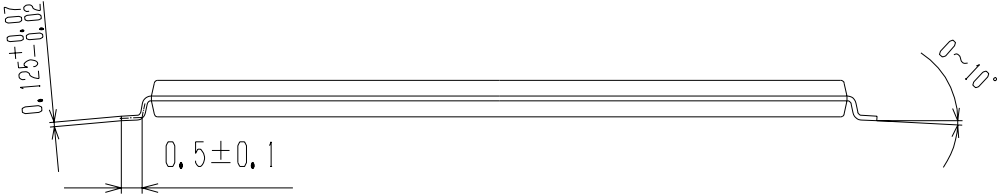
OUTLINE DRAWING



SANYO Package Code	EIAJ Package Code	JEDEC Package Code	TYPE NUMBER	ENACT No.	Mass (g)	Unit
TSOP32A(8*20)	—	—	LE28CW1001DT-15	S-039	0.25	



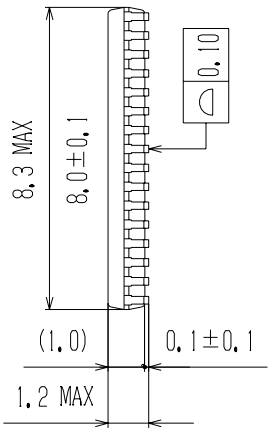
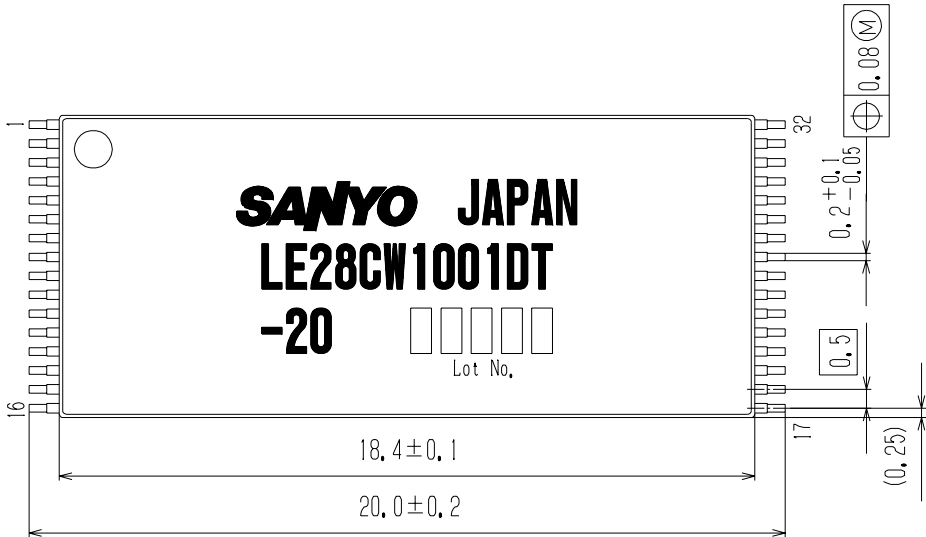
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T. sasaki
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A. kasahara
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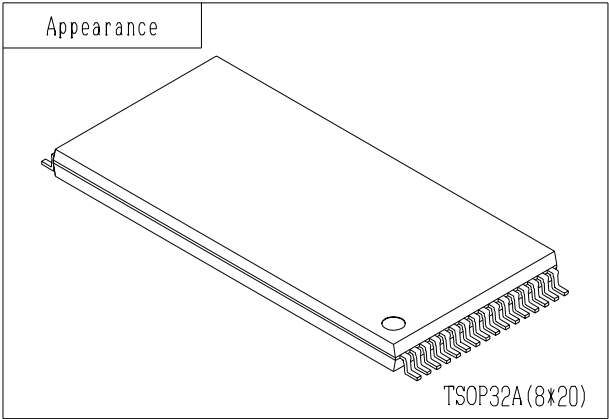
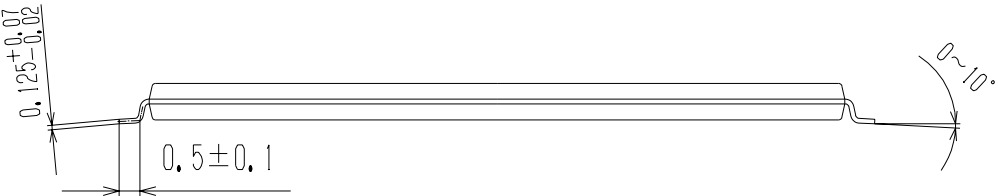
OUTLINE DRAWING



SANYO Package Code	EIAJ Package Code	JEDEC Package Code	TYPE NUMBER	ENACT No.	Mass (g)	Unit
TSOP32A (8*20)	—	—	LE28CW1001DT-20	S-039	0.25	



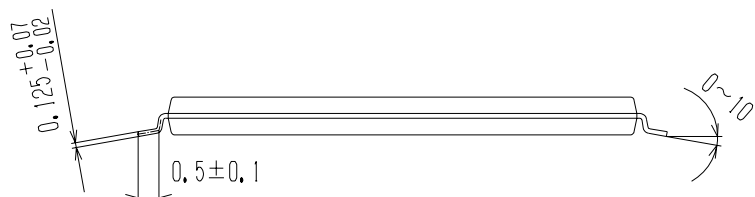
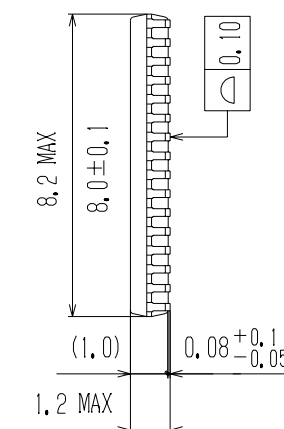
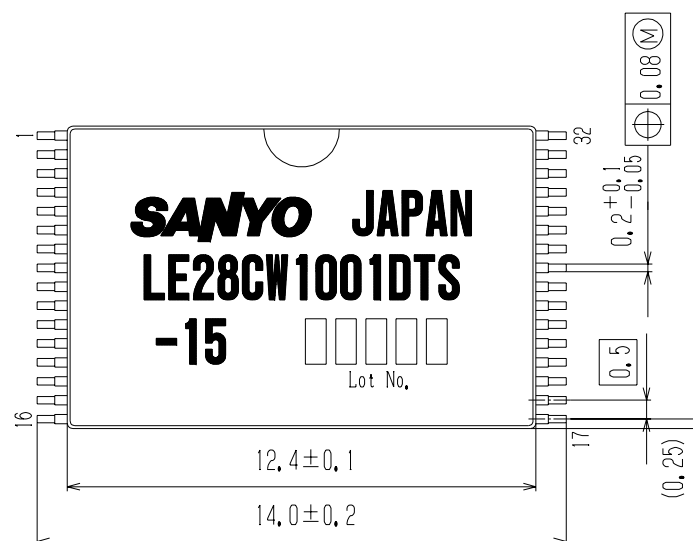
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A. kasahara
DATE
2000. 4. 17



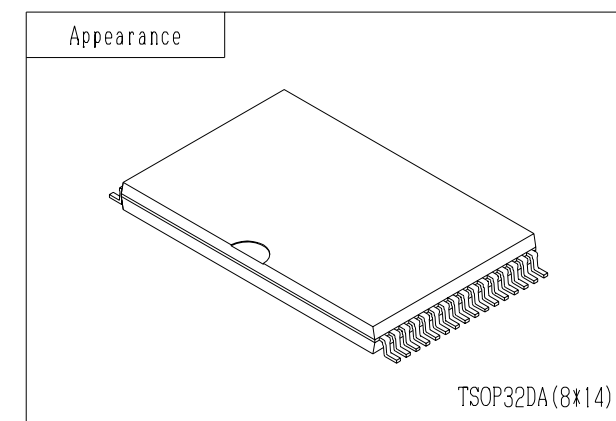
OUTLINE DRAWING

SANYO

SANYO Package Code	EIAJ Package Code	JEDEC Package Code	TYPE NUMBER	ENACT No.	Mass (g)	Unit
TSOP32DA(8×14)	—	—	LE28CW1001DTS-15	S-041	0.25	mm



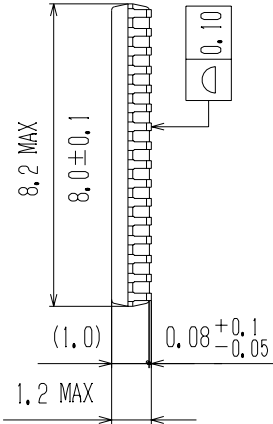
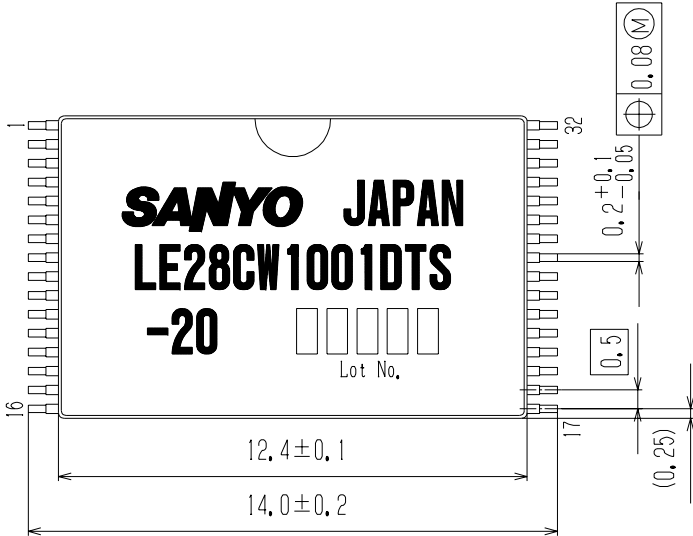
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OUTLINE DRAWING



SANYO Package Code	EIAJ Package Code	JEDEC Package Code	TYPE NUMBER	ENACT No.	Mass (g)	Unit
TSOP32DA (8×14)	—	—	LE28CW1001DTS-20	S-041	0.25	



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