SANYO

4M (512k × 8bits) Serial Flash EEPROM

Features

CMOS Flash EEPROM Technology
Single Volt Read and Write Operations
LE25FV401T : 2.7~3.6V
Sector Erase Capability: 2048 Bytes per sector
Operating Frequency: 20MHz
Low Power Consumption
Active Current (Read): 10 mA (Max.)
Standby Current: 20 µA (Max.)
Serial Peripheral Interface (S.P.I.) mode 0,3
High Read/Write Reliability
Sector-write Endurance Cycles: 10^5
10 Years Data Retention
Self-timed Erase and Programming
Byte Programming : 25 µs (Max.)
Sector Erase : 0.7s(Max)
Sector-write Endurance Cycles
less than 10^4 **: 25ms(Max)**
End of Write Detection
Status Register Read
Hardware Data Protection
$\overline{WP}$: pull up
Packages Available: MSOP8(225mil)

Product Description

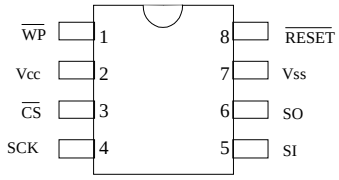
The LE25FV401T is a 512K x 8 CMOS sector erase, byte programmable serial Flash EEPROM. The LE25FV401T is manufactured using SANYO's proprietary, high performance CMOS Flash EEPROM technology. Breakthroughs in EEPROM cell design and process architecture attain better reliability and manufacturability compared with conventional approaches. LE25FV401T erases and programs with single power supply.

LE25FV401T conforms to Serial Peripheral Interface (S.P.I.).

Featuring high performance programming, the LE25FV401T byte programs in 25 µs max., sector (2048 bytes) erases in 25ms max. Both program and erase times can be optimized using interface feature such as Status Register to indicate the completion of the write cycle. To protect against an inadvertent write, the LE25FV401T has on chip hardware data protection scheme.

Designed, manufactured, and tested for a wide spectrum of applications, the LE25FV401T is offered with a guaranteed sector write endurance of 10^5 cycles. Data retention is rated greater than 10 years.

The LE25FV401T is best suited for applications that require re-programmable nonvolatile mass storage of program or data memory.



for 8-pin MSOP

Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the command register through serial input (SI). The addresses and data of Commands are latched to be used to operate functions such as Read,Sector_Erase, Byte_Program and so on.

Fig.3 and Fig.4 contain the timing waveforms of serial input and output. By setting CS# to LOW, the device is selected. And commands, addresses, and dummy bits can be let in serially through SI port. When the device is in Read or Status Register Read mode, SO pin is in Low-impedance state. And the requested data can be read out from MSB (most significant bit) synchronously with the falling edge of SCK.

*This product incorporate technology licensed from Silicon Storage Technology, Inc.
This preliminary specification is subject to change without notice.

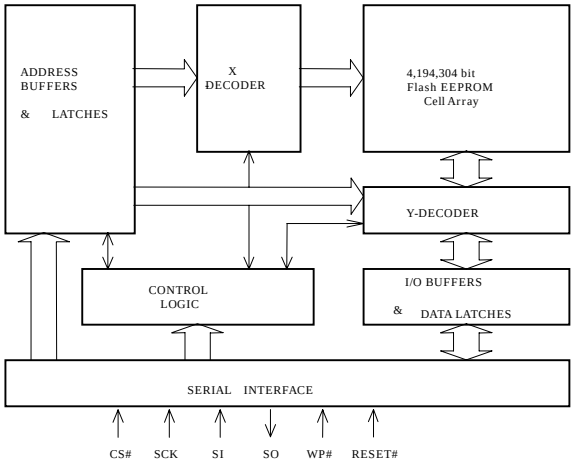


Figure2: Functional Block Diagram of LE25FV401T

Table1: Pin Description

Symbol	Pin Description	Functions
SCK	Serial Clock	To control the timing of serial data input and output. To latch input data and addresses synchronously at the rising edge of SCK, and read out output data synchronously at this falling edge.
SI	Serial Input	To input data or addresses serially from MSB to LSB (Least Significant Bit).
SO	Serial Output	To output data serially from MSB to LSB.
CS#	Chip Select	To activate the device when this pin is LOW. To deselect and put the device to standby mode when High.
WP#	Write Protect	To prevent inadvertent write when this pin is LOW. WP# is connected internally to the Vcc.
Vcc	Power Supply	To provide 2.7V to 3.6V supply.
Vss	Ground	
RESET#	Reset	To prevent inadvertent writes by setting this pin to LOW during system power-up. As RESET# is connected to Vcc internally, leave this pin open when this function is not necessary.

Table2: Commands Summary

Command	1st bus cycle	2nd bus cycle	3rd bus cycle	4th bus cycle	5th bus cycle	6th bus cycle
	OPcode	Address	Address	Address	Data / OPcode	Dummy
Read	FFH	A23-A16	A15-A8	A7-A0	X	X
Sector Erase	20H	A23-A16	A15-A8	X	D0H	X
Byte Program	10H	A23-A16	A15-A8	A7-A0	PD	X
Status Register	9FH					
Reset	FFH					
Read ID	90H	X	X	A7-A0	X	X

Definition for table 2:
1. X= don't care, H= number in hex.
2. A19-A23 are don't care for all commands, A8-A10 of Sector Erase,A1-A7 of Read ID,and A8-A10 of Protect Block Write are don’t care.
3. PD= Program data
4. Reset Command is effective when the device is only in Erase or Program sequence (in tSE,tBE or tBP period).

Command Definition

Table 2 contains a command list and a brief summary of the commands. The following is a detailed description of the options initiated by each command.

Read

Fig.5 shows the timing waveform of read operation. The read operation is initiated by READ command. After writing OPcode of "FFH" and following 24bit address and 16 dummy bits, SO is transformed into Low-impedance state, and the specified addresses' data are read out synchronously with SCK clock. While the SCK clock is continuously on, the device counts up the next address automatically and reads the data in order. When the address reaches its maximum, while the read operation still be continuing, the address is reset to the lowest one, and the device continues reading data from the beginning.

When CS# is set High so as to deselect the device, the read operation terminates with the output in High-impedance state. Do not execute read operation while the device is in Program or Erase Cycle to prevent inadvertent writes.

Status_Register Read

Fig.6 shows the timing waveform of Status_Register Read.

Status_Register can be read while the device is in Program or Erase mode. As is shown in the table below, the LSB (Least Significant Bit) of Status_Register is set to BSY# and the Fifth Bit of Status_Register is set to HUNG_UP with other bits intact. By setting CS# to LOW and writing "9FH" in command register, the contents of the Status_Register come out from MSB. The LSB of the Status_Register stands for if the device is busy or not. Therefore, "0" stands for busy and "1" for not in Program or Erase mode. The Fifth Bit of the Status_Register stands for if the sector erase is succeed or not.It is shown that the fifth bit becomes "1" when the sector erase passed the regulated limit time, and Sector Erase did not succeed,the device is hanging up.In this case,the device is locked and a busy state,and isn't ended automatically. Therefore, the reset operation by the command or the power supply is turned on again. When CS# goes High, Status Register reading terminates with the output pin in High-impedance state.

7(MSB)	6	5	4	3	2	1	0(LSB)
X	X	HUNG_UP	X	X	X	X	BSY#

Sector_Erase

Fig.7 shows the timing waveform of Sector_Erase. Sector_Erase command consists of 6 bus cycles from 1st bus cycle to 6th bus cycle. This command stages the device for electrical erasing of all bytes within a sector. A sector contains 2048 bytes. This sector erasability enhances the flexibility and usefulness of the LE25FV401T, since most applications only need to change a small number of bytes or sectors, not the entire chip. To execute the Sector_Erase operation, erase address, 2nd OPcode (D0H) and Dummy bits must be written to the command register after writing 1st OPcode of (20H). This two-step sequence ensures that only memory contents within the addressed sector are erased and other sectors are not inadvertently erased. The erase operation begins with the rising edge of the CS# pulse and terminates automatically by using an internal timer. Termination of this mode is found out by using Status Register Read.

Byte_Program

Fig.8 shows the timing waveform of Byte_Program. Byte_Program command consists of 6 bus cycles from 1st bus cycle to 6th bus cycle, and stages the device for Byte programmable. To execute the Byte_Program operation, program address, program data and Dummy bits must be written to the command register after writing the OPcode of (10H). The program operation begins with the rising edge of the CS# pulse and terminates automatically by using an internal timer. Termination of this mode is found out by using Status Register Read.

Read_ID

Fig.9 shows the timing waveform of Read_ID operation. The Read_ID command consists of 6 bus-cycles and read out manufacture code or device code which are indicated by the content of A0 synchronously with SCK 's falling edges. By setting "A0" to 0, manufacture code of "62H" can be read out from MSB. Similarly, by setting "A0" to 1, device code of "08H" are read out from MSB. This command is not executed for the duration of tBP(Programming Time),tSE(Sector Erase Time). When CS# is set High so as to deselect the device, the Read_ID operation terminates with the output in High-impedance state.

Reset

Fig.10 shows the timing waveform of Reset operation. Reset operation is effective while the device is already in Program or Erase mode. But the data of specified address are not guaranteed. The Reset Command can be provided as a means to safely abort the Program or Erase Command sequences. Following 4^{th} bus cycles (erase or program) with a write of (FFH) in 5^{th} bus cycle will safely abort the operation. Memory contents will not be altered.

Hardware Write Protection

Setting WP# to LOW prevents inadvertent writes by inhibiting write operation.To prevent inadvertent writes during system power-up, LE25FV401T has power-on-reset circuit.

As WP# is connected internally to the Vcc, don't connect externally to any nodes when this function is not necessary. To perform power up more safely, the usage of RESET# is recommended as follows. By holding RESET# LOW during system power up and setting to High after Vcc reaches operation voltage, inadvertent writes can be prevented (see Fig.12). Don't use this function except during power up. As RESET# is connected to Vcc internally, don't connect externally to any nodes when this function is not necessary.

Decouplling Capacitors

Ceramic capacitors (0.1 µF) must be added between V_{CC} and V_{SS} to each device to assure stable flash memory operation.

Absolute Maximum Stress Ratings

Storage Temperature .....-55 °C ~ 150 °C
Supply Voltage .....-0.5 V ~ 4.6 V
D.C. Voltage on Any Pin to Grand Potential .....-0.5 V ~ Vcc + 0.5 V

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

Operating Range

Ambient Temperature .....0 °C ~ 70 °C
Vcc .....2.7 V ~ 3.6 V

DC Operating Characteristics

Symbol	Parameter	Limit		unit	Test Condition
		Min.	Max.		
ICCR	Power Supply Current (Read)		10	mA	CS# = VIL SO,WP#,RESET# open SI = VIL / VIH f = 20MHz VCC = VCC max.
ICCW	Power Supply Current (Write)		25	mA	VCC = VCC max.
ISB1	Standby Vcc Current (TTL input)		3	mA	CS# = VIH SO,WP#,RESET# open SI = VIL / VIH VCC = VCC max.
ISB2	Standby Vcc Current (CMOS input)		20	µA	CS# = VCC–0.3V SO,WP#,RESET# open SI = VIL / VIH VCC = VCC max.
ILI	Input Leakage Current		10	µA	VIN = VSS ~ VCC, VCC = VCC max. WP#,RESET# is excluded
ILO	Output Leakage Current		10	µA	VIN = VSS ~ VCC, VCC = VCC max.
VIL	Input Low Voltage	–0.3	0.4	V	VCC = VCC max.
VIH	Input High Voltage	2.4	Vcc+0.3	V	VCC = VCC min.
VOL	Output Low Voltage		0.4 0.2	V V	IOL = 2.0 mA, VCC = VCC min. IOL = 100 µA, VCC = VCC min.
VOH	Output High Voltage	Vcc-0.2 Vcc-0.4		V V	IOH = –2.0 mA, VCC = VCC min. IOH = –100 µA, VCC = VCC min.

Power-up Timing

Symbol	Parameter	Minimum	Units
tPU_READ	Power-up to Read Operation	10	ms
tPU_WRITE	Power-up to Write Operation	10	ms
tPU_RST	From RESET# goes High to Command Entry	1	µs

Capacitance (Ta = 25 °C, f = 1 MHz)

Symbol	Description	Maximum*	Unit	Test Condition
CDQ	DQ Pin Capacitance	12	pF	VDQ = 0V
CIN	Input Capacitance	6	pF	VIN = 0V

Note: These parameters are periodically sampled and are not 100% tested.

AC Characteristics

Symbol	Parameter	Limit			unit
		Min.	Typ.	Max.	
fCLK	Clock Frequency			20	MHz
tCSS	CS# setup time	250			ns
tCSH	CS# hold time	250			ns
tCPH	CS# standby pulse width	250			ns
tCHZ	CS# to Hi-Z output			250	ns
tDS	Data Setup time	15			ns
tDH	Data hold time	15			ns
tCLH	SCK High pulse width	22			ns
tCLL	SCK Low pulse width	22			ns
tCLZ	SCK to Lo-Z output	0			ns
tV	SCK to output valid		10*[1]	20	ns
tHO	Output data hold time	0			ns
tSE	Sector Erase Cycle Time			25/700*[2]	ms
tBP	Byte Program Cycle time			25	µs
tRST	Write Reset Recovery Time			10	µs

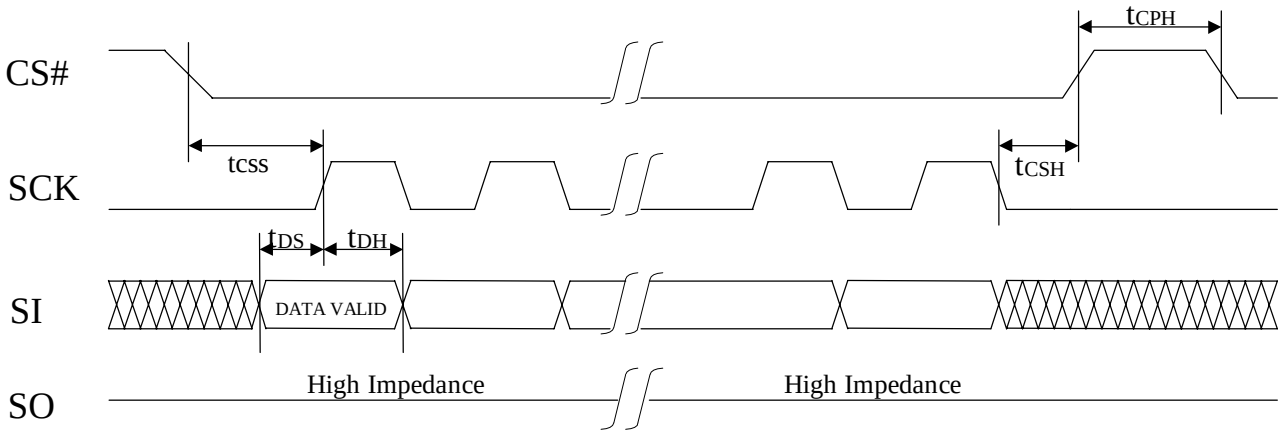
*1 : Vcc=3.0V, Room Temperature.
*2 : When Sector-Write Endurance Cycles is less than 10^4, tSE is 25ms.

AC Test Conditions

Input Pulse Level.....0V , 3.0V
Input Rise/Fall Time.....5 ns
Input/Output Timing Level 1/2Vcc
Input Load Levels.....30 pF

Timing waveforms

Figure 3: Serial Input Timing Diagram
(SPI mode 0)



(SPI mode 3)

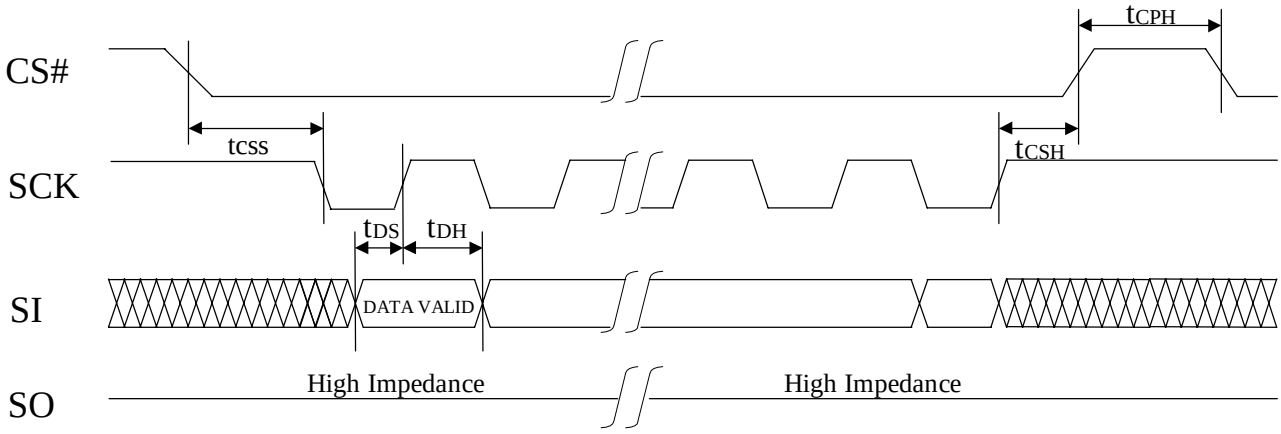
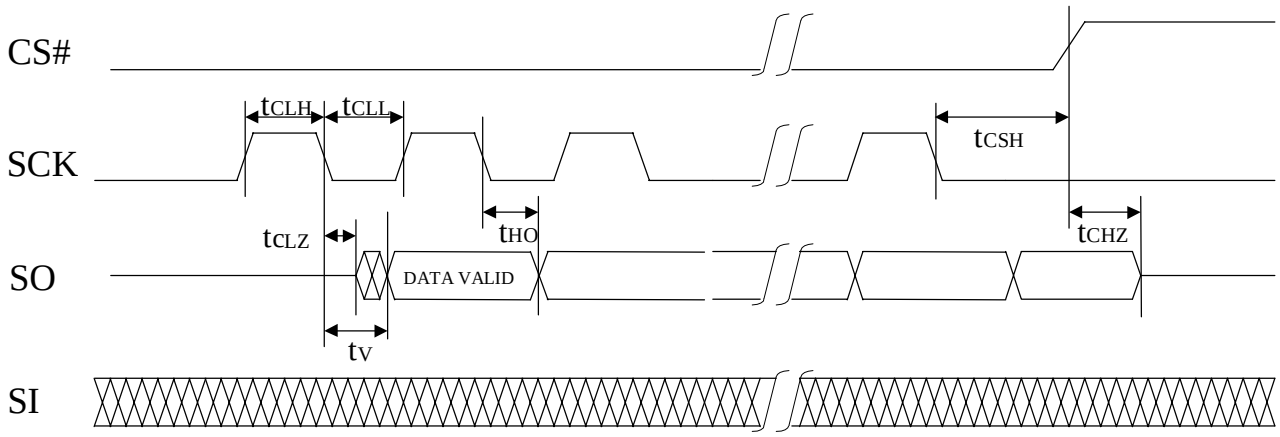
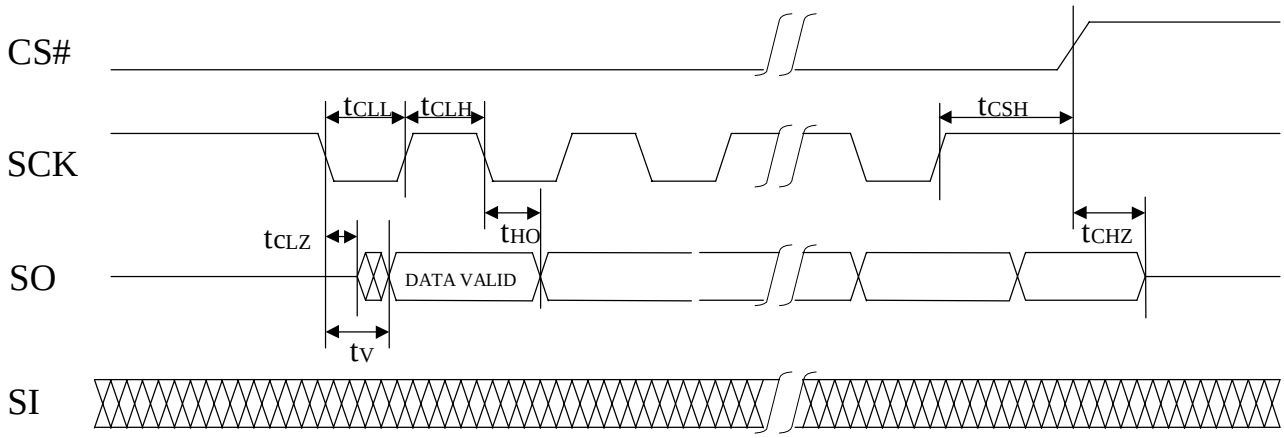


Figure 4: Serial Output Timing Diagram
(SPI mode 0)



(SPI mode 3)



(The following timing forms are described in SPI Mode 3)

Figure 5: Read Cycle Timing Diagram

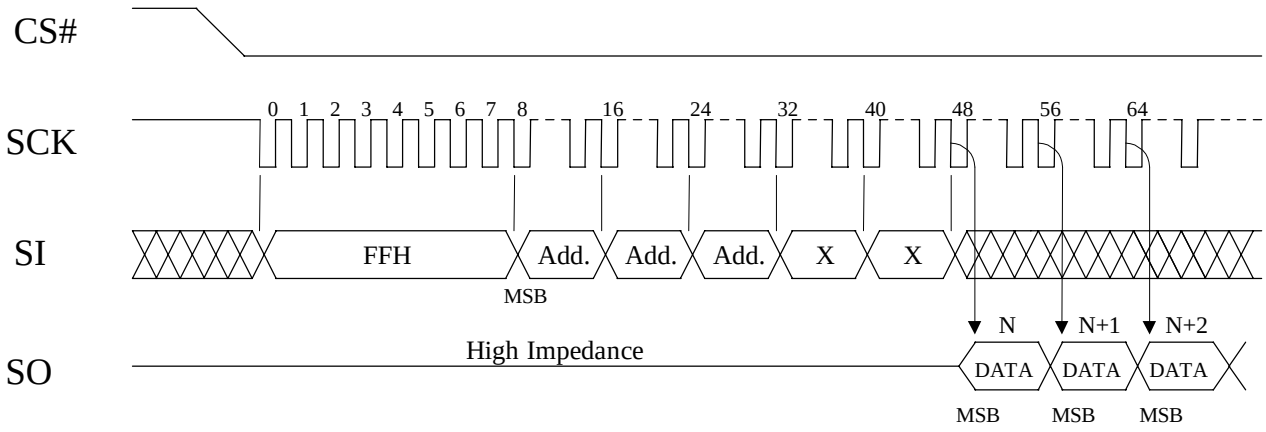


Figure 6: Status Register Read Timing Diagram

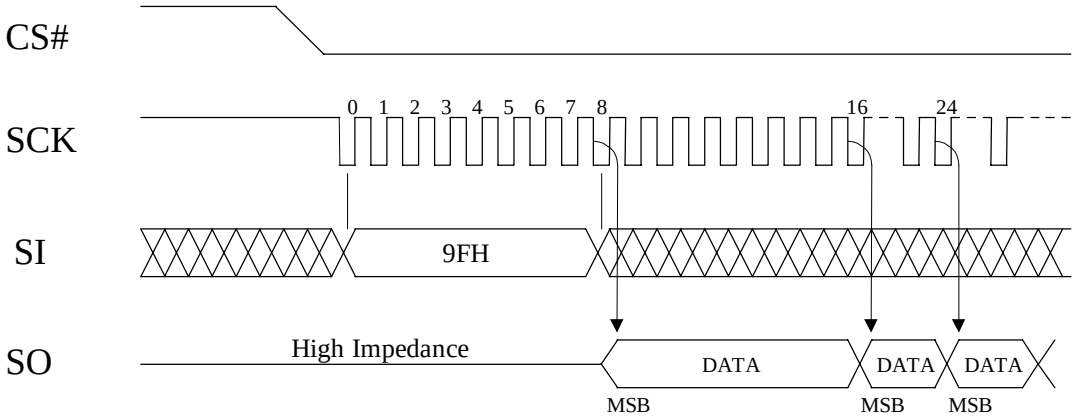


Figure 7: Sector_Erase Timing Diagram

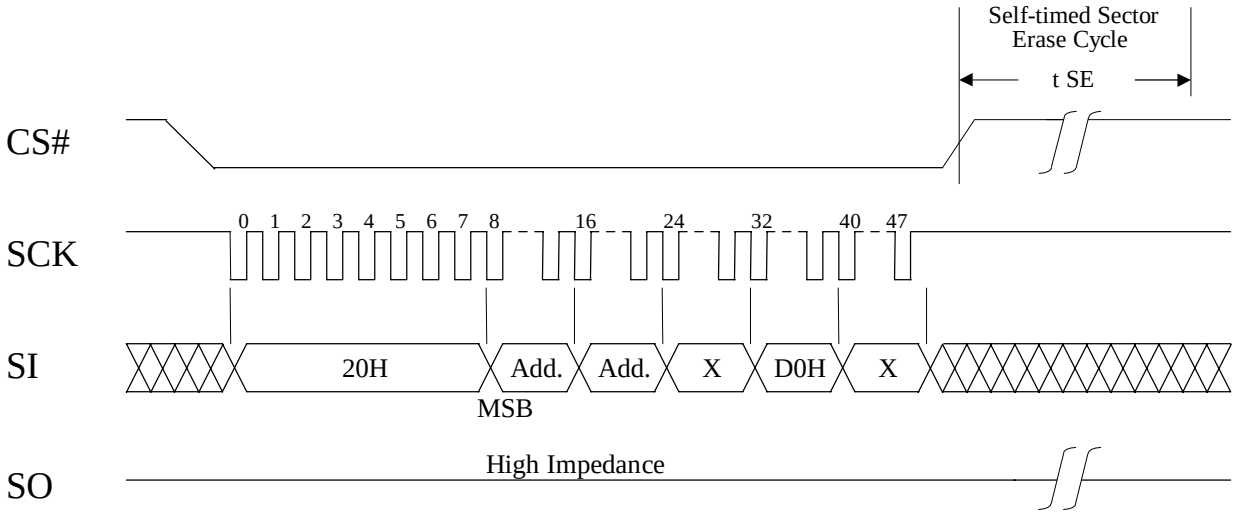


Figure 8: Byte_Program Timing Diagram

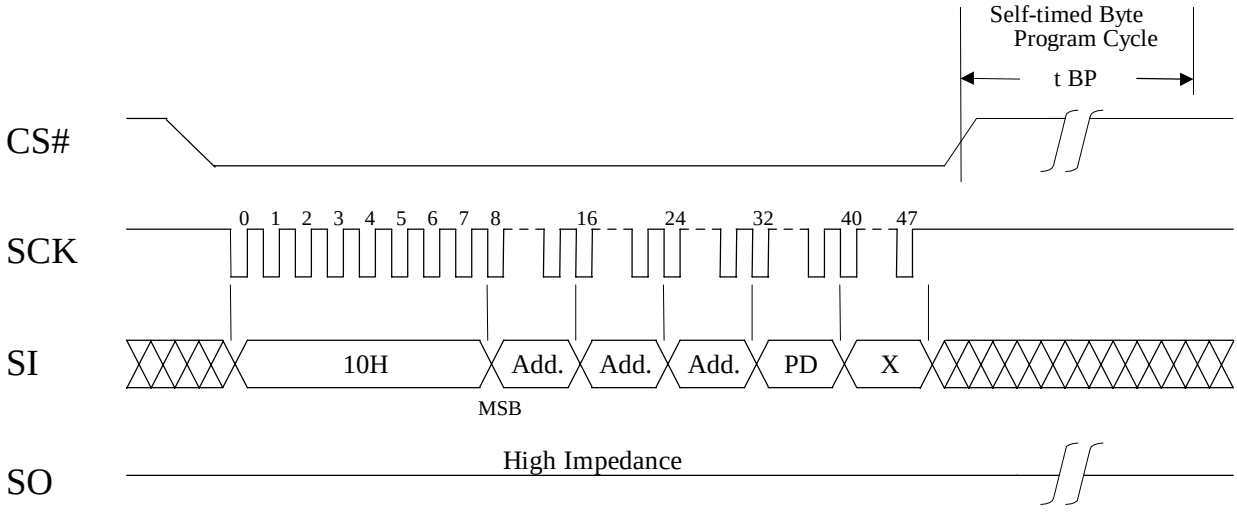


Figure 9: Read_ID Timing Diagram

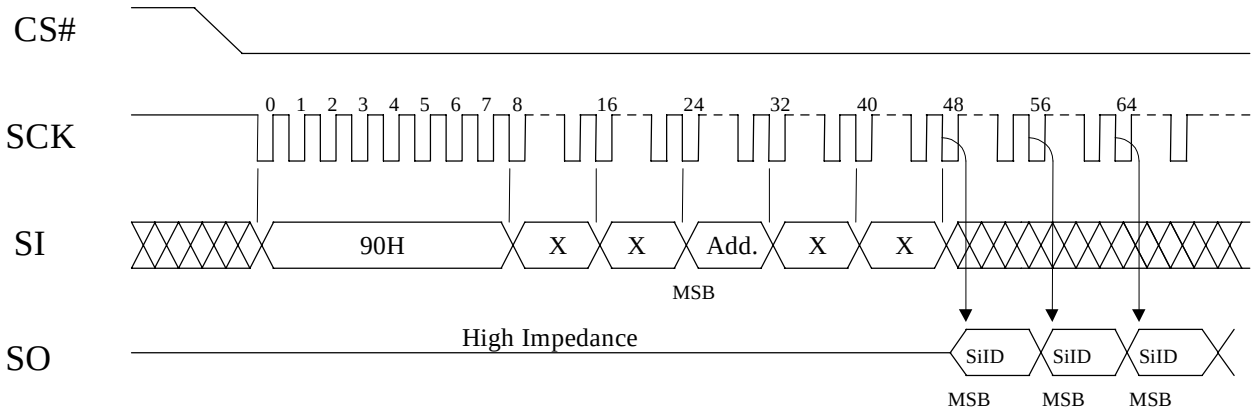


Figure 10: Reset Timing Diagram

Reset Command is effective when the device is only in Program or Erase sequence (in tBP,tSE or tBE period).

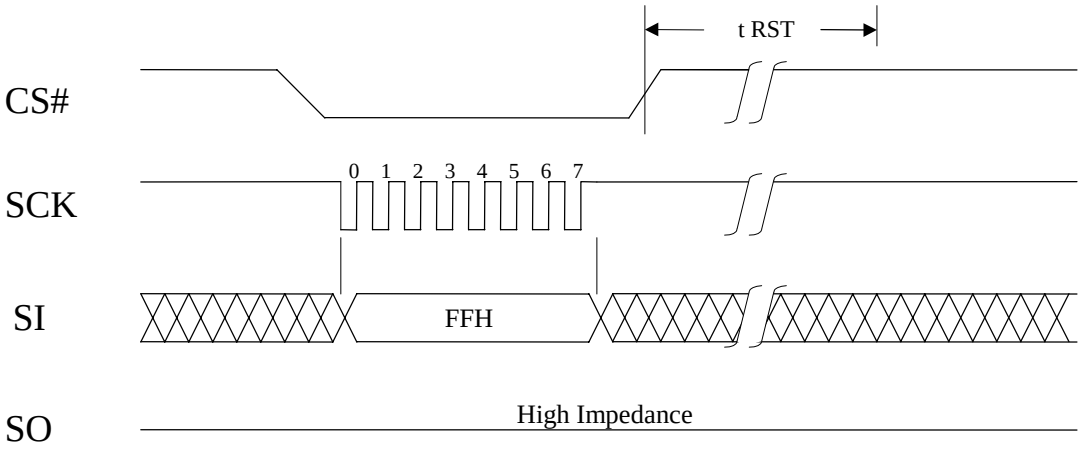


Figure 11: Command Entry Recover Timing from RESET# goes High