Ordering number : EN※4676

CMOS LSI

SANYO No. ※4676

LC78832M

16 Bits D/A Converter LSI with On-Chip Digital Filters

Preliminary

Overview

The LC78832M is a CMOS two-channel 16 bits D/A converter LSI that includes 2 × oversampling digital filters on chip.

Features

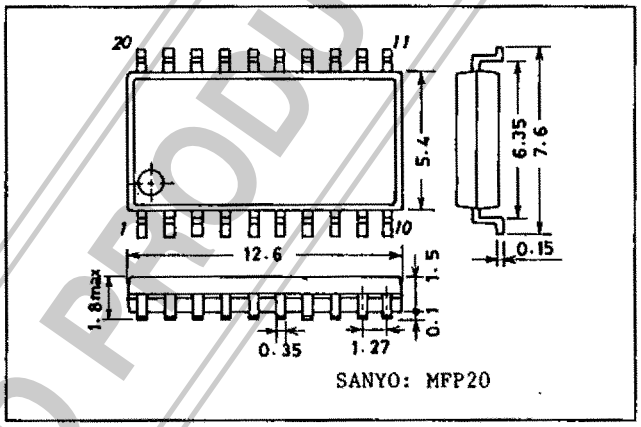
[Digital Filter Block]
- 2 × oversampling digital filters: FIR 43rd order
- De-emphasis filter: Fs = 44.1 kHz

[D/A Converter Block]
- Dynamic level shift conversion 16 bits D/A converters
- D/A converters for two channels on chip (common mode outputs)
- On-chip output op-amps
- System clock: 384 fs
- Single voltage power supply: 3.2 to 5.5 V
- Si gate CMOS process (low power dissipation)

Package Dimensions

unit: mm

3036B-MFP20



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		−0.3 to +7.0	V
Maximum input voltage	V_{IN} max		−0.3 to V_{DD} + 0.3	V
Maximum output voltage	V_{OUT} max		−0.3 to V_{DD} + 0.3	V
Operating temperature range	Topr		−30 to +75	°C
Storage temperature range	Tstg		−40 to +125	°C

Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		3.2	5.0	5.5	V
Reference voltage high level	Vref H		V_{DD} − 0.3		V_{DD}	V
Reference voltage low level	Vref L		0		0.3	V

DC Characteristics at Ta = −30 to +75°C, V_{DD} = 3.2 to 5.5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high level voltage 1	$V_{IH}1$	Input pins other than SYSCLK	2.2			V
Input low level voltage 1	$V_{IL}1$	Input pins other than SYSCLK			0.8	V
Input high level voltage 2	$V_{IH}2$	The SYSCLK pin	0.7 V_{DD}			V
Input low level voltage 2	$V_{IL}2$	The SYSCLK pin			0.3 V_{DD}	V

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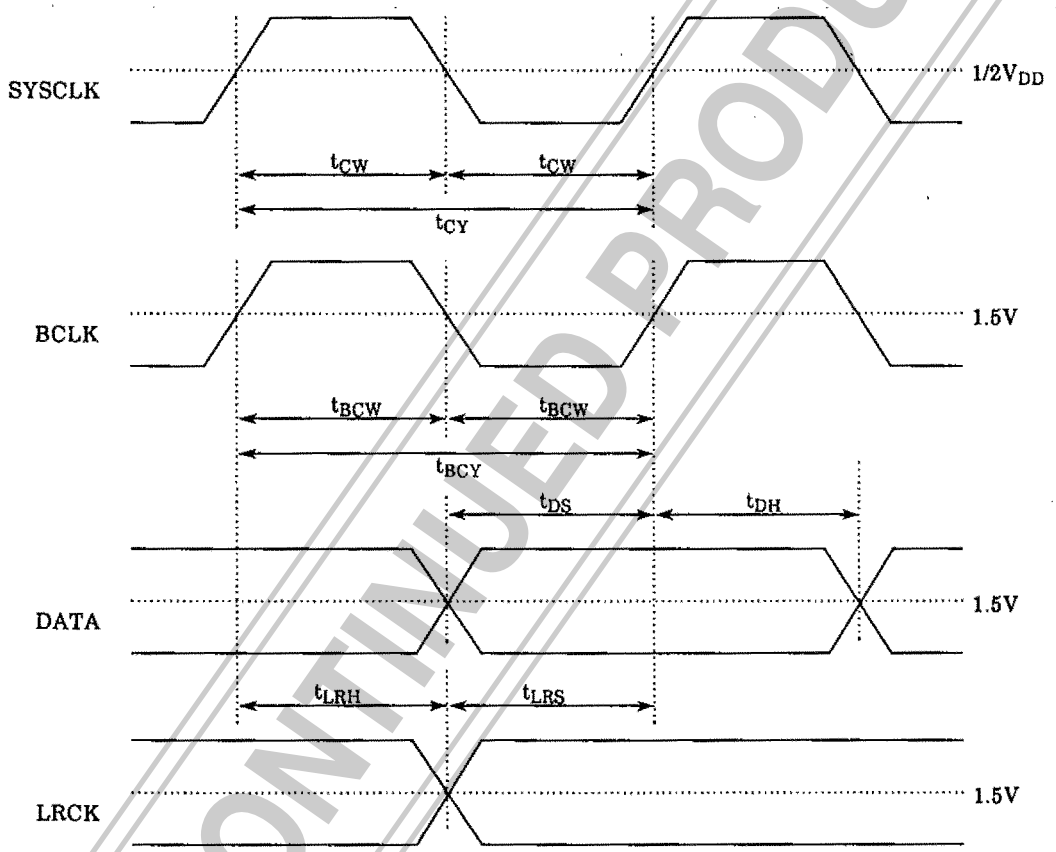
AC Characteristics at Ta = –30 to +75°C, V_{DD} = 3.2 to 5.5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Clock pulse width	t_{CW}		25			ns
Clock pulse period	t_{CY}		50		1000	ns
BCLK pulse width	t_{BCW}		60			ns
BCLK pulse period	t_{BCY}		120			ns
Data setup time	t_{DS}		40			ns
Data hold time	t_{DH}		40			ns
LRCK setup time	t_{LRS}		40			ns
LRCK hold time	t_{LRH}		40			ns

Input Waveforms



Electrical Characteristics (1)

at Ta = 25°C, DV_{DD} = AV_{DD} = Vref H = 5.0 V, DGND = AGND = Vref L = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
D/A converter resolution	RES			16		Bits
Total harmonic distortion	THD	At 1 kHz, 0 dB			0.08	%
Dynamic range	DR	At 1 kHz, –60 dB	90			dB
Cross talk	CT	At 1 kHz, 0 dB			–85	dB
Signal to noise ratio	S/N	JIS-A	96			dB
Full-scale output voltage	VFS			2.8		Vp-p
Power dissipation	Pd			100	150	mW
Output load resistance	R_L	Pins 1 and 20	5			kΩ

Note: Test circuit results apply to application circuits.

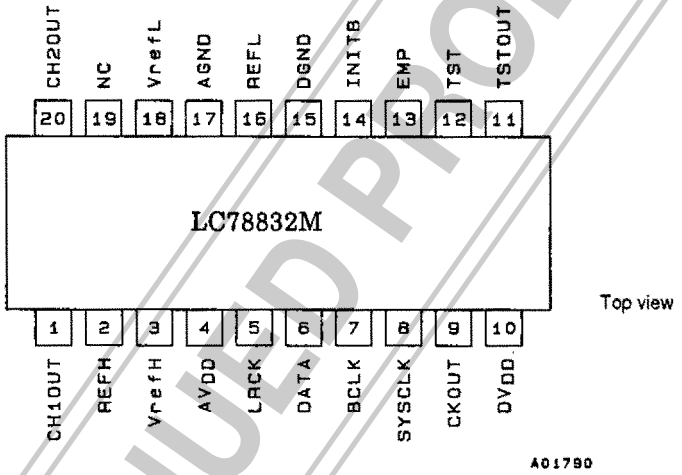
Electrical Characteristics (2)

at Ta = 25°C, DV_{DD} = AV_{DD} = Vref H = 3.2 V, DGND = AGND = Vref H = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
D/A converter resolution	RES			16		Bits
Total harmonic distortion	THD	At 1 kHz, 0 dB			0.1	%
Dynamic range	DR	At 1 kHz, –60 dB	90			dB
Cross talk	CT	At 1 kHz, 0 dB			–85	dB
Signal to noise ratio	S/N	JIS-A	96			dB
Full-scale output voltage	VFS			1.8		Vp-p
Power dissipation	Pd			30	45	mW
Output load resistance	R_L	Pins 1 and 20	30			kΩ

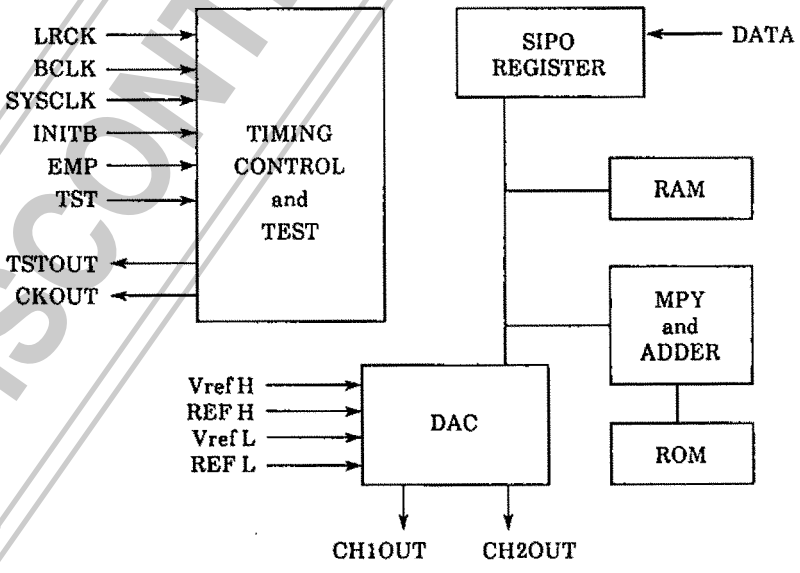
Note: Test circuit results apply to application circuits.

Pin Assignments



Top view

Block Diagram



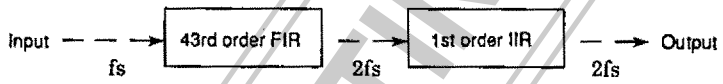
Pin Functions

Pin No.	Pin	Function
1	CH1OUT	Channel 1 analog output
2	REFH	Reference voltage high level Normally connected to AGND through a capacitor.
3	Vref H	Reference voltage high level input
4	AV_{DD}	Analog system power supply
5	LRCK	LR clock input The channel 1 signal is input when high, channel 2 when low.
6	DATA	Digital audio data input Data is input in a two's complement MSB first format.
7	BCLK	Bit clock input
8	SYSCLK	System clock input
9	CKOUT	System clock output
10	DV_{DD}	Digital system power supply
11	TSTOUT	Test output pin
12	TST	Test input pin
13	EMP	De-emphasis filter on/off switch The filter is on when high, off when low. The filter is designed for an Fs of 44.1 kHz.
14	INITB	Initialization signal input: The LSI is initialized when this pin is low.
15	DGND	Digital system ground
16	REFL	Reference voltage low Normally connected to AGND through a capacitor.
17	AGND	Analog system ground
18	Vref L	Reference voltage low input
19	NC	No connection
20	CH2OUT	Channel 2 analog output

Operating Description

1. Digital filters

The LC78832M performs the processing shown in the figure below.



- Oversampling

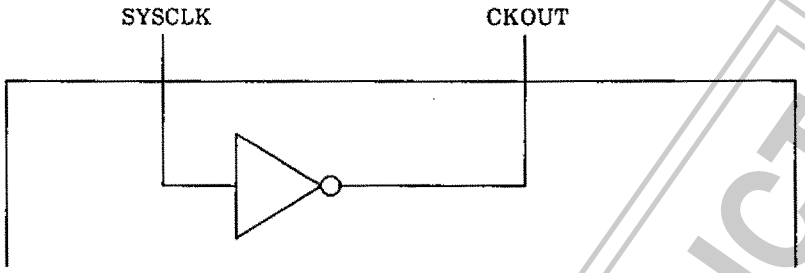
Oversampling is performed by the 2× interpolation filter formed by the 43rd order FIR.
The filter characteristics are shown in the logical values figures.

- De-emphasis

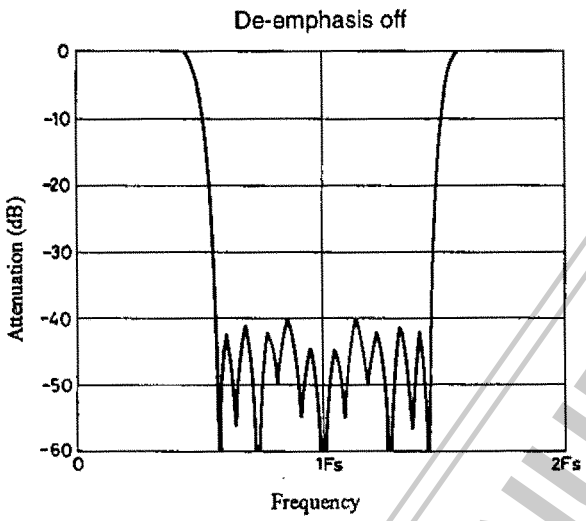
The first-order IIR filter performs de-emphasis.
The filter coefficients correspond to an fs of 44.1 kHz.
The filter characteristics are shown in the logical values figures.
The EMP pin is used to turn the de-emphasis filter on and off.
When the EMP is high, the de-emphasis filter will be on; when the EMP is low, the de-emphasis filter will be off.

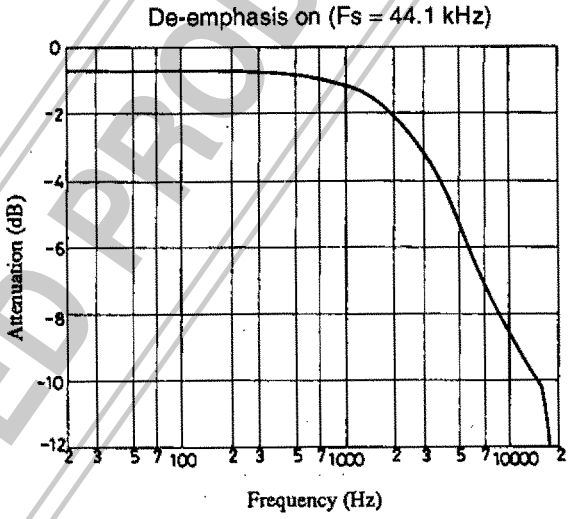
2. System Clock

The LC78832M uses a 384 fs system clock. A 384 fs clock must be input to the SYSCLK pin. Note that SYSCLK and CKOUT have the relationship shown in the figure.



Filter Characteristics (Logical Values)

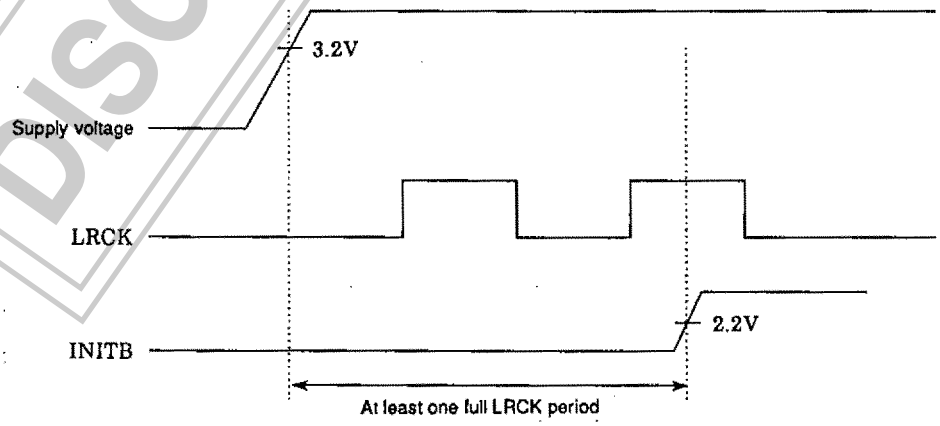




3. Initialization

The LC78832M must be initialized after power is applied. Initialization is performed by holding the INITB pin low. This low period must be at least one full LRCK period long, and must start after the power supply voltage has stabilized and after SYSCLK, BCLK, and LRCK have been applied, as shown in the figure.

While INITB is low, the output of the digital filters will be zero in all 16 bits, and the D/A converter outputs (CH1OUT and CH2OUT) will be analog zero (a potential essentially equal to (REFH + REFL)/2).



4. Digital Audio Data Input

The digital audio data is a 16-bit serial signal and is in an MSB first two's complement format. The 16-bit serial data is input from the DATA pin to an internal register on the rising edge of BCLK, and is read in on the rising and falling edges of LRCK.

Digital audio data input timing

5. D/A Converter

The LC78832M provides independent 16-bit D/A converters with built-in output op-amps for channel 1 and channel 2. These D/A converters use a dynamic level shifting conversion scheme that combines a resistor string D/A converter (R-string D/A converter), a pulse-width modulation D/A converter (PWM D/A converter), and a level shift D/A converter.

- R-string D/A converter

The R-string D/A converter is a 9-bit D/A converter circuit that consists of 512 (i.e., 2^9) individual resistors connected in series. These resistors divide the voltage applied at the ends of the string into 512 equal divisions. A switching circuit outputs two adjacent potentials from these divided potentials according to the upper 9 bits of the data. These two potentials are output to the PWM D/A converter. Here the relationship

$$V2 - V1 \fallingdotseq (VH - VL)/512$$

will hold.

- PWM D/A converter

The PWM D/A converter is a three-bit D/A converter circuit that uses a PWM (pulse width modulation) circuit to divide the span of the two potentials V1 and V2 output from the R-string D/A converter by eight. This D/A converter outputs either V1 or V2 depending on the middle 3 bits of the data.

- Level shift D/A converter

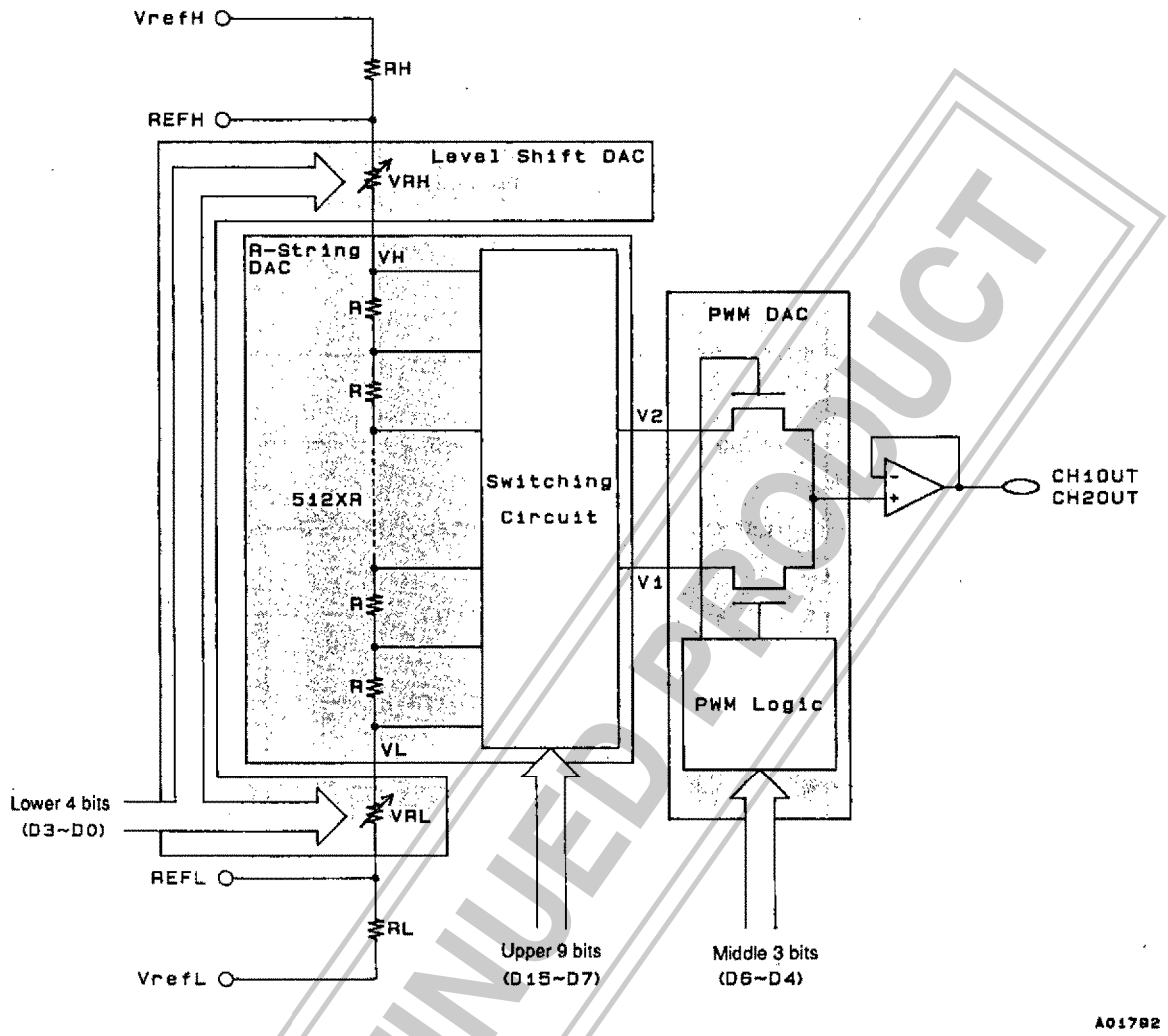
The level shift D/A converter is a four-bit D/A converter formed by connecting the variable resistors VRH and VRL in series at the ends of the R-string DAC. The lower four bits of data are used to adjust these variable resistors as follows:

— The value (VRH + VRL) is constant for all values of the data.

— The values of VRH and VRL are varied over the range 0 to 15R/128 (where R is the value of the unit resistors in the R-string D/A converter) in steps of R/128 Ω.

This results in the V1 and V2 outputs of the R-string D/A converter varying in steps of $\Delta V/128$ over the range 0 to $15 \times \Delta V/128$ (where $\Delta V = (VH - VL)/512$) according to the value of the low-order four bits of the data.

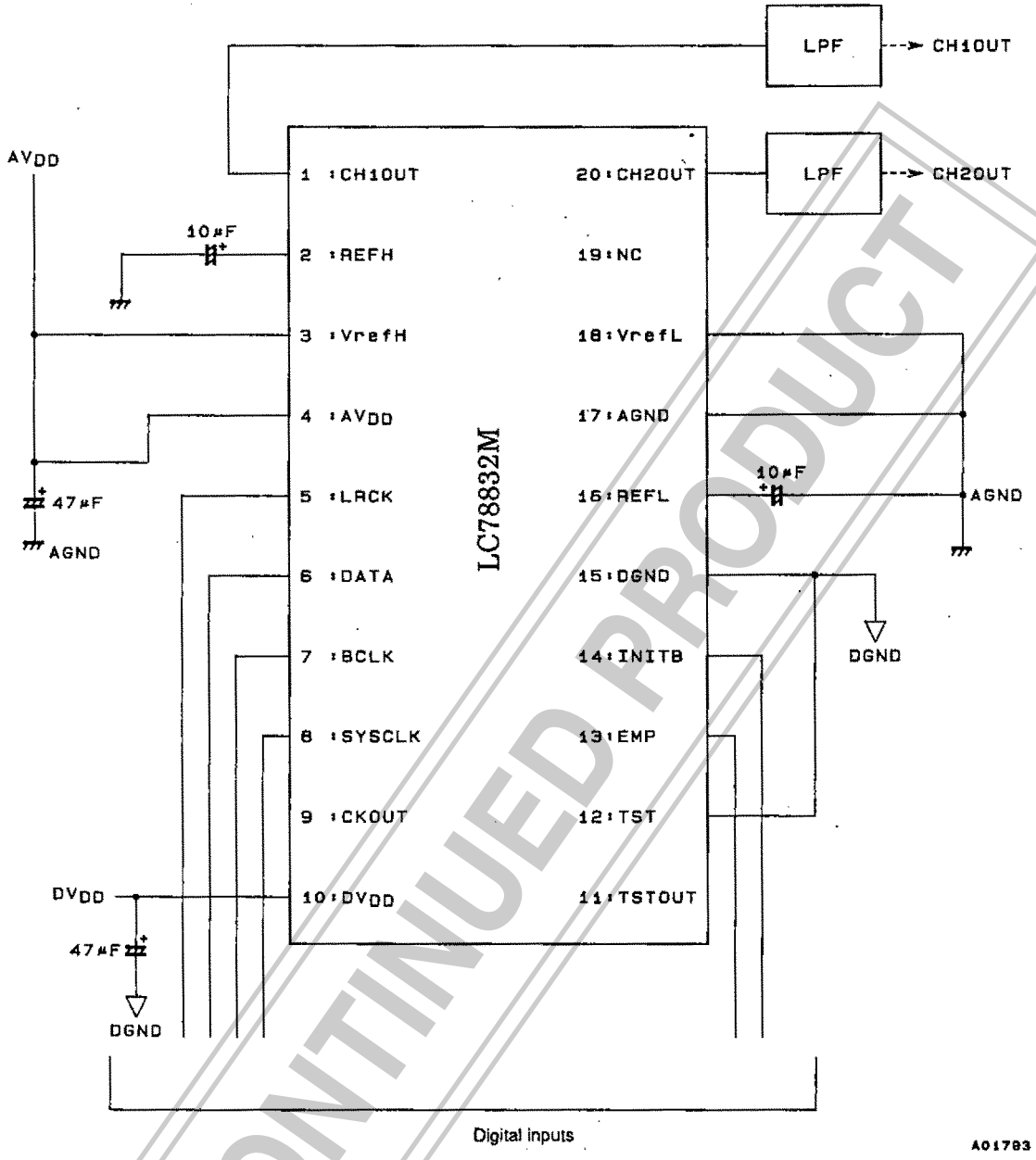
LC78832M D/A Conversion Scheme



Vref H, Vref L, REFH, and REFL

Normally the Vref H and Vref L pins, which supply the reference voltage to the resistor string, are connected to AV_{DD} and AGND respectively. Also, 10 µF capacitors are connected between REFH and AGND, and between REFL and AGND.

Application Circuit Example



Note: 1. Use a low-impedance high-stability power supply (a commercial three terminal regulator or equivalent) for V_{DD} and Vref H.
2. Since the circuit may latch up if there is a discrepancy in the rise time of the power signals applied to pin 4 (AV_{DD}) and pin 10 (DV_{DD}), design application circuits so that pins 4 and 10 come up at the same time.
3. Connect bypass capacitors between AV_{DD} and AGND and between DV_{DD} and DGND. To reduce noise, these capacitors should be placed as close as possible to the LSI.