Data Sheet
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L9520 POTS/DSL Enhanced Line Interface Low-Power SLIC and Ring Relay with Integrated Test

Introduction

The Agere Systems Inc. L9520 is a combination full-feature, ultralow-power SLIC, solid-state ringing access relay, and line test matrix. It forms an ideal chip set with the Agere T8531/2 codec for POTS and DSL line cards, providing *Telcordia*™ GR844 test capability, tone plant, and fully programmable ac parameters. The chip set will meet TR57 POTS requirements including the effects of the DSL coupling and POTS filter.

Applications

- POTS plus DSL
- Digital loop carrier (DLC)
- Central office (CO)

Features Overview

- Integrated SLIC, solid-state ring relay, and line test
- Ideal for POTS and DSL applications
- TR57 compliant POTS interface
- 5 V and battery operation
- Optional automatic battery switch
- 15 operational and test modes
- Two performance grades based on TR57 58 dB or ETSI/ITU-T 46 dB longitudinal balance requirements
- Minimal external components required at all interfaces
- Ultralow power dissipation
- Software/hardware adjustable dc parameters and supervision thresholds
- Ground start/ground key compatible
- Low impulse noise associated with ring relay
- Current-limited switches/thermal protection
- When paired with T8531/2 codec provides hardware and software for GR844 testing
- 68-pin MLCC package

Description Overview

The L9520 electronic line interface and line access circuit provides all the functions that are necessary to interface a codec to the tip and ring of a subscriber loop, integrating the battery feed and ringing access relay and the line test access in one low-power, low-cost package.

The L9520 provides an ideal solution for POTS plus DSL applications when used with the Agere Systems T8531/2 codec. Together, this chip set provides fully programmable ac parameters that are consistent with TR57 requirements, undergirded test that is consistent with GR844 requirements, and tone plant that includes DTMF generation, reception caller ID, and call progress tones.

The L9520 is optimized to interface to the Agere Systems T8531/2 codec. It will also cleanly interface to the Agere T8534/6 series codec. This device will not interface to any commercially available codec other than the Agere T8531/2 or T8534/6.

The L9520 requires a 5 V and battery supply to operate. Included is an automatic battery switch. The battery feed offers forward and reverse battery, on-hook transmission, ground start, ground key, and meter pulse operational modes. It also has a low-power scan and a disconnect mode.

In all operating states, this IC is designed for minimal power dissipation. This device is designed to minimize the number of external components required at all interfaces.

The dc template, current limit, and overhead voltage and loop supervision threshold are programmable via an applied voltage source. The voltage source may be an external programmable voltage source or derived from the V_{REF} SLIC output.

The integrated solid-state switch offers power ringing access. Impulse noise is minimized, therefore eliminating the need for external zero-cross switching circuitry.

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Features

- SLIC, solid-state ring relay, and line test access, integrated into a single package
- 5 V and battery operation
- User-defined power control options:
  - — Automatic battery switch
  - — Power control resistor
  - — Package thermal capabilities
- Minimal external components required
- Operating states:
  - — Forward active
  - — Reverse active (controlled rate of reversal)
  - — Scan
  - — Ground start (tip open)
  - — All-off or disconnect
  - — Ring
  - — Line test modes (dc/ac line voltage/current)
- Ultralow power:
  - — Scan state, 15 mW
  - — Active state, on-hook, 83 mW
  - — Ring state, on-hook, 155 mW
  - — Disconnect state, 7 mW
- Adjustable overhead voltage:
  - — Default overhead adequate for 3.14 dB into 900 Ω overload
  - — Controlled rate of overhead adjustment
- Latched parallel input data interface with reset
- Interrupt (unlatched) based loop status monitor
- Adjustable current limiter:
  - — 10 mA to 70 mA programming range
- Adjustable loop closure detector with hysteresis:
  - — 4 mA detect, 2.5 mA no detect minimum, upper limit of 15 mA detect
  - — Hysteresis, typical 20% of programmed on-hook to off-hook threshold
- Ring trip detector:
  - — Single-pole filtering
- Thermal shutdown protection with hysteresis
- Line break switch will foldover into a low-current state under high-voltage fault conditions
- Battery out-of-range monitor circuit:
  - — All-off upon loss of battery (low battery condition)
  - — All-off upon high battery (fault condition)
- Longitudinal balance:
  - — TR57 balance (L9520G)
  - — ETSI/ITU-T balance (L9520K)
- Ground start:
  - — Tip open state
  - — Ring ground detector
- Ground key:
  - — Tip/ring ground detector
- Line test:
  - — Line test modes (ac or dc), including the following:
    - ❏ Voltage tip to ground
    - ❏ Voltage ring to ground
    - ❏ Voltage tip to ring
    - ❏ Current tip to ring
    - ❏ Current tip to ground
    - ❏ Current ring to ground
  - — Generate test tones and control script via T8532 codec
  - — Direct coupling to T8531 codec
- Integrated 2 form C ring relay:
  - — Low impulse noise
  - — Current-limited switches
  - — Break-before-make and make-before-break switching
- Meets ITU-T K20, ITU-T K21, and *Telcordia* GR1089 requirements with external protection device
- 68-pin, surface-mount MLCC

Description

The L9520 electronic line interface and line access circuit provides all the functions that are necessary to interface a codec to the tip and ring of a subscriber loop, integrating the battery feed and ringing access relay in one low-power, low-cost package. The physical construction of the device is two chips. The first chip is manufactured in Agere's 90 V complementary bipolar integrated circuit (CBIC-S) technology. This chip contains the following SLIC functionality:

- ac transmission path
- dc feedback and functions
- Active dc current limit
- Active mode loop supervision
- Thermal shutdown

The second chip is manufactured with Agere's dielectrically isolated 320 V bipolar CMOS diffused metal oxide semiconductor (BCDMOS III) technology. This chip contains the following:

- Ring access relay
- Scan clamp circuitry
- Logic control
- Ring trip
- Test
- Thermal shutdown
- Battery monitor circuit

Description (continued)

The L9520 requires a 5 V power supply and a battery supply to operate. No –5 V supply is required. A battery switch is included that will automatically (based on subscriber loop length) apply either the primary higher-voltage battery or an optional lower-voltage auxiliary battery. Use of this feature will minimize off-hook power dissipation.

The switch point is a function of the user-programmed dc current limit and the magnitude of the auxiliary battery. Switching from the high-voltage battery to the low-voltage battery is quiet and does not interrupt the dc loop current, therefore preventing any impulse noise generation at the switch point. Design equations for the switch point and a graph showing loop/battery current versus loop resistance are given in the dc Characteristics section of this data sheet.

If the user does not want to provide an auxiliary battery, the design of the L9520 battery switch allows use of a power control resistor at the auxiliary battery input. This scheme will not reduce short-loop, off-hook power dissipation, but it will control power dissipation on the SLIC by sharing power among the SLIC, power resistor, and dc loop. However, in most cases, without the auxiliary battery, the power dissipation capabilities of the 68-pin MLCC package are enough that the power control resistor will not be needed. Design equations for power control options are given in the dc Characteristics section of this data sheet.

The L9520 has two active transmission ready states, forward active and reverse active. Both on-hook and off-hook transmission are provided during the forward and reverse battery modes. Battery reversal is quiet and does not break the ac path. Rate of battery reversal may be ramped to control switching time via optional external capacitors. Equations relating rate of battery reversal to these optional external capacitors are given in the dc Characteristics, Power Control section of this data sheet.

A low-power scan mode is available to reduce idle mode on-hook power. This mode is realized by using a scan clamp circuit. The following occurs in low-power scan mode:

- The scan clamp circuitry is active.
- Loop closure is active.
- All ac transmission, dc feed, and other supervision circuits, including ring trip, are shut down.
- Test is powered down.
- Thermal shutdown is active.
- Low battery sense shutdown is on.
- On-hook transmission is disabled.

When the scan clamp circuitry is on, overhead voltage is fixed and not controlled by OVH. When the scan clamp is on, current limit is not controlled by V_{PROG}; rather, it is set by the internal capabilities of the scan clamp circuit. See the dc Loop Current Limit and Overhead Voltage sections of this data sheet for more details.

A forward disconnect mode, where all circuits are turned off and power is denied to the loop, is also provided. During this mode, the NSTAT supervision output will read on-hook.

In the ring mode, the line break switches are opened and the power ring access switches are closed. In this mode, the ring trip detector in the SLIC is active and all other detectors and the tip/ring drive amplifiers are turned off to conserve power.

Make-before-break or break-before-make switching is achievable during ring cadence or ring trip. Toggling directly into or directly out of the ring mode table will give make-before-break switching. To achieve break-before-make switching, go to an intermediate all-off state (use forward disconnect state) before entering the ring mode or before leaving the ring mode. See the Switching Behavior section of this data sheet for more details on switching behavior.

Voltage transients or impulse noise associated with ring cadence or ring trip are minimized or eliminated with the L9520, therefore possibly eliminating the need for external zero-cross switching circuitry.

A tip open switch configuration is also available for ground start applications. A common-mode current detector is included for ground start and ground key applications.

Both the ring trip and loop closure supervision functions are included. Loop closure threshold is set by applying a voltage source to the LCTH input. The voltage source may be an external voltage source or derived from the SLIC V_{REF} output. A programmable external voltage source may be used to provide software control of the loop closure threshold. Design equations for the loop closure threshold are given in the Supervision section of this data sheet. Hysteresis is included.

The ring trip detector requires only a single-pole filter at the input. This will minimize the required number of external components. To help minimize device power dissipation, the ring trip detector is active only during the power ring mode.

Description (continued)

Ring trip and loop supervision status outputs appear in a common output pin, NSTAT. NSTAT is an unlatched supervision output; therefore, an interrupt-based control scheme may be used.

The dc current limit is set in the active modes via an applied voltage source. The voltage source may be an external voltage source. The voltage may be derived via a resistor divider network from the V_{REF} SLIC output. A programmable external voltage source may be used to provide software control of the loop closure threshold. Programming range is 10 mA to 70 mA. Design equations for this feature are given in the dc Characteristics section of this data sheet.

Overhead is programmable in the active modes via an applied voltage source. The voltage source may be an external voltage source or derived via a resistor divider network from the V_{REF} SLIC output.

A programmable external voltage source may be used to provide software control of the overhead voltage. A potential application of this feature is to increase overhead during test modes requiring higher voltages and reduce overhead during periods of nontest. The rate of change of the overhead voltage may be controlled by use of a single external capacitor at the C_{F1} node. If the rate of change is uncontrolled, there may be audible noise associated with this transition. Design equations for this feature are given in the dc Characteristics section of this data sheet.

If the overhead is not programmed via a resistor, the device develops a default overhead suitable for a 3.14 dBm overload into 900 Ω. For the default overhead, OVH is connected to ground.

The L9520 provides line test capability. In the test mode, a voltage proportional to the ac or dc tip-to-ground, ring-to-ground, tip-to-ring voltage or current may be presented at the SLIC TESTLEV output.

An ac test tone may also be applied to either a test input (TESTSIG–) or through the TESTSIG+ input. By varying the frequency of the applied test tone, parameters such as line capacitance may be measured.

This test feature may be conveniently utilized with the T8531/2 codec. This codec provides necessary test tones and provides control and data interpretation to run a test script consistent with GR844 requirements.

The TESTSIG inputs should be externally connected to the device's V_{REF} if they are not used.

Test level outputs at TESTLEV are referenced to the internally generated reference voltage V_{REF}. This reference voltage may also be output at TESTLEV so the users can compensate test results at TESTLEV for the internal reference.

Note that during nontest modes, TESTLEV is high impedance to conserve power. Inputs TESTSIG are turned off during any nontest mode and during the V_{REF} test mode.

The various test modes are achieved through a series of integrated analog switches that can reconfigure the SLIC to provide normal SLIC operation or the appropriate test function.

Test modes are achieved through the device state table. When entering a test mode, the state of the SLIC is unchanged; therefore, testing can be done with the SLIC in forward and reverse battery active modes. Additionally, via the line break switches associated with the ring relay, use of a tip-open or ring-open state is used to make single-ended voltage and current measurements.

Data control is via a parallel latched data control scheme. Data latches are edge-level sensitive. Data is latched in when the LATCH control input goes low. While LATCH is low, the user cannot change the data control inputs. The data control inputs may only be changed when LATCH is high.

Incorporation of data latches allows for data control information and loop supervision information to be passed to and from the SLIC via data buses rather than on a per-line basis, therefore minimizing routing complexity and board routing area.

A device RESET pin is included. When this pin is low, the logic inputs are overridden and the device will be reset into SLIC forward disconnect state and the switch into the all-off state. NSTAT is forced to the on-hook condition when RESET is low.

The overall device protection is achieved through a combination of an external secondary protector along with an integrated thermal shutdown feature, a battery voltage window comparator, the break switch foldback characteristic, and the dc/dynamic current-limit response of the break and tip return switches.

For protection against long duration fault conditions, such as power cross and tip/ring shorts, a thermal shutdown mechanism is integrated into the device. Upon reaching the thermal shutdown temperature, the device will enter an all-off mode. Upon cooling, the device will re-enter the state it was in prior to thermal shutdown. Hysteresis is built in to prevent oscillation. During this mode, the NSTAT supervision output overrides the actual loop status and forces an off-hook.

Description (continued)

The line break switches and tip return switch are current-limited switches. The current-limit mechanism limits current through the switch to the specified dc current limit under low frequency or dc faults (power cross and/or tip/ring to ground short) and limits the current to the specified dynamic current-limit response under transient faults, such as lightning.

A foldover characteristic is incorporated into the line break switches within their I-V curve. Under voltage conditions higher than the normal operating range, such as may be seen under an extreme lightning or power cross fault condition, the line break switch will foldover into a low-current state. This feature allows for more relaxed specifications on the ring side protector, therefore allowing for higher-voltage ringing signals. (Tip side protector is limited by the requirements on the tip return switch.) This feature is part of the overall device protection scheme.

This device uses a window comparator to force an all-off condition if the battery drops below, or rises above, a specified threshold.

Upon loss of V_{BAT1}, the L9520 will automatically enter an all-off mode. The device will enter this mode if the magnitude of the battery drops below a nominal 15 V and will remain in this mode until the magnitude of the battery rises above a typical 20 V. During this mode, the NSTAT supervision output will override the actual hook status and force an off-hook or logic low.

When the device is in the scan mode, because of the design of the scan clamp circuit, common-mode current can be forced into or out of the battery supply. Because of this, and depending upon power supply design, the magnitude of the battery may rise above the maximum operating condition during extended longitudinal currents or during a power cross fault condition. To prevent excess current from being forced into or out of the battery, if the magnitude of the battery rises typically above 75 V to 80 V, the device will enter an all-off state. The device will remain in the all-off state until the magnitude of the battery drops into the normal operating range. During this mode, the NSTAT supervision output will override the actual hook status and force an off-hook or logic low.

See the Protection section of this data sheet for more details on device protection. Contact your Agere account representative for a recommended secondary protection device.

Two performance grades based on longitudinal balance are available. The higher-grade longitudinal balance is consistent *Telcordia* TR57 requirements. The lower-grade, with European ETSI and *Telcordia* GR-909 requirements.

Transmit and receive gains have been chosen to minimize the number of external components required in the SLIC-codec ac interface. The L9520 uses a voltage feed, current sense architecture; therefore, the transmit gain is a transimpedance. The L9520 transimpedance is set via a single external resistor, and this device is designed for optimal performance with a transimpedance set at 300 V/A. The L9520 offers a single-ended to differential receive gain of 2.

A receive gain of 2 is appropriate when choosing an Agere System third-generation type codec. Third-generation codecs will synthesize termination impedance, set hybrid balance, and set overall gains. To accomplish these functions, third-generation codecs typically have both analog and digital gain filters. For optimal signal-to-noise performance, it is best to operate the codec at a higher-gain level. If the SLIC then provides a high gain, the SLIC output may be saturated, causing clipping distortion of the signal at tip and ring. To avoid this situation with a higher-gain SLIC, external resistor dividers are used. These external components are not necessary with the lower gain offered by the L9520.

A higher receive gain is needed when choosing a first-generation type codec where termination impedance, hybrid balance, and overall gains are set by external analog filters. The higher gain is typically required for interface to a competitive third-generation type codec requiring an inherent resistive termination. Since a higher-gain option is not available with this part, the device may only be used with the Agere T8531/2 or T8534/6 codecs.

This device is packaged in a 68-pin MLCC surface-mount package.

Architecture

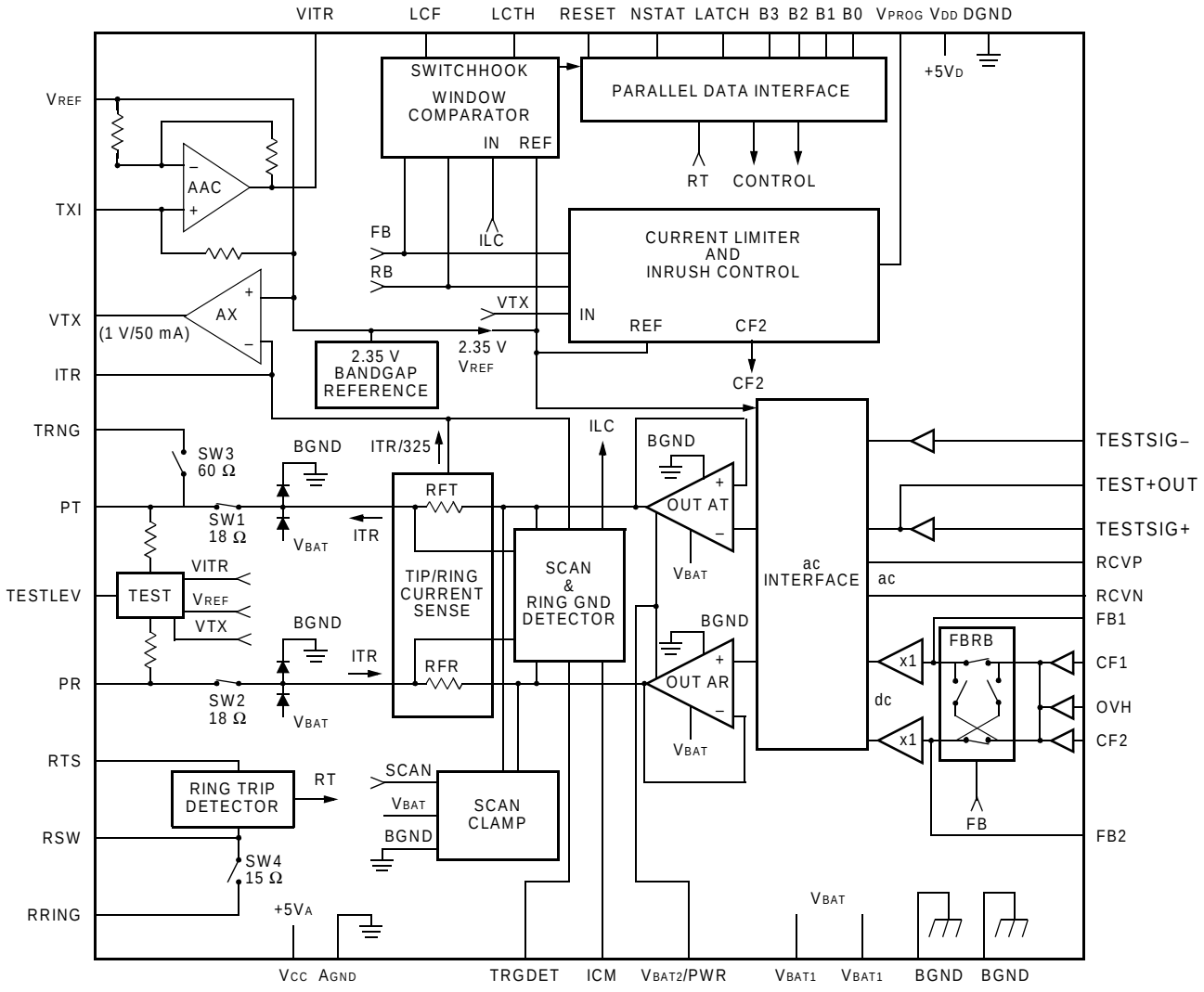

Figure 1. Architecture Diagram

Architecture (continued)

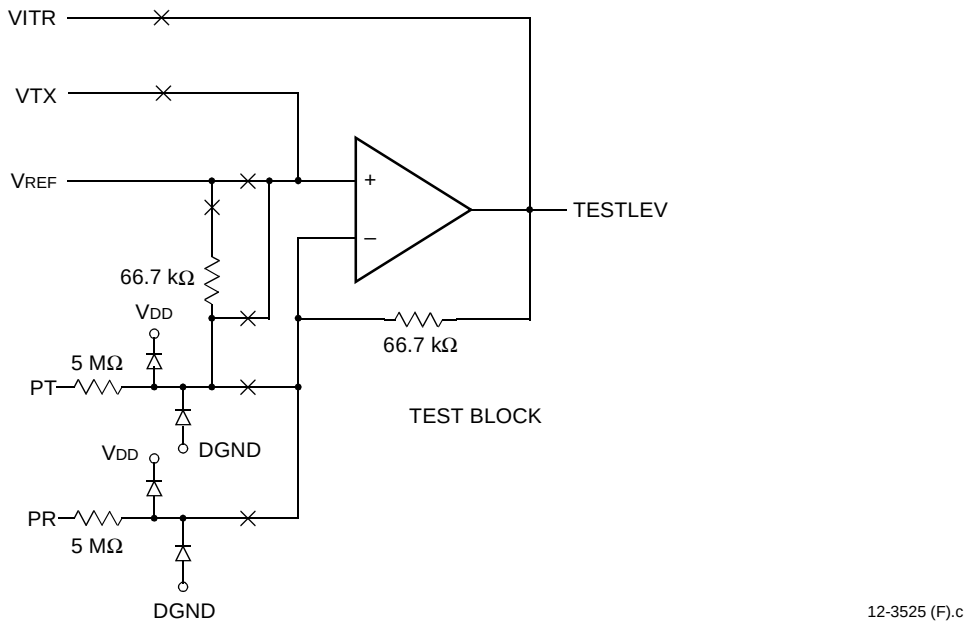

Figure 2. Test Switch Configuration

Pin Information

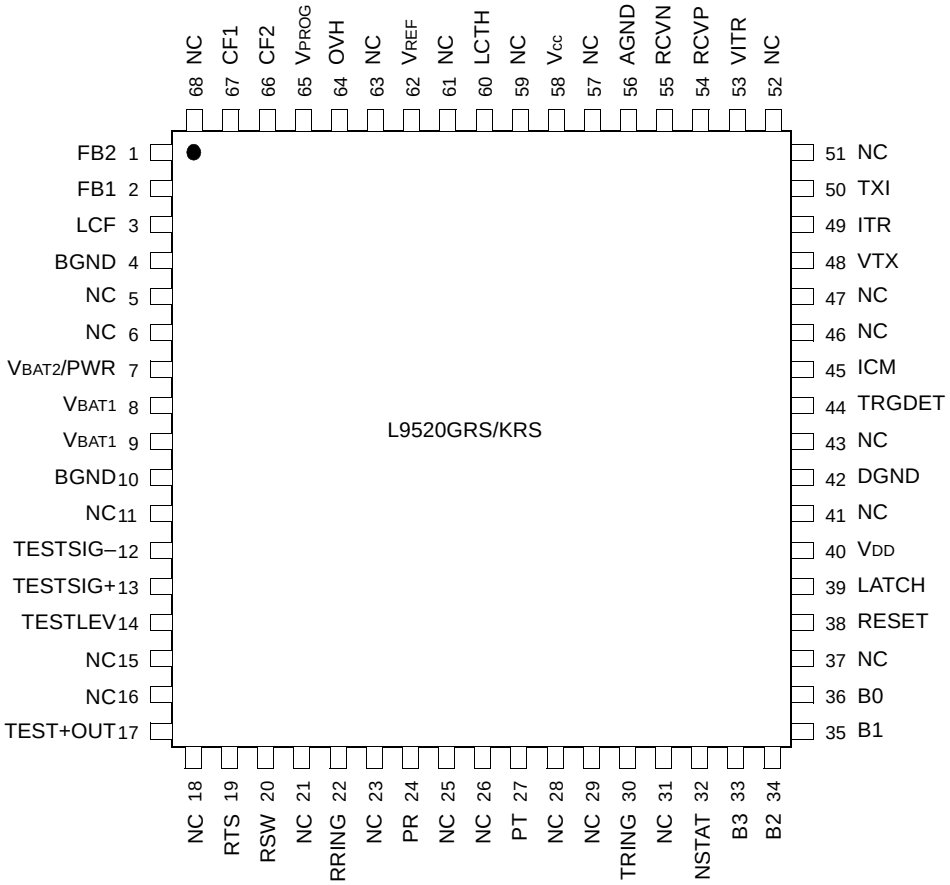

Figure 3. 68-Pin MLCC

Pin Information (continued)

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	FB2	—	**Polarity Reversal Slowdown Capacitor.** Connect a capacitor from this node to ground to control the rate of battery reversal. If controlled battery reversal is not desired, leave this pin open.
2	FB1	—	**Polarity Reversal Slowdown Capacitor.** Connect a capacitor from this node to ground to control the rate of battery reversal. If controlled battery reversal is not desired, leave this pin open.
3	LCF	—	**Loop Closure Filter Capacitor.** Connect a capacitor from this node to V_{CC} to filter the loop closure detector. If loop closure filtering is not required, leave this node open.
4	BGND	G	**Battery Ground.** Ground return for the battery supply.
7	V_{BAT2}/PWR	P	**Auxiliary Battery.** If a lower-voltage auxiliary battery is used, connect the auxiliary battery supply to this node. If a power control resistor is used, connect the power control resistor from this node to V_{BAT1}. If no power control technique is used, connect this node to V_{BAT1}.
8	V_{BAT1}	P	**Office Battery Supply.** Negative high-voltage power supply.
9	V_{BAT1}	P	**Office Battery Supply.** Negative high-voltage power supply.
10	BGND	G	**Battery Ground.** Ground return for the battery supply.
12	TESTSIG–	I	**Test Input–.** This input injects a test signal to the line when an appropriate test operational state is chosen. This node is active when any TEST mode is chosen, overhead is not increased per ROVH in TEST modes. Connect this node to V_{REF} if not used.
13	TESTSIG+	I	**Test Input+.** This input injects a test signal to the line when an appropriate test operational state is chosen. Before this node can be used, the test sense circuity must be activated via a test mode; then activate Test Input+ via the TEST-R mode. Connect this node to V_{REF} if not used.
14	TESTLEV	O	**Test Level Output.** This output pin will provide a voltage that is proportional to either the dc line voltage, dc line current, ac line voltage, ac line current, or internal reference voltage, dependent upon which operational state is selected.
17	TEST+OUT	O	**TEST+OUT.** Output of TESTSIG+ amplifier.
19	RTS	I	**Ring Trip Sense.** Sense input for the ring trip detector.
20	RSW	O	**Ring Lead Ringing Access Switch.** Ringing relay connects this pin to pin RRING. Connect this pin to pin PR through a 400 Ω current-limiting resistor.
22	RRING	I	**Ringing Access.** Input to solid-state ringing access switch. Connect to ringing generator.
24	PR	I/O	**Protected Ring.** The output of the ring driver amplifier and input to loop sensing connected through solid-state break switch. Connect to subscriber loop through overvoltage/current protection.
27	PT	I/O	**Protected Tip.** The output of the tip driver amplifier and input to loop sensing connected through solid-state break switch. Connect to subscriber loop through overvoltage/current protection.
30	TRING	O	**Tip Ringing Return.** Ring relay connects this pin to PT. Connect to ringing supply return.
32	NSTAT	O	**Loop Status.** The output of the loop status detector (loop start detector wired-OR with ring trip detector). This loop status supervision output is not controlled by the data latch.
33	B3	I	**Data Control Input.** See Table 2 and Table 3 for details.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type	Name/Function
34	B2	I	**Data Control Input.** See Table 2 and Table 3 for details.
35	B1	I	**Data Control Input.** See Table 2 and Table 3 for details.
36	B0	I	**Data Control Input.** See Table 2 and Table 3 for details.
38	RESET	I	**Reset.** A logic low will override the B[0:3] and LATCH inputs and reset the state of the SLIC to the disconnect state and the switch to the all-off state.
39	LATCH	I	**Latch Control Input.** Edge-level sensitive control for data latches.
40	V_{DD}	P	**5 V Digital Power Supply.** 5 V supply for digital circuitry.
42	DGND	G	**Digital Ground.** Ground return for V_{DD} current.
44	TRGDET	O	**Tip/Ring Ground Detect.** When high, this open collector output indicates the presence of a ring ground or a tip ground. This supervision output may be used in ground start, ground key, or common-mode fault detection applications. It has an internal pull-up.
45	ICM	I	**Common-Mode Current Sense.** To program tip or ring ground sense threshold, connect a resistor to ground and connect a capacitor to AGND to filter 50 Hz/60 Hz. If unused, the pin is connected to ground.
48	VTX	O	**Tip/Ring Voltage Output.** This output is a voltage that is directly proportional to the differential tip/ring current. A resistor from this node to ITR sets the device transimpedance. Gain shaping for termination impedance with a COMBO I codec is also achieved with a network from this node to ITR.
49	ITR	I	**Transmit Gain.** A current output that is proportional to the differential current flowing from tip to ring. Input to AX amplifier. Connect a resistor from this node to VTX to set transmit gain to 300 Ω. Gain shaping for termination impedance with a COMBO I codec is also achieved with a network from this node to VTX.
50	TXI	I	**Transmit ac Input (Noninverting).** Connect a 0.1 µF capacitor from this pin to VTX for dc blocking.
53	VITR	O	**Transmit ac Output Voltage.** The output is a voltage that is directly proportional to the differential ac tip/ring current. This output is connected via a proper interface network to the codec.
54	RCVP	I	**Receive ac Signal Input (Noninverting).** This high-impedance input controls the ac differential voltage on tip and ring.
55	RCVN	I	**Receive ac Signal Input (Inverting).** This high-impedance input controls the ac differential voltage on tip and ring.
56	AGND	G	**Analog Ground.** Ground return for V_{CC} current.
58	V_{CC}	P	**5 V Analog Power Supply.** 5 V supply for analog circuitry.
60	LCTH	I	**Loop Closure Program Input.** Connect a voltage source or ground, via a resistor, to this point to program the loop closure threshold.
62	V_{REF}	O	**SLIC Internal Reference Voltage.** Output of internal 2.35 V SLIC reference voltage.
64	OVH	I	**Overhead Voltage Program Input.** Connect a voltage source to this point to program the overhead voltage. Voltage source may be external or derived via a resistor divider from V_{REF}. A programmable external voltage source may be used to provide software control of the overhead voltage. If a resistor or voltage source is not connected, the overhead voltage will default to approximately 5.5 V (sufficient to pass 3.14 dBm in to 900 Ω). If the default overhead is desired, connect this pin to ground.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type	Name/Function
65	V_{PROG}	I	**Current-Limit Program Input.** Connect a voltage source to this point to program the dc current limit. Voltage source may be external or derived via a resistor divider from V_{REF}. A programmable external voltage source may be used to provide software control of the loop closure threshold.
66	CF2	—	**Filter Capacitor.** Connect a 0.1 µF capacitor from this node to ground for filtering.
67	CF1	—	**Filter Capacitor.** Connect a capacitor from this node to OVH to control the rate of change of the overhead voltage. If controlled overhead is not desired, leave this node open.
5, 6, 11, 15, 16, 18, 21, 23, 25, 26, 28, 29, 31, 37, 41, 43, 46, 47, 51, 52, 57, 59, 61, 63, 68	NC	—	**No Connection.**

Operating States

Input State Coding

State control is via a tiered logic system. The device must initially be set to a primary control state (B3 = 0). This will set the operational state of the SLIC and switch. The secondary control table (B3 = 1) is used to turn on the TESTLEV+ amplifier or to turn on the test circuitry and TESTSIG– amplifier to enter a test state. The primary state of the device (the state of the SLIC and switch) will not change when entering a secondary control state.

Within the primary control table, each state will set the SLIC and the switch to a specific mode. The exception is the tip-amp and ring-amp states. The tip-amp and ring-amp states will change the configuration of the switches, but leave the state of the SLIC unchanged from the previous primary control mode.

Once a primary (device) control state is selected, the TESTSIG+ amplifier or the TESTSIG– amplifier and test circuitry can be activated via a secondary control state. Within the secondary control table, there are TEST active and TEST-R active modes. Upon entering a TEST active mode in the secondary control table, both TESTLEV output and TESTSIG– input are active and the test switches set to the appropriate condition. (See Figure 2.) An exception is the V_{REF} test active mode. Upon entering V_{REF}, only the TESTLEV output is active, and the internal (2.35 V typical) reference voltage appears at TESTLEV. In the V_{REF} mode, the TESTSIG– input is deactivated.

TEST-R modes will only activate the TESTSIG+ amplifier. In order to use TESTSIG+, first enter a TEST mode to turn on the test circuit (also turns on TESTSIG–), then enter a TEST-R mode to turn on the TESTSIG+ amplifier. TEST-R mode is designed for testing of higher voltage signals such as many be seen in ringer equivalent tests.

Once TESTSIG+ is on, the user may reverse the battery in the primary state table without turning off TESTSIG+. If the user goes to scan, ring, or disconnect mode, TESTSIG+ is turned off.

Unlike TESTSIG+, the test feature, once on, will remain on if the user transitions to forward active, reverse active, scan, ring, or disconnect state in the primary state table.

TESTSIG+ is deactivated by selecting TEST off in the secondary control table.

Data control is via a parallel latched data control scheme. Data latches are edge-level sensitive. Data is latched in when the LATCH control input goes low. Data must be set up 200 ns before LATCH goes low and held 50 ns after LATCH goes high. While LATCH is low, the user should not change the data control inputs at B0, B1, B2, and B3. The data control inputs at B0, B1, B2, and B3 may only be changed when LATCH is high. NSTAT supervision output is not controlled by the LATCH control input.

Operating States (continued)

Input State Coding (continued)

Table 2. Primary Control States

B3	B2	B1	B0	RESET	State
0	0	0	0	1	Scan
0	0	0	1	1	Powerup, forward battery
0	0	1	0	1	Powerup, reverse battery
0	0	1	1	1	Tip and ring amp open
0	1	0	0	1	Ring
0	1	0	1	1	Tip amp
0	1	1	0	1	Ring amp
0	1	1	1	1	Disconnect, break-before-make
X	X	X	X	0	Reset—disconnect, break-before-make, and TESTLEV high impedance

Table 3. Secondary Control States

B3	B2	B1	B0	Type	Active	State	Change Test Switch Configuration[1]
1	0	0	0	Test	TESTLEV, TESTSIG–	Voltage: Tip to Ring	Y
1	0	0	1	Test	TESTLEV, TESTSIG–	Voltage: Tip to Ground	Y
1	0	1	0	Test	TESTLEV, TESTSIG–	Voltage: Ring to Ground	Y
1	0	1	1	Test	TESTLEV, TESTSIG–	Current: Tip to Ring—VTX	Y
1	1	0	0	Test	TESTLEV	Voltage: Reference—V_{REF}	Y
1	1	0	1	Test	TESTLEV, TESTSIG–	Current: Tip to Ring—VITR	Y
1	1	1	0	Test	TESTLEV, TEST+OUT, TESTSIG+	TEST-R	N
1	1	1	1	Test	TESTLEV	TEST-R off	N

1. Refer to Figure 2.

Table 4. Supervision Coding

Pin NSTAT	Pin TRGDET
0 = off-hook or ring trip	0 = ring ground
1 = on-hook and no ring trip	1 = no ring ground

State Definitions

Primary Control Modes

Powerup, Forward Battery

- Normal talk and battery feed state.
- Pin PT is positive with respect to pin PR.
- All ac transmission and dc feed circuits are powered up.
- On-hook transmission is enabled.
- Thermal shutdown is active.
- Battery window comparator sense shutdown is on.
- Switch break switches (SW1 and SW2) are closed and ring access switches (SW3 and SW4) are open.
- V_{BAT1} is applied to tip and ring during on-hook conditions.
- Automatic battery switch selects V_{BAT1} or V_{BAT2} during off-hook conditions.
- All supervision circuits except for ring trip detector are active.
- Overhead is set via pin OVH.
- TEST+OUT is in the high-impedance mode, and TESTSIG+ input is off unless this feature is selected via the secondary control table.
- NSTAT represents the loop closure detector status.

Powerup, Reverse Battery

- Normal talk and battery feed state.
- Pin PR is positive with respect to pin PT.
- All ac transmission and dc feed circuits are powered up.
- On-hook transmission is enabled.
- Thermal shutdown is active.
- Battery window comparator sense shutdown is on.
- Switch break switches (SW1 and SW2) are closed, and ring access switches (SW3 and SW4) are open.
- V_{BAT1} is applied to tip and ring during on-hook conditions.
- Automatic battery switch selects V_{BAT1} or V_{BAT2} under off-hook conditions.
- All supervision circuits except for ring trip detector are active.
- Overhead is set via pin OVH.
- TEST+OUT is in the high-impedance mode, and TESTSIG+ input is off unless this feature is selected via the secondary control table.
- NSTAT represents the loop closure detector status.

Scan

- Scan clamp circuitry is active.
- Loop closure is active.
- All ac transmission, dc feed, and other supervision circuits, including ring trip, are shut down.
- Test circuitry is powered down.
- Thermal shutdown is active.
- Battery window comparator sense shutdown is on.
- On-hook transmission is disabled.
- Pin PT is positive with respect to PR, and V_{BAT1} is applied to tip/ring.
- Switch break switches (SW1 and SW2) are closed, and ring access switches (SW3 and SW4) are open.
- When the scan clamp circuitry is on, overhead voltage is fixed and not controlled by OVH. Also the current limit is not the normal current limit set at V_{PROG}.
- NSTAT represents the loop closure detector status.

Ground Start

- Tip amplifier is on, and the tip break switch is open.
- The device presents a high impedance (>100 kΩ) to pin PT and a current-limited battery (V_{BAT2}) to PR.
- Common-mode current detector is on.
- Ring trip detector is off.
- Output TRGDET indicates current flowing in the ring lead.
- This is not a defined state in the primary control mode table. It is achieved via the powerup and the ring amp states in the primary control mode table.

State Definitions (continued)

Primary Control Modes (continued)

Ringing

- Switch break switches (SW1 and SW2) are open, and ring access switches (SW3 and SW4) are closed.
- Tip/ring drive amplifiers are powered down.
- Ring trip circuit is active.
- Loop supervision and common-mode current detectors are powered down.
- NSTAT represents the ring trip detector status.

Disconnect—Break Before Make

- The tip and ring amplifiers are turned off to conserve power.
- Break switches (SW1 and SW2) and ring access switches (SW3 and SW4) are open. This mode is also used as a transitional mode to achieve break-before-make switching from the power ring to active or scan mode.
- All supervision circuits are powered down; NSTAT overrides the actual loop condition and is forced high (on-hook).

Tip Amp

- The tip-side break switch is closed, and the ring-side break switch and ring access switches are open.
- SLIC mode is unaffected by reconfiguring the ring relay via this mode; therefore, SLIC will remain in the mode it was in prior to selecting this mode.

Ring Amp

- The ring-side break switch is closed, and the tip-side break switch and ring access switches are open.
- SLIC mode is unaffected by reconfiguring the ring relay via this mode; therefore, SLIC will remain in the mode it was in prior to selecting this mode.

Tip and Ring Amp Open

- The tip-side and ring-side break switches are open and the ring access switches are open.
- SLIC mode is unaffected by reconfiguring the break switches via this mode; therefore, SLIC will remain in the mode it was in prior to selecting this mode.
- This is the calibration mode for differential and single-ended tip/ring current measurements.

Reset

- Selection of device reset via the RESET pin will set the device into the disconnect, break-before-make, and TESTLEV high impedance state.

Secondary Control Mode States

Voltage: Tip to Ground

- A voltage proportional to the tip-to-ground voltage appears at the TESTLEV output.
- TESTSIG– input is on.

Voltage: Ring to Ground

- A voltage proportional to the ring-to-ground voltage appears at the TESTLEV output.
- TESTSIG– input is on.

Voltage: Tip to Ring

- A voltage proportional to the differential tip-to-ring voltage appears at the TESTLEV output.
- TESTSIG– input is on.

Current: Tip to Ring—VTX

- A voltage proportional to the ac, plus dc tip-to-ring differential current, tip-to-ground current, or ring-to-ground current appears at the TESTLEV output. Use this state for dc measurements.
- Choice is determined by primary control mode table.
- Differential current is selected by choosing powerup forward or reverse from the primary control mode table.
- Tip-to-ground or ring-to-ground current is selected by first choosing powerup forward or reverse from the primary mode table, and then choosing tip amp or ring amp from the primary mode table.
- TESTSIG– input is on.

State Definitions (continued)

Secondary Control Mode States (continued)

Current: Tip to Ring—VITR

- A voltage proportional to the ac tip-to-ring differential current, tip-to-ground current, or ring-to-ground currents appears at TESTLEV output. Use this state for ac measurements.
- Choice is determined by primary control mode table.
- Differential current is selected by choosing powerup forward or reverse from the primary control mode table.
- Tip-to-ground current or ring-to-ground current is selected by first choosing powerup forward or reverse from the primary mode table, and then choosing tip amp or ring amp from the primary mode table.
- TESTSIG– input is on.

Voltage: Reference—VREF

- A voltage proportional to the internal dc reference voltage (V_{REF}) appears at the TESTLEV output.
- TESTSIG–/TESTSIG+ inputs are off.
- This is the calibration state for voltage measurements.

TEST-R

- The TESTSIG+ input is activated.
- The TEST+OUT output is activated.
- Device mode per primary control mode table. Turn on the test sense circuitry by choosing the appropriate test state via the secondary control table. Once test sense circuitry is active, choose TEST-R to turn on TESTSIG+ amplifier.

TEST-R Off

- The TESTSIG+ input is deactivated.
- TEST+OUT is high impedance.
- Device mode is per primary control mode table.

Special States

Thermal Shutdown

- Not controlled via truth table inputs.
- This mode is caused by excessive heating of the device, which may be encountered in an extended power cross situation.
- Upon reaching the thermal shutdown temperature, the device will enter an all-off mode.
- Upon cooling, the device will re-enter the state it was in prior to thermal shutdown.
- Hysteresis is built in to prevent oscillation. In this mode, supervision output NSTAT is forced low (off-hook) regardless of loop status or if the disconnect logic state is selected.

Battery Out of Range

- Not controlled via truth table inputs.
- This mode is caused by a battery out of range; that is, the battery voltage rising above or below a specified threshold.
- Upon reaching the specified high or low battery voltage, the device will enter an all-off mode.
- Upon the battery returning to the specified normal operating range, the device will re-enter the state it was in prior to the low battery shutdown.
- Hysteresis is built in to prevent oscillation. In this mode, supervision output NSTAT is forced low (off-hook) regardless of loop status or if the disconnect logic state is selected.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 5. Absolute Maximum Ratings

T_A = 25 °C.

Parameter	Symbol	Min	Max	Unit
5 V dc Supplies (V_{CC} + V_{DD})	—	–0.5	7.0	V
High Office Battery Supply (V_{BAT1})	—	–75	0.5	V
Auxiliary Office Battery Supply (V_{BAT2})	—	—	V_{BAT1} to 0.5 V	V
Ringing Voltage	—	—	110	Vrms
Logic Input Voltage	—	–0.5	V_{CC} + 0.5 V	V
Maximum Junction Temperature	—	—	165	°C
Storage Temperature Range	—	–40	125	°C
Relative Humidity Range	—	5	95	%
Switch 1, 2, 3; Pole to Pole	—	—	320	V
Switch 4; Pole to Pole	—	—	465	V
Switch Input to Output	—	—	320	V

Note: The IC can be damaged unless all ground connections are applied before, and removed after, all other connections. Furthermore, when powering the device, the user must guarantee that no external potential creates a voltage on any pin of the device that exceeds the device ratings. For example, inductance in a supply lead could resonate with the supply filter capacitor to cause a destructive overvoltage.

Electrical Characteristics

In general, minimum and maximum values are testing requirements. However, some parameters may not be tested in production because they are guaranteed by design and device characterization. Typical values reflect the design center or nominal value of the parameter; they are for information only and are not a requirement. Minimum and maximum values apply across the entire temperature range (–40 °C to +85 °C) and entire battery range (–36 V to –70 V). Unless otherwise specified, typical is defined as 25 °C, V_{CC} = V_{DD} = 5.0, V_{BAT1} = –48 V V_{BAT2} = –25 V. Positive currents flow into the device.

Table 6. Device Operating Conditions and Powering

Parameter	Min	Typ	Max	Unit
Temperature Range	–40	—	85	°C
Humidity Range	5	—	95[1]	%RH
V_{BAT1} Operational Range	–36	–48	–72	V
V_{BAT2} Operational Range	–19	–25	V_{BAT1}	V
5 V dc Supplies (V_{CC}, V_{DD})	4.75	5.0	5.25	V
Supply Currents, Scan State				
No Loop Current, V_{BAT} = –48 V, V_{CC} = V_{DD} = 5 V:				
$I_{VCC+VDD}$	—	2	2.5	mA
I_{VBAT1}	—	100	200	µA
Power Dissipation	—	15	22	mW
Supply Currents, Forward/Reverse Active State				
No Loop Current, with On-hook Transmission, Test Not Active,				
V_{BAT} = –48 V, V_{CC} = V_{DD} = 5 V:				
$I_{VCC+VDD}$	—	6	6.5	mA
I_{VBAT1}	—	1.1	1.4	mA
Power Dissipation	—	83	100	mW
Supply Currents, Forward Disconnect State, V_{BAT} = –48 V, V_{CC} = V_{DD} = 5 V:				
$I_{VCC+VDD}$	—	1.2	1.85	mA
I_{VBAT1}	—	20	275	µA
Power Dissipation	—	7	22.5	mW
Supply Currents, Ring State, No Loop Current,				
V_{BAT} = –48 V, V_{CC} = V_{DD} = 5 V, V_{RING} = 80 Vrms:				
$I_{VCC+VDD}$	—	5	—	mA
I_{VBAT1}	—	200	—	µA
I_{RING} Generator	—	1.5	—	mA
Power Dissipation	—	155	—	mW
Power Adders, V_{CC} = V_{DD} = 5 V,				
Power Test Amplifiers Drawn Only from 5 V Supply:				
TESTSIG+	—	1	—	mW
TESTSIG–	—	5	—	mW
PSRR 500 Hz—3000 Hz:				
V_{BAT1}, V_{BAT2}	45	—	—	dB
V_{CC}	30	—	—	dB

1. Not to exceed 26 grams of water per kilogram of dry air.

Electrical Characteristics (continued)

Package Thermal Characteristics

Table 7. Thermal

Parameter	Min	Typ	Max	Unit
Thermal Protection Shutdown (T_{TSD})[1, 2]	150	165	—	°C
Thermal Resistance, Junction to Ambient (Θ_{JA})[1, 3]: Natural Convection 1S2P Board	—	17	—	°C/W

1. This parameter is not tested in production. It is guaranteed by design and device characterization.
2. Careful thermal design as a function of maximum battery, loop length, maximum ambient temperature packages, thermal resistance, airflow, PCB board layers, and other related parameters must ensure that thermal shutdown temperature is not exceeded under normal use œndi-tions.
3. Airflow, PCB board layers, and other factors can greatly affect this parameter.

Ring Trip Detector

Table 8. Ring Trip Detector

Parameter	Min	Typ	Max	Unit
Voltage at Input that Will Cause Ring Trip After Appropriate Zero Crossings	±2.0	±2.4	±2.8	V
Voltage at Input that Will Cause Immediate Ring Trip	±12	±15	±18	V
Ringing Source[1]: Frequency (f) dc Voltage ac Voltage	 19 –39.5 60	 20 — —	 28 –57 105	 Hz V Vrms
Ring Trip (NDET = 0)[2, 3]: Loop Resistance Trip Time NDET Valid	 2000 — —	 — — —	 — 200 80	 Ω ms ms

1. The ringing source may be either of the following:
   The ringing source consists of the ac and dc voltages added together (battery-backed ringing); the ringing return is ground.
   The ringing source consists of only the ac voltage (earth-backed ringing); the ringing return is the dc voltage.
2. NDET must also indicate ring trip when the ac ringing voltage is absent (<5 Vrms) from the ringing source.
3. Pretrip ringing must not be tripped by a 10 kΩ resistor in parallel with an 8 µF capacitor applied across tip and ring.

Electrical Characteristics (continued)

Test

Table 9. ac Test Source

Parameter	Min	Typ	Max	Unit
Test Source[1, 2]:				
Frequency (f1)	—	—	16	kHz
Signal Gain (TESTSIG–/+ to amplifier outputs) $V_{TESTSIG}$ = 0.35 Vrms	—	10	—	—
Signal Gain Voltage Coefficient	—	1.27	—	1/V
Input Signal	0	—	0.75	Vrms
Harmonic Distortion[3]	—	—	5	%

1. ac test signal should be ac coupled into TESTSIG.
2. A pull-down resistor to V_{REF} should be connected to TESTSIG.
3. This parameter is not tested in production; it is guaranteed by design and characterization.

Table 10. Test Sense

Parameter	Min	Typ	Max	Unit
Single-ended Voltage Gain ±10 V on Tip/Ring	—	1/75	—	—
Differential Voltage Gain ±10 V on Tip/Ring	—	1/75	—	—
Voltage Gain Accuracy (single-ended or differential)	–3.5	—	3.5	%
Voltage Coefficient	—	0.01[1]	—	%/V
Current Gain at VTX (dc) Differential	19.6	20	20.4	V/A
Current Gain at VTX (dc) Single-ended	9.8	10	10.2	V/A
Current Gain at VITR (ac) Differential	291	300	309	V/A
Current Gain at VITR (ac) Single-ended	145.5	150	154.5	V/A
Overload at VTX[2]	±105	—	—	mA
Overload at VITR[2]	±7	—	—	mA
V_{REF}	—	2.35	—	V
V_{REF} Accuracy	–5	—	5	%
TESTLEV Offset Relative to V_{REF}	–40	—	40	mV
TESTLEV Amplifier:				
Output Voltage Swing	AGND + 0.35	—	V_{CC} – 0.4	V
Input Voltage Swing	AGND + 0.35	—	V_{CC} – 1.0	V

1. This is the voltage coefficient with respect to tip/ring voltage. See Table 22 for application of this parameter.
2. This parameter is not tested in production; it is guaranteed by design and characterization.

Electrical Characteristics (continued)

SLIC 2-Wire Port

Table 11. SLIC 2-Wire Port

Parameter	Min	Typ	Max	Unit
PT and PR Drive Current = dc + Longitudinal + Signal Currents	105	—	—	mApeak
Signal Current	10	—	—	mArms
Longitudinal Current Capability per Wire (Longitudinal current is independent of dc loop current.)	8.5	15	—	mArms
dc Active Mode Loop Current – I_{LIM} (R_{LOOP} = 100 Ω):				
Programming Range (2.5 Vrms max into 200 Ω ac)	10	—	70	mA
Voltage at V_{PROG}	0.2	—	1.4	V
dc Active Mode Loop Current – I_{LIM} (R_{LOOP} = 100 Ω):				
Programming Range (5 Vrms max into 200 Ω ac)	10	—	45	mA
Voltage at V_{PROG}	0.2	—	0.9	V
dc Current-limit Variation:				
V_{PROG} = 0.8 V (I_{LIMIT} = 40 mA)	—	5	—	%
Loop Resistance Range (from PT/PR) (3.17 dBm overload into 600 Ω):				
I_{LOOP} = 20 mA at V_{BAT1} = –48 V	1900	—	—	Ω
V_{REF}	2.23	2.35	2.47	V
Offset at V_{PROG}	–40	—	40	mV
dc Feed Resistance (includes internal SLIC dc resistance and break switch resistance)	50	75	110	Ω
dV/dT Sensitivity at PT/PR	—	200	—	V/µs
Ground Start State PT Resistance	100	—	—	kΩ
Powerup Open Loop Voltages (V_{BAT1} = –48 V):				
Forward/Reverse Active Mode |PT – PR| – V_{BAT1} (programming range)	5.5	—	15	V
Voltage at OVH (programming voltage)	0	—	1.9	V
Forward/Reverse Active Mode |PT – PR| – V_{BAT1} (OVH to GND)	5.5	6.1	—	V
Common Mode	—	(V_{BAT1} + 1)/2	—	V
Powerup Open Loop Voltages:				
Scan Mode |PT – PR| – V_{BAT1}	0	—	13.5	V
Loop Closure Threshold:				
Voltage at LCTH	0	—	V_{REF}	V
Loop Closure Threshold Hysteresis	—	20	—	%
Ground Key/Ground Start:				
Gain ICM to TRGDET	—	1	—	µA/mA
Common-mode Detector Threshold	5	—	10	mA
Longitudinal to Metallic Balance at PT/PR (Test Method: *IEEE*® Std. 455):				
300 Hz to 3.4 kHz (L9520G)	61	—	—	dB
300 Hz to 3.4 kHz (L9520K)	54	—	—	dB
Metallic to Longitudinal (harm) Balance:				
200 Hz to 4000 Hz	40	—	—	dB

Electrical Characteristics (continued)

Analog Pin Characteristics

Table 12. Analog Pin Characteristics

Parameter	Min	Typ	Max	Unit
TXI (input impedance)	75	105	—	kΩ
V_{PROG} Input Bias Current[1] (current flows out of pin)	—	–50	–250	nA
V_{OH} Input Bias Current[1] (current flows out of pin)	—	–50	–250	nA
LCTH Input Bias Current[1] (current flows into pin)	—	50	250	nA
VTX:				
Output Offset	—	—	±40	mV
Output Drive Current	±1	—	—	mA
Output Voltage Swing (±1 mA load):				
Maximum	AGND	—	V_{CC}	V
Minimum	AGND + 0.35	—	V_{CC} – 0.4	V
Output Short-circuit Current	—	—	±50	mA
Output Load Resistance[1]	10	—	—	kΩ
Output Load Capacitance[1]	—	50	—	pF
VITR:				
Output Offset	—	—	±100	mV
Output Drive Current	±1	—	—	mA
Output Voltage Swing (±1 mA load):				
Maximum	AGND AGND	—	V_{CC}	V
Minimum	+ 0.35	—	V_{CC} – 0.4	V
Output Short-circuit Current	—	—	±50	mA
Output Load Resistance[1]	10	—	—	kΩ
Output Load Capacitance[1]	—	50	—	pF
RCVN and RCVP:				
Input Voltage Range (V_{CC} = 5.0 V)	0	—	V_{CC} – 0.5	V
Input Bias Current	—	—	±1.5	µA

1. This parameter is not tested in production. It is guaranteed by design and device characterization.

Electrical Characteristics (continued)

ac Feed Characteristics

Table 13. ac Feed Characteristics

Parameter	Min	Typ	Max	Unit
ac Termination Impedance[1]	150	600	1400	Ω
Total Harmonic Distortion (200 Hz—4 kHz)[2]:				
Off-hook	—	—	0.3	%
On-hook	—	—	1.0	%
Transmit Gain[3] f = 1004 Hz, 1020 Hz:				
PT/PR Current to VITR	–291	–300	–309	V/A
Receive Gain, f = 1004 Hz, 1020 Hz Open Loop:				
RCVP or RCVN to PT—PR (gain = 2)	1.94	2	2.06	—
ac Feed Resistance (includes internal SLIC ac resistance and break switch resistance)	50	75	110	Ω
Gain vs. Frequency (transmit and receive)[2] 900 Ω = 2.16 µF Termination, 1004 Hz Reference:				
200 Hz—300 Hz	–0.3	0	0.05	dB
300 Hz—3.4 kHz	–0.05	0	0.05	dB
3.4 kHz—20 kHz	–3.0	0	0.05	dB
20 kHz—266 kHz	—	—	2.0	dB
Gain vs. Level (transmit and receive)[2] 0 dBV Reference:				
–55 dB to +3.0 dB	–0.05	0	0.05	dB
Idle-channel Noise (tip/ring) 600 Ω Termination:				
Psophometric	—	–82	–77	dBmp
C-Message	—	8	13	dBrnC
3 kHz Flat	—	—	20	dBrn
Idle-channel Noise (VTX) 600 Ω Termination:				
Psophometric	—	–82	–77	dBmp
C-Message	—	8	13	dBrnC
3 kHz Flat	—	—	20	dBrn

1. Set externally either by discrete external components or a third- or fourth-generation codec. Any complex impedance R1 + R2 || C between 150 Ω and 1400 Ω can be synthesized.
2. This parameter is not tested in production. It is guaranteed by design and device characterization.
3. VITR transimpedance depends on the resistor from ITR to VTX. This gain assumes an ideal 6.34 kΩ, the recommended value. Positive current is defined as the differential current flowing from PT to PR.

Electrical Characteristics (continued)

Logic Inputs and Outputs, V_{DD} = 5.0 V

Table 14. Logic Inputs and Outputs

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltages:					
Low Level	V_{IL}	–0.5	0.4	0.7	V
High Level	V_{IH}	2.0	2.4	V_{DD}	V
Input Current:					
Low Level (V_{DD} = 5.25 V, V_I = 0.4 V)	I_{IL}	—	—	±50	µA
High Level (V_{DD} = 5.25 V, V_I = 2.4 V)	I_{IH}	—	—	±50	µA
Output Voltages (CMOS):					
Low Level (V_{DD} = 4.75 V, I_{OL} = 180 µA)	V_{OL}	0	0.2	0.4	V
High Level (V_{DD} = 4.75 V, I_{OH} = –20 µA)	V_{OH}	2.4	—	V_{CC}	V

Timing Requirements

Table 15. Timing Requirements

Parameter	Symbol	Min	Typ	Max	Unit
Minimum Setup Time from B0, B1, B2, B3 to LATCH	t_{SU}	200	—	—	ns
Minimum Hold Time from LATCH to B0, B1, B2, B3	t_{HL}	50	—	—	ns

Data control is via a parallel latched data control scheme. Data latches are edge-level sensitive. Data is latched in when the LATCH control input goes low. Data must be set up by t_{SU} ns before LATCH goes low, and hold t_{HL} ns after LATCH goes high. While LATCH is low, the user should not change the data control inputs at B0, B1, B2, and B3. The data control inputs at B0, B1, B2, and B3 may only be changed when LATCH is high. NSTAT supervision output is not controlled by the LATCH control input.

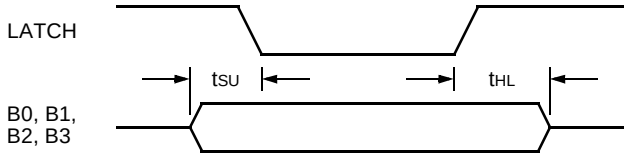

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Figure 4. Timing Requirements

Electrical Characteristics (continued)

Switch Characteristics

Table 16. Break Switches (SW1, SW2)

Parameter	Min	Typ	Max	Unit
Off State:				
Maximum Differential Voltage	—	—	±320[1]	V
dc Leakage Current (Vsw = ±320 V)	—	—	±20	µA
On State (See On-State Switch I-V Characteristics section.):				
Resistance	—	18	28	Ω
Maximum Differential Voltage (V_{MAX})[2]	—	—	320	V
Foldback Voltage Breakpoint 1 (V1)	72	—	—	V
Foldback Voltage Breakpoint 2 (V2)	V1 + 0.5	—	—	V
dc Current Limit 1 ($I_{LIMIT}1$)	105	250	450	mA
dc Current Limit 2 ($I_{LIMIT}2$)	2	—	—	mA
Dynamic Current Limit:				
10 x 700 µs, 1000 V Applied Surge T < 0.5 µs	—	2.5	—	A
dV/dT Sensitivity[2, 3]	—	200	—	V/µs

1. At 25 °C, maximum voltage rating has a temperature coefficient of 0.167 V/°C.
2. This parameter is not tested in production. It is guaranteed by design and device characterization.
3. Applied voltage is 100 Vp-p square wave at 100 Hz to measure dV/dT sensitivity.

Table 17. Ring Return Switch (SW3)

Parameter	Min	Typ	Max	Unit
Off State:				
Maximum Differential Voltage	—	—	±320[1]	V
dc Leakage Current (Vsw = ±320 V)	—	—	±20	µA
On State (See On-State Switch I-V Characteristics section.):				
Resistance	—	60	100	Ω
Maximum Differential Voltage (V_{MAX})[2]	—	—	130	V
dc Current Limit	—	200	—	mA
Dynamic Current Limit:				
10 x 700 µs, 1000 V Applied Surge T = 0.5 µs	—	2.5	—	A
dV/dT Sensitivity[2, 3]	—	200	—	V/µs

1. At 25 °C, maximum voltage rating has a temperature coefficient of 0.167 V/°C.
2. This parameter is not tested in production. It is guaranteed by design and device characterization.
3. Applied voltage is 100 Vp-p square wave at 100 Hz to measure dV/dT sensitivity.

Electrical Characteristics (continued)

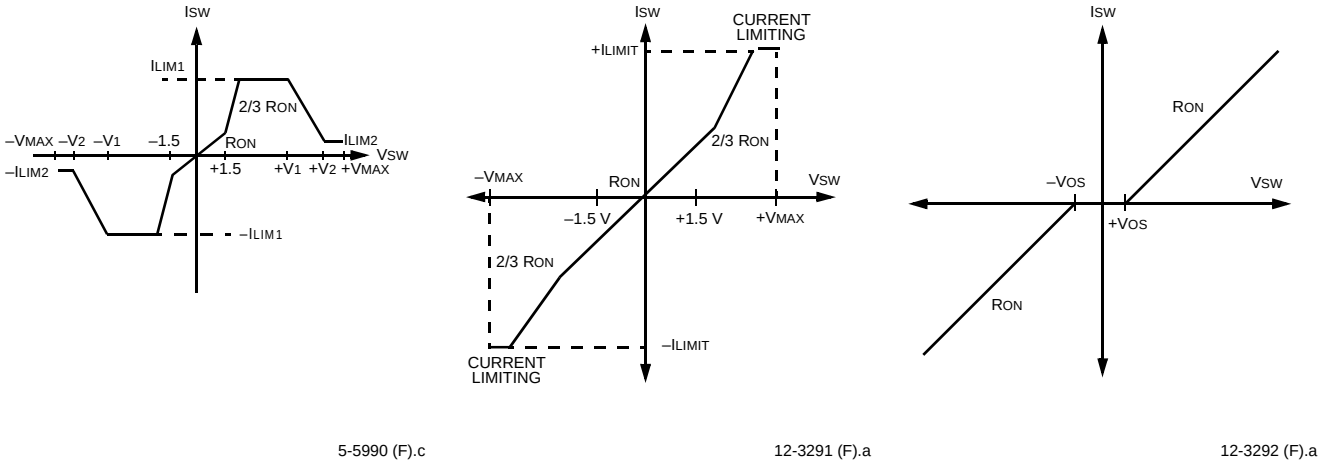
Switch Characteristics (continued)

Table 18. Ringing Access Switch (SW4)

Parameter	Min	Typ	Max	Unit
Off State:				
Maximum Differential Voltage	—	—	±475	V
dc Leakage Current (Vsw = ±475 V) (pole to pole)	—	—	±20	µA
Isolation	—	—	±320	V
On State (See On-State Switch I-V Characteristics section.):				
Resistance	—	—	15	Ω
Voltage	—	—	3	V
Steady-state Current[1]	—	—	150	mA
Surge Current (10 x 700 µs pulse)[2]	—	—	2	A
Release Current	—	500	—	µA
dV/dT Sensitivity[2, 3]	—	200	—	V/µs

1. Choice of secondary protector and feed resistor should ensure these ratings are not exceeded. A minimum 400 Ω feed resistor is recommended.
2. This parameter is not tested in production. It is guaranteed by design and device characterization.
3. Applied voltage is 100 Vp-p square wave at 100 Hz to measure dV/dT sensitivity.

On-State Switch I-V Characteristics



5-5990 (F).c 12-3291 (F).a 12-3292 (F).a

A. Line Break Switch SW1, SW2 **B. Ring Return SW3** **C. Ring Access SW4**

Figure 5. On-State Switch I-V Characteristics

Test Configurations

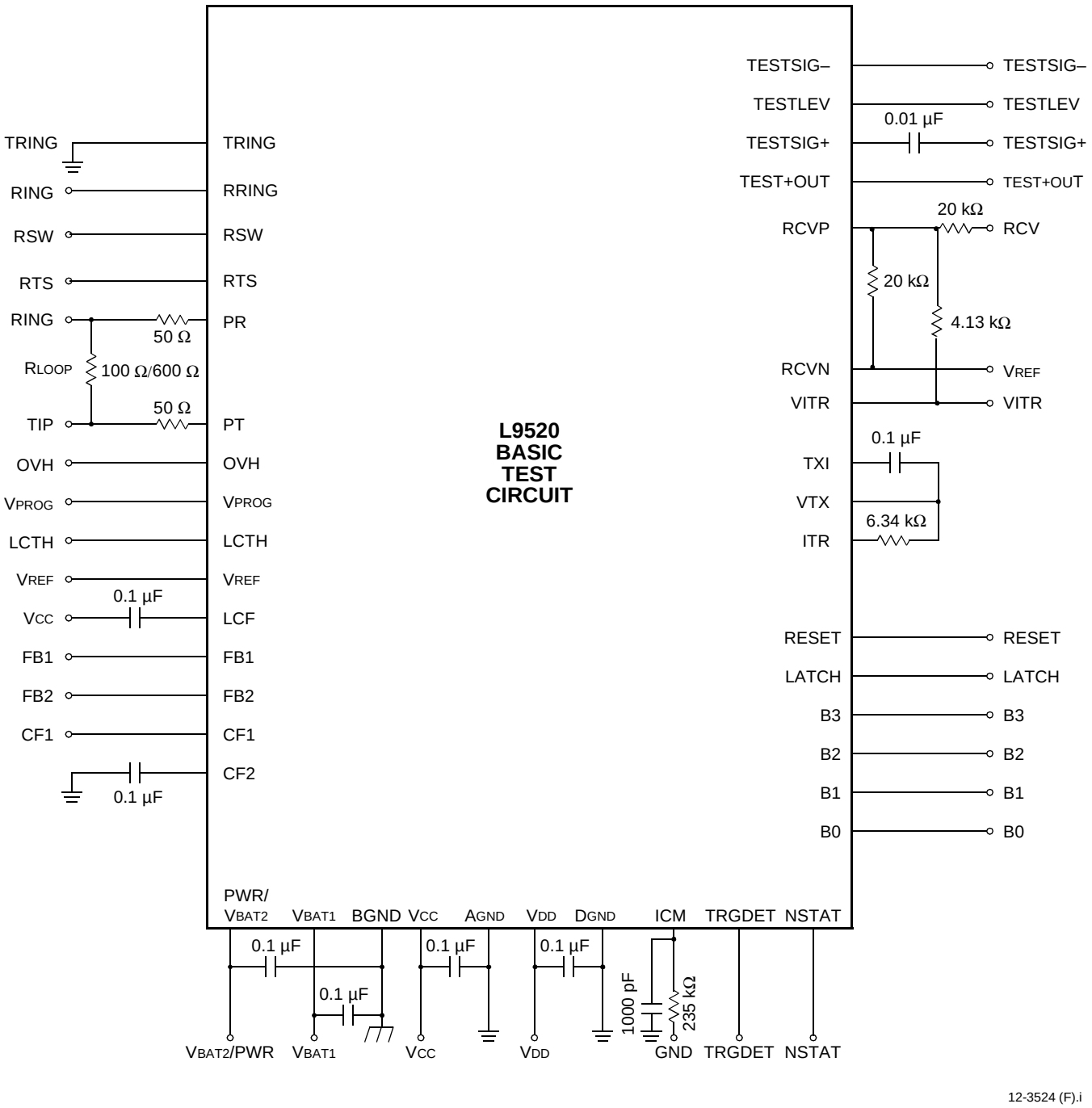
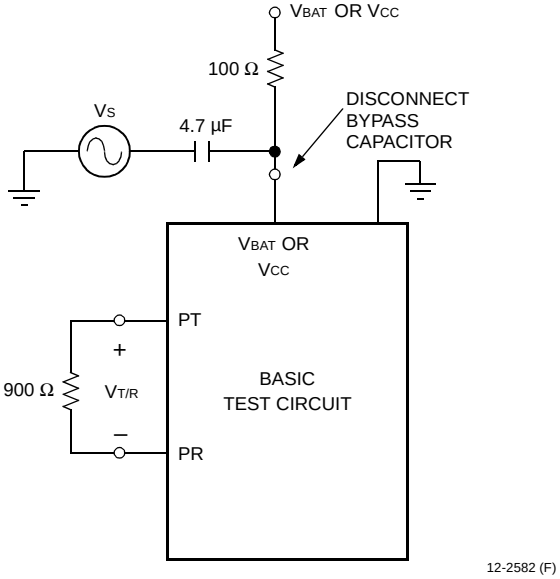


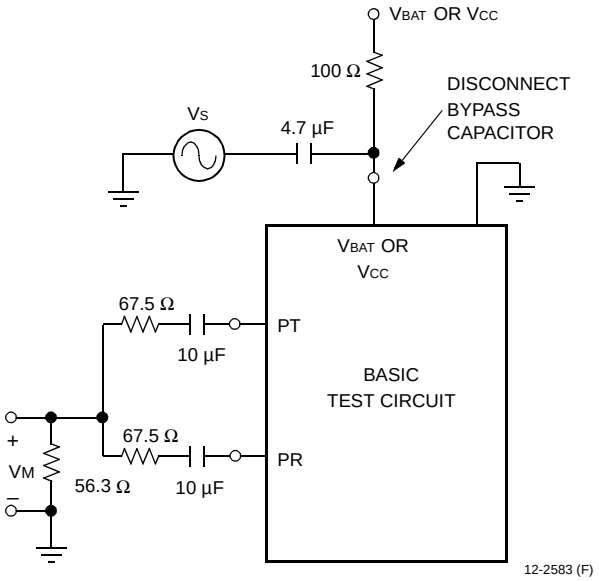
Figure 6. Basic Test Circuit

Test Configurations (continued)



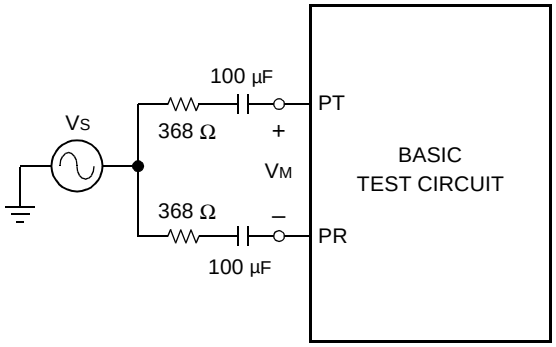
$$PSRR = 20 \log \frac{V_S}{V_{T/R}}$$

Figure 7. Metallic PSRR



$$PSRR = 20 \log \frac{V_S}{V_M}$$

Figure 8. Longitudinal PSRR

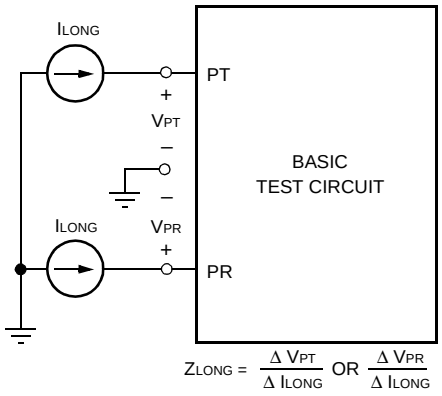


$$\text{LONGITUDINAL BALANCE} = 20 \log \frac{V_S}{V_M}$$

12-2584 (F)

ANSI®/*IEEE* STANDARD 455-1985

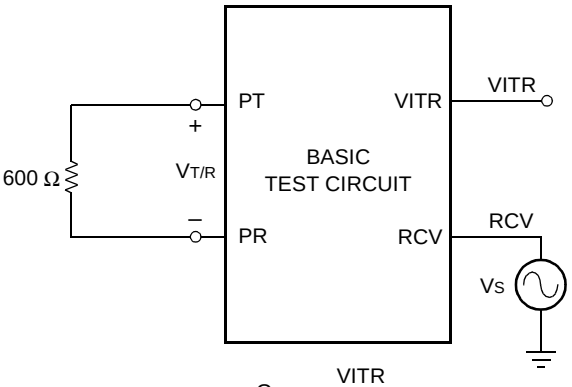
Figure 9. Longitudinal Balance



$$Z_{LONG} = \frac{\Delta V_{PT}}{\Delta I_{LONG}} \text{ OR } \frac{\Delta V_{PR}}{\Delta I_{LONG}}$$

12-2585 (F)

Figure 10. Longitudinal Impedance



$$G_{XMT} = \frac{VITR}{V_{T/R}}$$

$$G_{RCV} = \frac{V_{T/R}}{V_{RCV}}$$

12-2587 (F).g

Figure 11. ac Gains

Applications

dc Characteristics

Power Control

Under normal device operating conditions, thermal design must ensure that the device temperature does not rise above the thermal shutdown. Power dissipation is highest with higher battery voltages, with higher current limit, and under shorter dc loop conditions. Higher ambient temperature will reduce thermal margins. Power control may be done in several ways, by use of the integrated automatic battery switch and a lower-voltage auxiliary battery or by use of a power control resistor with single battery operation. The thermal capability of the 68-pin MLCC package is sufficient enough to allow for single battery operation without the power control resistor when the device is used under lower-power operating conditions.

Power Derating

Operating temperature range, maximum current limit, maximum battery voltage, minimum dc loop length, protection resistors' values, number of PCB board layers, and airflow, will influence the overall thermal performance. The still-air thermal resistance of the 68-pin MLCC package is typically 17 °C/W for a 1S2P JEDEC standard board with natural convection airflow.

The L9520 will enter thermal shutdown at a temperature of 150 °C. The thermal design should ensure that the SLIC does not reach this temperature under normal operating conditions.

For this example, assume a maximum ambient operating temperature of 85 °C, a maximum current limit of 30 mA, and a maximum battery of –56 V. Further assume a (worst-case) minimum dc loop of 20 Ω for wire resistance, 50 Ω protection resistors, and 200 Ω for the handset. Include the effects of parameter tolerance in these calculations.

$T_{TSD} – T_{AMBIENT(max)}$ = allowed thermal rise
150 °C – 85 °C = 65 °C

Allowed thermal rise =
package thermal impedance x SLIC power dissipation
65 °C = 17 °C/W x SLIC power dissipation

Allowed SLIC power dissipation (P_D) = 3.82 W

Therefore, in this example, if the total power dissipated on the SLIC is less than 3.82 W, it will not enter thermal shutdown. Total SLIC power is calculate as follows:

Total P_D = maximum battery x (maximum current limit) (current limit accuracy) + SLIC quiescent power.

For the L9520, the worst-case SLIC on-hook active quiescent power is 100 mW. Therefore,

Total off-hook power = $(I_{LOOP})(1.05) \times (V_{BATAPPLIED})$ + SLIC quiescent power
Total off-hook power = (0.030 A)(1.05) x (52) + 100 mW
Total off-hook power = 1.864 W

The power dissipated in the SLIC is the total power dissipation less the power that is dissipated in the loop.

SLIC P_D = total power – loop power

Loop off-hook power = $(I_{LOOP} \times 1.05)^2 \times (R_{LOOPdcmin} + 2R_P + R_{HANDSET})$
Loop off-hook power = $\{(0.030\ A)(1.05)\}^2 \times (20\ \Omega + 100\ \Omega + 200\ \Omega)$
Loop off-hook power = 317.5 mW

SLIC off-hook power = total off-hook power – loop off-hook power
SLIC off-hook power = 1.864 W – 0.3175 W
SLIC off-hook power = 1.5465 W < 3.82 W

Therefore, under the operating conditions of this example, the thermal capability of the 68-pin MLCC package is enough to ensure that the L9520 will not be driven into thermal shutdown and that no additional power control measures are needed. If, however, for a given set of operating conditions, the thermal capabilities of the package are not enough to ensure that the SLIC is driven into thermal shutdown, then one of the power control techniques described below should be used. Additionally, even if the thermal capability of the 68-pin MLCC package is enough to ensure that the L9520 will not be driven into thermal shutdown, the battery switch technique described below can be used to reduce total short-loop power dissipation.

Automatic Battery Switch

Use of the automatic battery switch controls power dissipation by automatically switching to the lower-voltage auxiliary battery under short dc loop conditions, therefore reducing the short-loop power that is generated. This has the advantage of not only controlling device temperature rise, but reducing overall power dissipation. The switch will automatically apply the appropriate battery to support the dc loop. No logic control is needed to control the switch. Switching is quiet, and the dc loop current will not be interrupted when switching between batteries. The lower-voltage auxiliary battery is connected to the V_{BAT2}/PRW package pin.

Applications (continued)

dc Characteristics (continued)

The equation governing the switch point is as follows:

$$R_{LOOP} = \frac{|V_{BAT2}| - 3.0}{I_{LIM}} - 2R_P - R_{dc}$$

A graph showing loop and battery current versus loop resistance with use of the battery switch is shown in Figure 12.

The V_{BAT2} voltage must be chosen properly so that the power dissipation is minimized. When the voltage at pin PR equals V_{BAT2} + 1 V + (50 Ω x I_{LOOP}), the loop current minus 3.5 mA to 4.5 mA flows into V_{BAT2} and 3.5 mA to 4.5 mA of the loop current plus quiescent current flows into V_{BAT1}.

To choose V_{BAT2}, add the following:

1. Maximum tip overhead voltage (2 V for V_{OVH} = 0).
2. Maximum loop voltage (maximum loop resistance, protection resistance, and dc feed resistance [100 Ω] times the maximum loop current limit).
3. 1 V for the soft switch.

Therefore, for a 40 mA current limit, 640 Ω loop, 30 Ω protection resistors, and 3.17 dBm signal (V_{OVH} = 0):

V_{BAT2} = –(2 + 0.042 x (100 + 60 + 640) + 1) = –36.6 V. Then, for any loop resistance from 0 Ω to 640 Ω, the worst-case V_{BAT1} and V_{BAT2} currents will be:

I_{BAT1} = 1.39 mA + 4.0 mA = 5.39 mA

I_{BAT2} = 42 mA – 5.39 mA = 36.61 mA

Total max power = 1.641 W (V_{BAT} = –48 V)

Note that to minimize power statistically, this may not be the best choice for V_{BAT2}. Over a large number of lines, power is minimized according to the statistical distribution of loop resistance.

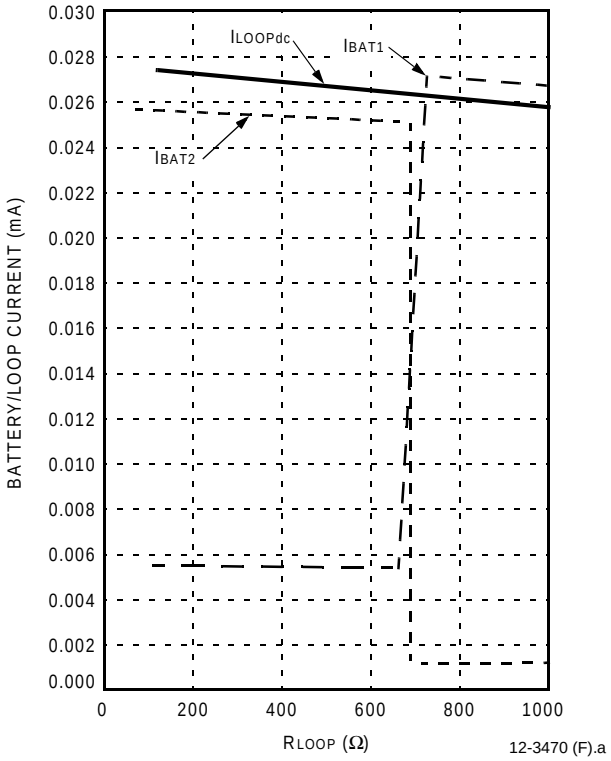


Figure 12. L9520 Loop/Battery Current (with Battery Switch) vs. Loop Resistance

dc Loop Current Limit

In the active modes, dc current limit is programmable via an applied voltage source at the device's V_{PROG} control input. The voltage source may be an external voltage source or derived via a resistor divider network from the V_{REF} SLIC output or an external voltage source. A programmable external voltage source may be used to provide software control of the loop current limit. The loop current limit (I_{LIM}) is related to the V_{PROG} voltage by the following:

I_{LIM} (mA) = 50 x V_{PROG} (V)

Applications (continued)

dc Characteristics (continued)

Note that the overall current-limit accuracy achieved will not only be affected by the specified accuracy of the internal SLIC current-limit circuit (accuracy associated with the 50 term), but also by the accuracy of the voltage source, the accuracy of any external resistor divider network used, and the voltage offsets due to the specified input bias current. If a resistor divider from V_{REF} is used, a lower magnitude resistor will give a more accurate result due to a lower offset associated with the input bias current; however, lower value resistors will also draw more power from V_{REF}. The sum of the two resistors in the resistor divider should be between 75 kΩ and 200 kΩ. Offset at V_{PROG} and V_{REF} accuracies are specified in Table 9 and Table 11.

The previous equation describes the active mode steady-state, current-limit response. There will be a transient response of the current-limit circuit (with the device in the active mode) upon an on- to off-hook transition. Typical active mode transient current-limit response is given in Table 19.

Table 19. Typical Active Mode On- to Off-Hook Tip/Ring Current-Limit Transient Response

Parameter	Value	Unit
dc Loop Current: Active Mode R_{LOOP} = 100 Ω On-hook to Off-hook Transition t < 5 ms	I_{LIM} + 60	mA
dc Loop Current: Active Mode R_{LOOP} = 100 Ω On-hook to Off-hook Transition t < 50 ms	I_{LIM} + 20	mA
dc Loop Current: Active Mode R_{LOOP} = 100 Ω On-hook to Off-hook Transition t < 300 ms	I_{LIM}	mA

The current limit with the SLIC set in an active mode will be different from the current limit with the SLIC set in the scan mode. This is due to differences in the scan clamp circuit versus the active tip/ring drive amplifiers. The scan mode current limit is fixed and is a function of the internal design of the scan clamp circuit. The steady-state scan mode current limit will be a typical 40 mA to 50 mA and may, over temperature and process, vary typically from 30 mA to 110 mA. The scan clamp current limit will typically settle to its steady-state value within 300 ms.

Overhead Voltage

Overhead is programmable in the active mode via an applied voltage source at the device's OVH control input. The voltage source may be an external voltage source or derived via a resistor divider network from the V_{REF} SLIC output or an external voltage source. A programmable external voltage source may be used to provide software control of the overhead voltage.

The overhead voltage (V_{OH}) is related to the OVH voltage by:

V_{OH} = 5.5 V + 5 x V_{OVH} (V)

Overall accuracy is determined by the accuracy of the voltage source and the accuracy of any external resistor divider network used and voltage offsets due to the specified input bias current. If a resistor divider from V_{REF} is used, lower magnitude resistor will give a more accurate result due to a lower offset associated with the input bias current; however, lower value resistors will also draw more power from V_{REF}. The sum of programming resistors should be between 75 kΩ and 200 kΩ.

Note that a default overhead voltage of 5.5 V is achieved by shorting input pin OVH to analog ground. Internally, the SLIC needs typically 2 V from each supply rail to bias the amplifier circuitry. This can be thought of as an internal saturation voltage.

The default overhead provides sufficient headroom for on-hook transmission of a 3.14 dBm signal into 900 Ω.

$$3.14 = 10 \log \frac{V^2}{0.9}$$

V = 1.36 V, which is required over and above the internal saturation voltage for signal swing.

1.36 V + 4 V = 5.36 V < 5.5 V default overhead; therefore, a 3.14 dBm into 900 Ω signal is passed without clipping distortion.

The overhead voltage accuracy achieved will not only be affected by the accuracy of the internal SLIC circuitry, but also by the accuracy of the voltage source and the accuracy of any external resistor divider network used.

In the scan mode, overhead is unaffected by V_{OVH} and internally fixed by the scan clamp circuitry to within the specified limits.

Overhead voltage may need to be increased to accommodate on-hook transmission of higher-voltage signals. For example, the 20 Hz signal used in GR844 ringer equivalent tests.

Applications (continued)

Power Control Resistor (continued)

Loop Range

The dc loop range is calculated using the following:

$$R_L = \frac{|V_{BAT}| - V_{OH}}{I_{LOOP}} - 2R_P - R_{dc}$$

V_{BAT1} is used because the maximum loop range is being calculated. The loop resistance value where the device automatically switches to V_{BAT2} is calculated in the Automatic Battery Switch section of this data sheet.

Battery Feed

The L9520 operates in a dc unbalanced mode. In the forward active state, under open circuit (on-hook) conditions with the default overhead chosen, the tip-to-ring voltage will be a nominal 5.5 V less than the battery. This is the overhead voltage. The tip and ring overhead is achieved by biasing ring a nominal 3.5 V above battery and by biasing tip a nominal 2.0 V below ground.

During off-hook conditions, some dc resistance will be applied to the subscriber loop as a function of the physical loop length, protection, and telephone handset. As the dc resistance decreases from infinity (on-hook) to some finite value (off-hook), the tip-to-ring voltage will decrease as shown in Figure 13.

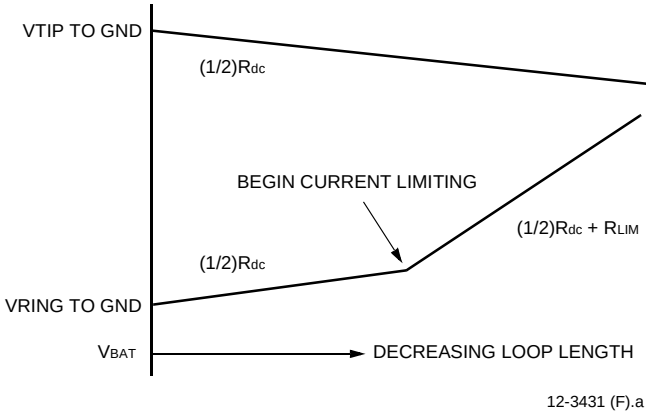


Figure 13. Tip/Ring Voltage

As illustrated in Figure 13, as loop length decreases, the tip-to-ground voltage will decrease with a slope corresponding to one-half the internal dc feed resistance of the SLIC (typical 75 Ω). The ring-to-ground voltage will also decrease with a slope corresponding to one-half the internal dc feed resistance of the SLIC, until the SLIC reaches the current-limit region of operation. At that point, the slope of the ring-to-ground voltage will increase to the sum of one half the internal dc feed resistance plus approximately 10 kΩ.

The dc feed characteristic can be described by the following:

$$I_{LOOP} = \frac{|V_{BAT}| - V_{OH}}{R_{LOOP} + 2R_P + R_{dc}}$$

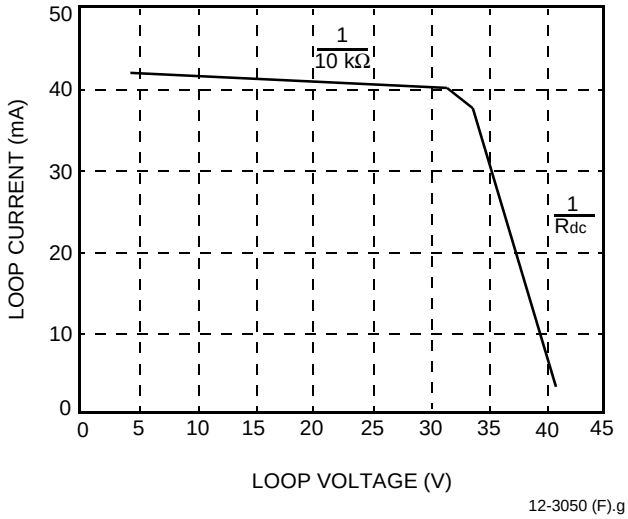
$$V_{T/R} = \frac{(|V_{BAT}| - V_{OH}) \bullet R_{LOOP}}{R_{LOOP} + 2R_P + R_{dc}}$$

Where:
I_{LOOP} = dc loop current.
$V_{T/R}$ = dc loop voltage.
$|V_{BAT}|$ = battery voltage magnitude.
V_{OH} = overhead voltage.
R_{LOOP} = loop resistance, including wire and handset resistance.
R_P = protection resistance.
R_{dc} = SLIC internal dc feed resistance.

Applications (continued)

Power Control Resistor (continued)

Refer to Figure 13 and Figure 14 in this section and to Figure 12 in the Automatic Battery Switch section.



Notes:
V_{BAT1} = –48 V.
V_{BAT2} = –24 V.
I_{LIM} = 40 mA (R_{PROG} = 66.5 kΩ).

Figure 14. L9520 Loop Current vs. Loop Voltage

Starting from the on-hook condition and going through to a short circuit, the curve passes through the following two regions:

- Region 1: On-hook and low loop currents: the slope corresponds to the dc feed resistance of the SLIC (plus any series resistance). The open-circuit voltage is the battery voltage minus the overhead voltage of the device.
- Region 2: Current limit: the dc current is limited to a value determined by V_{PROG}. This region of the dc template has a high resistance (10 kΩ).

Notice that the I-V curve is uninterrupted when the power is shifted from the high-voltage battery to the low-voltage battery (if the auxiliary battery option is used).

This is shown in Figure 12 in the Automatic Battery Switch section.

Battery Reversal Rate

The rate of battery reverse is controlled or ramped by capacitors FB1 and FB2. A chart showing FB1 and FB2 values versus typical ramp time is given in Table 20.

Leave FB1 and FB2 open if it is not desired to ramp the rate of battery reversal.

Table 20. FB1 and FB2 Values vs. Typical Ramp Time

C_{FB1} and C_{FB2}*	Transition Time
0.01 µF	20 ms
0.1 µF	220 ms
0.22 µF	440 ms
0.47 µF	900 ms
1.0 µF	1.8 s
1.22 µF	2.25 s
1.3 µF	2.5 s
1.4 µF	2.7 s
1.6 µF	3.2 s

* Typical recommended value for C_{FB1} and C_{FB2} is less than 0.033 µF.

Longitudinal to Metallic Balance

Longitudinal to metallic balance at PT/PR is specified in the Electrical Characteristics section of this data sheet.

Supervision

Loop Closure

Loop closure supervision threshold is programmed via an applied voltage source or ground, through a resistor at the LCTH input. Loop closure status is presented at the NSTAT output. NSTAT is an unlatched output that represents either the loop closure or ring trip status, depending on the device state. See Table 2 and Table 3 for more details. Loop closure threshold current (I_{LCTH}) is set by the following:

$$\frac{250(V_{REF} - V_{LCTH})}{R_{LCTH}\ (k\Omega)} = I_{LCTH}\ (mA)$$

where:
R_{LCTH} is a resistor from the LCTH node to ground or a voltage source.
V_{LCTH} is ground or an external voltage source.

There is a built-in hysteresis associated with the loop closure detector. The above equation describes the on-hook to off-hook threshold. To help prevent false glitches, the off-hook to on-hook threshold will be a typical 20% lower than the corresponding on-hook to off-hook threshold. Connect a 0.01 µF capacitor to 0.1 µF capacitor from this node to LCF, to V_{CC}, to filter the loop closure detector. The larger the capacitor, the higher the filtering. If loop closure filtering is not required, leave LCF open.

Supervision (continued)

Ring Trip

Ring trip is set by the value of RS1.

The ring trip threshold at the ring trip inputs is ±2.5 V minimum, ±3.5 V maximum.

A resistor value of 400 Ω, as shown in Figure 3, will set the ring trip current threshold to ±7.5 mA typical.

Ring trip is asserted upon entering the ringing mode until the second zero crossing of ringing. This is either a positive-going zero crossing (between –40 V and –30 V at –50 V V_{BAT}) or a negative-going zero crossing (between –10 V and –20 V at –50 V V_{BAT}). The different threshold for positive-going and negative-going zero crossings is the result of hysteresis of approximately 20 V. The act of turning on the switch may or may not produce a ringing zero crossing; therefore, there may be a delay of up to almost one cycle of ringing or 50 ms until NSTAT is high.

Ring trip will not be asserted unless the ring trip threshold is exceeded for two zero crossings. This is either a positive-going zero crossing (between –40 V and –30 V at –50 V V_{BAT}) or a negative-going zero crossing (between –10 V and –20 V at –50 V V_{BAT}). The different threshold for positive-going and negative-going zero crossings is the result of hysteresis of approximately 20 V.

Note that since the ringing voltage is monitored at RSW, one zero crossing can occur at switch turn-on depending on initial conditions.

Ring trip is asserted immediately if the ring trip input is 15 V ± 3 V.

Tip or Ring Ground Detector

In the ground key or ground start applications, a common-mode current detector is used to indicate that either a tip or ring ground has occurred (ground key) or an off-hook has occurred (ground start). The detection threshold is set by connecting a resistor from ICM to ground as follows:

$2350/R_{ICM}$ (kΩ) = I_{TH} (mA)

Additionally, a filter capacitor across R_{ICM} will set the time constant of the detector. No hysteresis is associated with this detector.

Switching Behavior

The solid-state ring relay in the L9520 device is able to provide either make-before-break or break-before-make timing with respect to switching into and out of the ring mode. If switching is done directly into and out of the ring mode, the design of the L9520 will give make-before-break switching with respect to both the ring and tip side switches. To achieve break-before-make switching, the user should, via software control, enter an intermediate all-off mode when switching into and out of the ring mode. The all-off state should be held a minimum of 8 ms.

Make-Before-Break Operation

The break switches are constructed from DMOS transistors. The tip side ring return is also a DMOS transistor. Because the on resistance of the break switches is less than the tip side ring return switch, the break switches are physically bigger. This implies a larger gate to source capacitance, with inherently slower switching speeds since it will take longer to charge or discharge the gate to source capacitance of the break switches (to change the state of the switch). The ring access switch is a pnpn type device. The pnpn device has inherently faster switching speeds than any of the DMOS type switches.

Going from the active to ring mode, the smaller tip side ring return switch and the pnpn ring access switch will change states before the larger break switches. Therefore, the ring contacts are made before the line break switches are broken: make-before-break operation.

Going from the ring mode to active or scan, the natural tendency is for the smaller tip side ring return DMOS to break or open, before the larger DMOS can turn on. This would not be make-before-break operation on the tip side. Therefore, circuitry is added to speed up charging of the tip break switch, to speed up the turn on of that switch to give make-before-break operation on the tip side.

On the ring side, going from the ring mode to the active or scan mode, the pnpn will not turn off until the ring current drops below the hold current of the pnpn device (which is typically 500 µA); this is effectively zero current for zero current turn off. This can take up to one-half cycle of ringing to occur. With this inherent delay in switching by the pnpn ring access switch, the break switches will make contact before the ring access switch breaks contact; so again, make-before-break switching is achieved.

Supervision (continued)

Make-Before-Break Operation (continued)

With the make-before-break switch, there will be a period of time (depending on ring signal frequency but measured in tens of microseconds) where all four switch contacts will be on. This means that the ring generator will be connected through the current-limited break switches to the input of the SLIC device. Current will be limited by the break switch current limit, and this will not damage the SLIC. This current may, however, cause a false glitch at the NSTAT supervision output that will need to be digitally filtered. The board designer should consider any ramifications of this state on the overall system or ring generator and battery design.

The major benefit of make-before-break switching is that it will minimize any impulse noise generated during ringing cadence. In many cases when operating the switch in the make-before-break mode, no special design to switch at zero current and voltage crossing is required. Impulse noise generation when using solid-state relays is documented in the *Impulse Noise and the L758X Series of Solid State Switches* Application Note.

Break-Before-Make Operation

To achieve break-before-make, use the logic control sequence device switching as shown in Table 21.

Table 21. Break-Before-Make Logic Control Sequence Device Switching

State	Break Switches	Ring Switches	Comment
Active/Scan	closed	open	—
Disconnect (all-off)	open	open	hold >8 ms
Ring	open	closed	—
Disconnect (all-off)	open	open	hold >8 ms
Active/Scan	closed	open	—

The advantage of break-before-make operation is that it eliminates the current spike when the ring access relay changes state. The disadvantage is that it forces an all-off state. Under inductive ringing loads, due to Ldi/dt effects, may cause a reduction in the impulse noise performance compared to make-before-break switching.

Protection

External Protection

An external overvoltage clamp is required to ensure that the off-state and on-state ratings of the solid-state break switch and solid-state ring access switch are not exceeded. The solid-state switches in the L9520 are constructed in a dielectrically isolated high-voltage technology. Because of the high device-to-device isolation that is inherent in the dielectric isolation, only a tip-to-ground and a ring-to-ground clamp is required. A tip-to-ring overvoltage clamp is not needed. A foldback or crowbar type device is recommended to minimize power across the solid-state switches under a fault condition.

The break switches and tip return switch are constructed from DMOS transistors. Because the on resistance of the break switches is less than the tip side ring return switch, the break switches are physically bigger and have a higher current handling capability. Additionally, the break switches have a foldback characteristic that enables them to survive a higher on-state voltage (320 V) than the tip ring return switch (130 V), which does not have the foldback characteristic. (See the On-State Switch I-V Characteristics section.) The ring access switch is a pnpn type device. Additionally, the ring side will see the full power ring voltage, and the tip side switch will see the power ringing voltage that is attenuated by the ringing load, subscriber loop, feed resistor, and protection resistors. Because of these differences, the protection requirements on the tip side are different from the protection requirements on the ring side. Therefore, it is recommended that an asymmetrical (with respect to tip and ring) overvoltage protection scheme be used.

Contact your Agere account representative for a recommended protection device.

Additionally, a series protection resistor with a fusible characteristic or a PTC resistor is recommended to limit current during lightning and power cross faults. A minimum 50 Ω is recommended in tip and ring.

Protection (continued)

External Protection (continued)

The overall device protection is achieved through a combination of the external overvoltage and overcurrent devices, along with the integrated thermal shutdown feature, the integrated window comparator, the break switch foldback characteristic, and the dc/dynamic current-limit response of the break and tip return switches.

Active Mode Response at PT/PR

The line break switches and tip return switch are current-limited switches. The current-limit mechanism limits current through the switch to the specified dc current limit under low frequency or dc faults (power cross and/or tip-ring to ground short) and limits the current to the specified dynamic current-limit response under transient faults, such as lightning.

During a lightning fault (typical 1000 V 10 x 700 µs applied surge), the current-limited line break switches will pass typically 2.5 A for 0.5 µs before forcing the break switches off. Once in the off state, the external protection device must ensure that the off-state voltage rating of 320 V is not exceeded. Note that the maximum differential voltage is the positive zener rating of the protection device less the battery voltage, which will appear on the line feed side of the switch.

For a lower-voltage power cross, whose maximum peak voltage is below the foldback voltage breakpoint 1 (V1), the current-limited break switch will pass the current equal to the dc current limit. The current limit has a negative temperature coefficient, so as the device continues to pass current, the current limit will reduce with increasing device temperature. Ultimately, the device will reach the thermal shutdown temperature and the thermal shutdown mechanism will force an all-off state, which will stop current flow and begin device cooling. In the all-off state, the external protection device ensures that the switch off-state voltage rating is not exceeded. Once the device cools significantly, the break switches will turn on, and current will begin to flow again, until temperature forces the all-off state. This will continue until the fault condition is gone.

Sneak-under surge is a voltage surge that is just below the clamping threshold of the secondary protection device. For this type of surge, when the surge voltage is below the foldback voltage breakpoint 1, operation is as described above. When the surge voltage rises above the foldback voltage breakpoint 1 (V1), but is still less than the secondary protector clamping voltage, the line break switch will crowbar into the high-impedance region of its I-V characteristic and reduce current to the specified $I_{LIMIT}2$ value.

For surges whose magnitude range above the trigger of the external secondary protector, the device will operate as described above for the portion of the surge below the secondary protector trigger voltage. When the voltage rises above the external secondary protector's trigger voltage, the secondary protector will crowbar on, shunting fault current to ground and reducing the tip/ring voltage seen at the device.

In the active mode, the external secondary protector must ensure that the off-state voltage ratings of the ring access and ring return switch are not exceeded. Normally, the ring return switch is connected to ground on the TRING side and to the protector on the PT side; therefore, the protector on the tip side in the active mode must clamp at less than 320 V. As will be seen in the Ring Mode Response at PT/PR section, during the power ringing mode, this clamp voltage on the tip side is significantly less than 320 V.

Normally, the ring access switch is connected to the ring generator on the RRING side and to the protector on the PR side; therefore, on one side of the switch, there is the battery voltage and the peak negative ring signal, and on the PR side, the maximum turn-on voltage of the secondary protector. The ring access switch is of pnpn construction. Therefore, if the off-state voltage rating of the ring access switch is exceeded, the device will crowbar into a low-impedance state. This will cause a surge into the ring generator and can cause the on-state current rating of the switch to be exceeded.

The difference of the battery plus peak negative ring signal voltage less the maximum turn on of the secondary protector must not exceed the off-state voltage rating of the ring access switch. Additionally, as the secondary protector will see the power ring signal, the minimum turn-on rating of the secondary protector must be high enough to not clamp the ring signal and cause clipping distortion. The ring side will see the full power ring voltage, and the tip side switch will see the power ringing voltage that is attenuated by the ringing load, subscriber loop, feed resistor, and protection resistors; therefore, the ring side secondary protector requires a higher clamping voltage than the tip side.

Protection (continued)

Ring Mode Response at PT/PR

In this mode, the line break switches are off and the ring access and ring return switch is on. The secondary protectors must ensure that the minimum off-state voltage rating of the line break switches is not exceeded. Note that the maximum differential voltage is the positive zener rating of the protection device less the battery voltage which will appear on the line feed side of the switch.

The ring access switch is a pnpn type switch. This switch has no internal current limiting. Therefore, through external current limit, the user must ensure that the surge ratings (both dynamic and dc for lightning and power cross faults) are not exceeded. A minimum 400 Ω ring feed resistor is recommended. This resistor also will set the ring trip threshold. See the Ring Trip section within the Supervision section of this data sheet.

During a lightning fault (typical 1000 V 10 x 700 µs applied surge), the current-limited tip return switch will pass, typically 2.5 A for 0.5 µs before forcing the switch off. Once in the off state, the external protection device must ensure that the off-state voltage rating of 320 V is not exceeded.

For power cross for lower-voltage faults, the tip side power ringing return switch will behave like the line break switches. However, this switch does not have the foldback clamping feature that is included in the line break switches; therefore, in the on state, the voltage seen by the tip side power ringing return switch before damage is less than the line break switches. The on-state voltage of the line break switches can go up to the off-state voltage rating. The tip side power ringing return voltage should see less than 130 V in the on state. Therefore, the secondary protector on the tip side should have a maximum crowbar voltage of 130 V. With typical protection device tolerance, this implies a minimum clamping voltage of 100 V. The users should ensure, based on minimum loop length, ringing load, and peak ring signal voltage, that the ring signal is not distorted by the (lower) voltage rating of the tip-side protector.

Internal Tertiary Protection

The external secondary protector and switch current limit protect the 320 V high-voltage switches from lightning and power cross conditions. Integrated into the L9520 IC is an internal tertiary protection scheme that is meant to protect the 90 V SLIC portion of the device from residue fault current and voltages that may be passed through the switches to the actual SLIC inputs. This scheme includes an internal diode bridge voltage clamp and a battery out of range detector that forces an all-off condition if the battery voltage falls high or low out of the specified operating range.

Diode Bridge

The internal inputs of the actual SLIC chip are clamped to ground and to V_{BAT1} by an integrated diode bridge. Residual positive fault currents are clamped to ground, and residual negative fault currents are clamped to battery. This implies that the battery have some current-sourcing capability.

High common-mode currents, as may be seen under a fault condition, will be sensed and reduced to zero by the battery monitor circuit (see Battery Out of Range Detector: High (Magnitude) section). However, this detector will not prevent longitudinal current from flowing out of battery. The battery supply must have the ability to source longitudinal currents as specified in the longitudinal current capability requirement in Table 11.

Battery Out of Range Detector: High (Magnitude)

This feature is useful in remote power applications where a dc-dc converter with limited ability to sink current is used as the primary battery supply. Under a fault condition, the diode bridge will want to source current out of the battery. As a function of the dc-dc converter input capacitance and design, this current may cause the magnitude of supply voltage to rise and ultimately cause damage to the supply. To prevent damage to the supply, the L9520 device will monitor the battery supply voltage. If the magnitude of the battery rises above the maximum specified operating battery, the battery out of range detector will force the line break switches and ring access switches into an all-off state, and will also force the SLIC into the disconnect state. This will stop the current flow out of the battery, preventing damage to the battery fault conditions. NSTAT is forced low during this mode of operation.

Battery Out of Range Detector: Low (Magnitude)

The L9520 device will monitor the battery supply voltage. If the magnitude of the battery drops below the minimum specified operating battery, the battery out of range detector will force the line break switches and ring access switches into an all-off state, and will also force the SLIC into the disconnect state. NSTAT is forced low during this mode of operation.

Line Test with Agere T8531/2 Codec

The L9520 and T8531/2 can be used in combination to form a chip set that is optimized for the POTS portion of a POTS and DSL line circuit. This chip set supports line and chip diagnostics on a per-line basis for the POTS per *Telcordia* GR844 specifications. Test algorithms and a detailed test script supporting GR844 requirements are available. Contact your Agere Systems account representative for more details.

All measurements that appear at the TESTLEV output are referenced to the internal V_{REF} voltage of the device. For that reason, there is a test mode in which V_{REF} itself will appear at the TESTLEV output.

When making a voltage measurement, first measure V_{REF} and subtract V_{REF} from $V_{TESTLEV}$.

When making a current measurement, open the line break switches and measure $V_{TESTLEV}$. This value is then subtracted from the $V_{TESTLEV}$ that is seen during the actual measurement. Note that due to internal biasing of the line break switches, the value seen at $V_{TESTLEV}$ with the line break switches open will be less than the value seen with the line break switches closed under on-hook (open-loop) conditions.

TESTSIG–/+ should be externally connected to the device's V_{REF} if it is not used during a test condition. This may be done by a high-impedance pull-up resistor. Additionally, TESTSIG should be ac coupled to the test signal generator.

Table 22 shows design equations to measure the various line voltages and currents.

Table 22. TESTLEV Output Options

Test Mode	Relationship	Comments
Test Off	High Impedance	—
V_{REF}	$V_{TESTLEV} = V_{REF} + V_{OFFSET}$	Unity follower on V_{REF}. This is the voltage measurement calibration state; use the V_{REF} state in the secondary control state table.
Tip-to-Ring Voltage	$(V_{TIP} – V_{RING}) = 75 (1 – 0.0075 \lvert V_{TL}\rvert) \times V_{TL}$ $V_{TL} = V_{TESTLEV} – (V_{REF} + V_{OFFSET})$	Difference amp.
Tip-to-Ground Voltage	$V_{TIP} = –75 (1 – 0.0075 \lvert V_{TL}\rvert) \times V_{TL} + V_{REF} + V_{OFFSET}$ $V_{TL} = V_{TESTLEV} – (V_{REF} + V_{OFFSET})$	Inverting amp.
Ring-to-Ground Voltage	$V_{RING} = –75 (1 – 0.0075 \lvert V_{TL}\rvert) \times V_{TL} + V_{REF} + V_{OFFSET}$ $V_{TL} = V_{TESTLEV} – (V_{REF} + V_{OFFSET})$	Inverting amp.
VTX, Zero Current (tip open, ring open)	$V_{TESTLEV} = V_{ZEROCUR}$	Unity follower on VTX close to $V_{REF} + V_{AXOFFSET} + V_{OFFSET}$. This is the current measurement calibration state. In the secondary control state table, use tip amp or ring amp for single-ended current measurement calibration. Use tip and ring amp for differential current measurement calibration. Do not use the disconnect mode for current calibration.
VTX, dc Current Tip/Ring (tip closed, ring closed)	$V_{TESTLEV} = 20 V/A \times I_{TIP\text{-}to\text{-}RING} + V_{ZEROCUR}$	Differential current.
VTX, dc Current Ring Ground (tip closed, ring open)	$V_{TESTLEV} = 10 V/A \times I_{TIP\text{-}to\text{-}RING} + V_{ZEROCUR}$	Single-ended voltage.
VTX, dc Current Ring Ground (tip open, ring closed)	$V_{TESTLEV} = –10 V/A \times I_{TIP\text{-}to\text{-}RING} + V_{ZEROCUR}$	Single-ended voltage.
VITR, Zero Current (tip open, ring open)	$V_{TESTLEV} = V_{ZAC}$	Unbuffered output of VITR close to $V_{REF} + V_{AXOFFSET} + V_{ACOFFSET}$. This is the current measurement calibration state. In the secondary control state table, use tip amp or ring amp; for single-ended current measurement calibration, use tip and ring amp for differential current measurement calibration. Do not use the disconnect mode for current calibration.
VITR, ac Current (tip closed, ring closed)	$V_{TESTLEV} = 300 V/A \times I_{TIP\text{-}to\text{-}RING} + V_{ZAC}$	—

ac Applications

ac Parameters

There are four key ac design parameters. Termination impedance is the impedance looking into the 2-wire port of the line card. It is set to match the impedance of the telephone loop in order to minimize echo return to the telephone set. Transmit gain is measured from the 2-wire port to the PCM highway, while receive gain is done from the PCM highway to the transmit port. Transmit and receive gains may be specified in terms of an actual gain, or in terms of a transmission level point (TLP), that is, the actual ac transmission level in dBm. Finally, the hybrid balance network cancels the unwanted amount of the receive signal that appears at the transmit port.

Codec Types

First-Generation Codecs

These perform the basic filtering, A/D (transmit), D/A (receive), and µ-law/A-law companding. They all have an op amp in front of the A/D converter for transmit gain setting and hybrid balance (cancellation at the summing node). Depending on the type, some have differential analog input stages, differential analog output stages, +5 V only or ±5 V operation, and µ-law/A-law selectability. These are available in single and quad designs. This type of codec requires continuous time analog filtering via external resistor/capacitor networks to set the ac design parameters. An example of this type of codec is the Agere T7504 quad 5 V only codec.

Third-Generation/Fourth-Generation Codecs

This class of devices includes all ac parameters set digitally under microprocessor control. Depending on the device, it may or may not have data control latches. Fourth-generation codes have additional functionality such as tone plant generation and reception, PPM generation, test algorithms, and echo cancellation. Again, this type of codec may be +5 V only or ±5 V operation, single quad or 16-channel, and µ-law/A-law or 16-bit linear coding selectable. Examples of this type of codec are the Agere T8536/7 (5 V only, quad, standard features), T8533/4 (5 V only, quad with echo cancellation), and T8531/2 (5 V only, 16-channel with self-test).

ac Interface Network

The internal gains of the L9520 are such that this device may only be interfaced to the Agere Systems T8531/2 16-channel third-generation codec, or to any member of the Agere Systems T853X family of quad ac applications.

Design Tools

PSPICE® Models

L9510 and SLIC *PSPICE* models are available for circuit performance evaluation and verification.

Application System

A self-contained microprocessor-controlled application system with the quad third-generation T8534/6/8 or 16-channel T8531/2 codec is available. Any Agere SLIC is interfaced to this system via a daughter board connection. Codec coefficients are generated with Aquarium software and downloaded into the evaluation system via a simple TEXT file. User control is via a PC terminal emulator via an RS232 connection to the system.

Application Boards

Stand-alone SLIC application boards are also available.

ac Applications (continued)

Third-Generation Codec ac Interface Network: Complex Termination

The following reference circuit shows the complete SLIC schematic for interface to the Agere T8536 third-generation. All ac parameters are programmed by the T8536. Note that this codec differentiates itself in that no external components are required in the ac interface to provide a dc termination impedance or for stability. Also, this example illustrates the device using the battery switch with multiple battery operation. The test features are not used in this application. See the T8535/6 data sheet for information on coefficient programming.

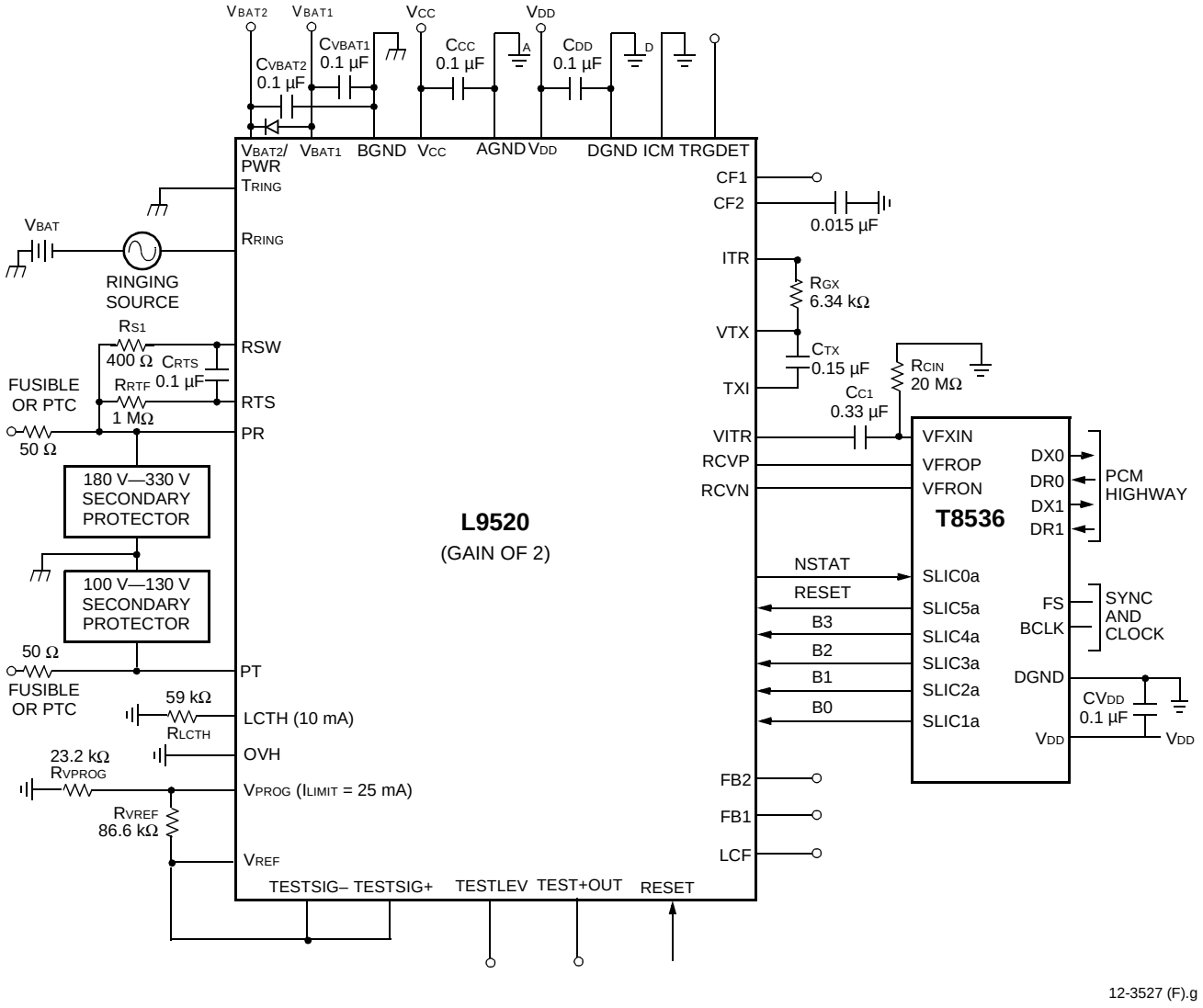


Figure 15. L9520 SLIC for Agere T8536 Third-Generation Codec, Dual-Battery Operation, ac Parameters, Fully Programmable

ac Applications (continued)

Third-Generation Codec ac Interface Network: Complex Termination (continued)

Table 23. L9520 Parts List for Agere T8536 Third-Generation Codec Meter Pulse Application, Dual-Battery Operation, ac and dc Parameters, and Fully Programmable

Name	Value	Tolerance	Rating	Function
Fault Protection				
R_{PR}	50 Ω	1%	Fusible or PTC	Protection resistor.
R_{PT}	50 Ω	1%	Fusible or PTC	Protection resistor.
Protector[1]	180 V to 320 V	—	—	Ring-side secondary protector.
Protector[1]	100 V to 130 V	—	—	Tip-side secondary protector.
Power Supply				
Diode	1N4004	—	—	Reverse battery current.
C_{VBAT1}	0.1 µF	20%	100 V	Filter capacitor.
C_{VBAT2}	0.1 µF	20%	50 V	Filter capacitor.
C_{CC}	0.1 µF	20%	10 V	Filter capacitor.
C_{DD}	0.1 µF	20%	10 V	Filter capacitor.
C_{F2}	0.015 µF	20%	100 V	Filter capacitor.
Ringing/Ring Trip				
C_{RTF}	0.1 µF	20%	100 V	Ring trip filter capacitor.
R_{RTF}	1 MΩ	1%	1/16 W	Ring trip filter resistor.
R_{RS1}	400 Ω	5%	2 W	Sets ring trip threshold.
dc Parameters				
R_{LCTH}	59.0 kΩ	1%	1/16 W	Loop start supervision threshold.
R_{VPROG}	23.2 kΩ	1%	1/16 W	dc current limit.
R_{VREF}	69.8 kΩ	1%	1/16 W	dc current limit/overhead.
PPM				
C_{PPM}	0.01 µF	20%	5 V	ac couple PPM input.
R_{PPM}	17.4 kΩ	1%	1/16 W	PPM hybrid rejection.
C_{PPM1}	—	—	—	PPM hybrid rejection.
ac Interface				
R_{GX}	6.34 kΩ	1%	1/16 W	Sets T/R to VITR transimpedance.
R_{CIN}	20 MΩ	5%	1/16 W	dc bias.
C_{TX}	0.15 µF	20%	10 V	ac/dc separation.
C_{C1}	0.33 µF	20%	10 V	dc blocking capacitor.

1. Contact your Agere account representative for a recommended secondary protection device.

ac Applications (continued)

Fourth-Generation Codec ac Interface Network: Complex Termination

Figure 16 shows the L9520—T8531/2 schematic for use in the POTS plus DSL application, including per line test capability. All ac parameters are programmed by the T8531/2. The ringing is injected through the L9520 solid-state ringing contact. Line voltage and current sense is through the L9520. Test tones are applied through the L9520 PPMIN input rather than the TESTSIG input. GR844 algorithm and test script is provided by the DSP engine in the T8531. Both the test signals and ac signal transmission are sent to the T8532 from the L9520 TESTLEV output, rather than the SLIC VITR output. Dual-battery operation is also shown in Figure 16.

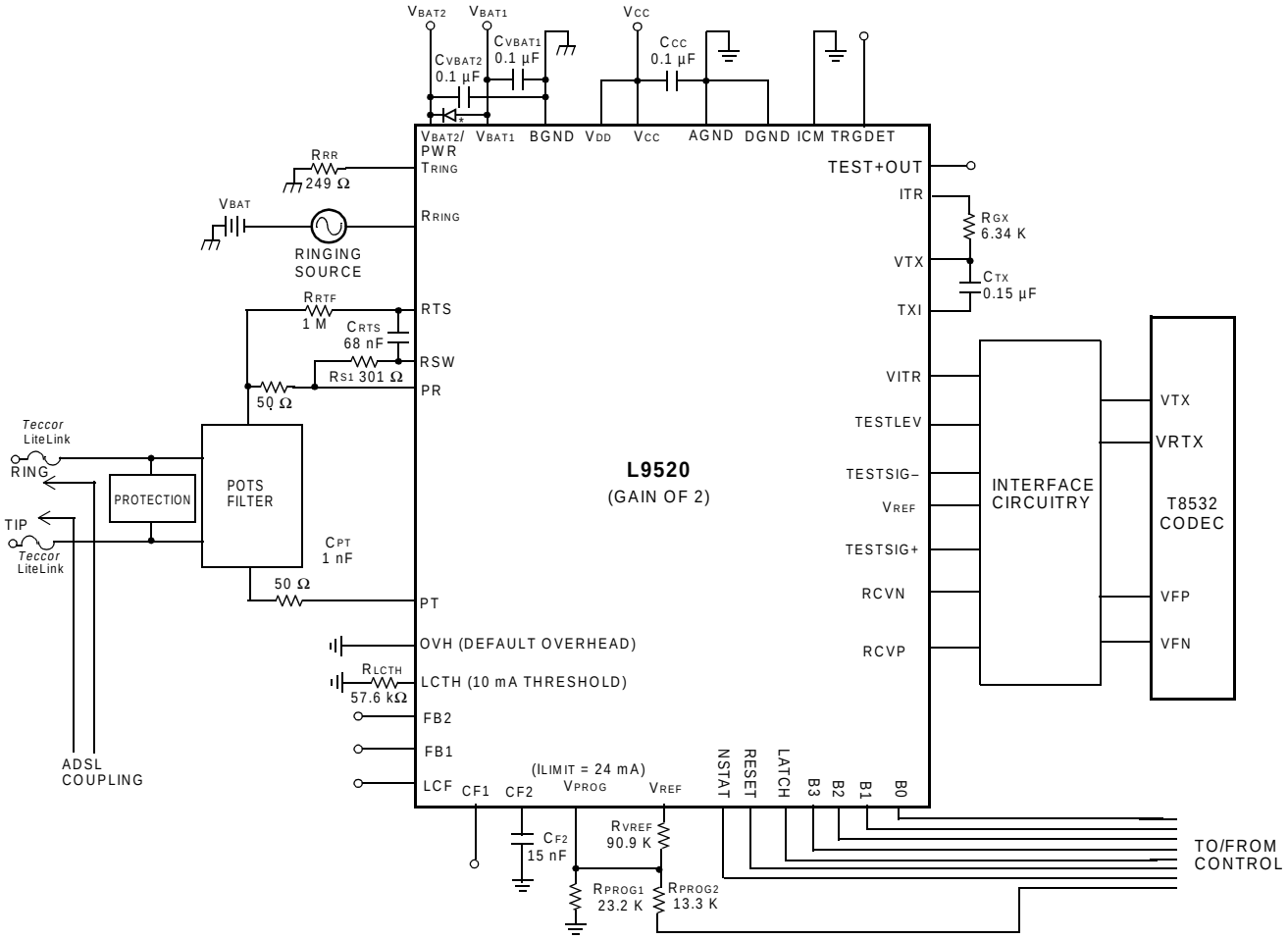


Figure 16. L9520 SLIC for Agere T8531/2 Fourth-Generation Codec, with DSL Compensation, Dual-Battery Operation, ac and dc Parameters, and Fully Programmable per Line Test

ac Applications (continued)

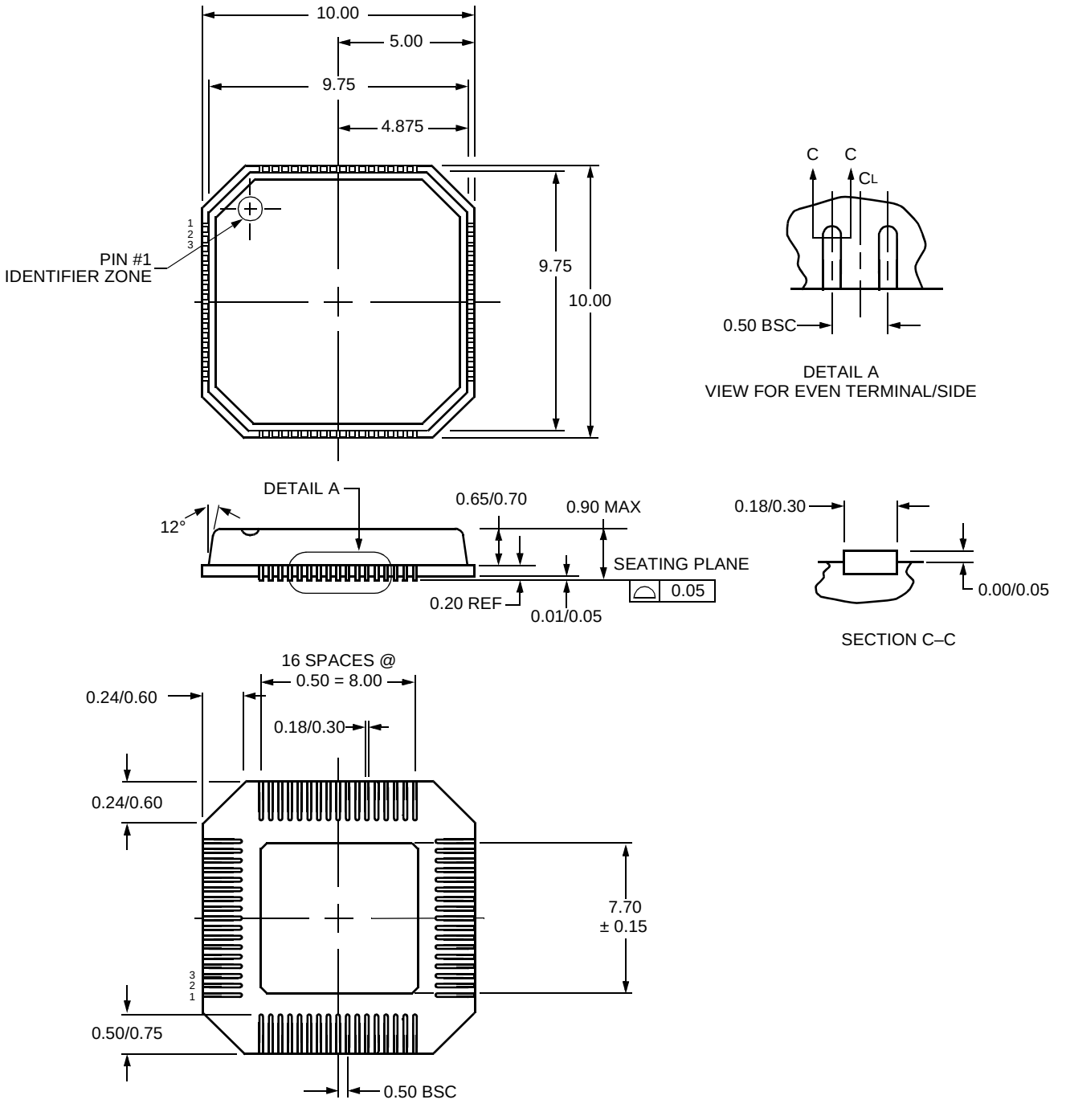
Fourth-Generation Codec ac Interface Network: Complex Termination (continued)

Table 24. L9520 Parts List for Agere T8531/2 Fourth-Generation Codec, with DSL Compensation, Dual-Battery Operation, ac and dc Parameters, and Fully Programmable per Line Test

Name	Value	Tolerance	Rating	Function
Protection				
R_{PR}	50 Ω	1%	0.5 W	Protection resistor.
R_{PT}	50 Ω	1%	0.5 W	Protection resistor.
Power Supply				
Diode	1N4004	—	—	Reverse battery current. **Note:** Only one diode per board is required for this function on a multichannel board.
C_{VBAT1}	0.1 µF	20%	100 V	Filter capacitor.
C_{VBAT2}	0.1 µF	20%	50 V	Filter capacitor.
C_{CC}	0.1 µF	20%	10 V	Filter capacitor.
C_{F2}	0.015 µF	20%	100 V	Filter capacitor.
Ringing/Ring Trip				
C_{RTS}	68 nF	20%	100 V	Ring trip filter capacitor.
R_{RTF}	1 MΩ	1%	1/16 W	Ring trip filter resistor.
R_{S1}	301 Ω	5%	1 W	Sets ring trip threshold.
R_{RR}	249 Ω	5%	1 W	Ring return.
dc Parameters				
R_{LCTH}	57.6 kΩ	1%	1/16 W	Loop start supervision threshold.
R_{VREF}	90.9 kΩ	1%	1/16 W	Loop current limit.
R_{PROG1}	23.2 kΩ	1%	1/16 W	Loop current limit.
R_{PROG2}	13.3 kΩ	1%	1/16 W	Lower loop current limit for test.
ac Interface				
R_{GX}	6.34 kΩ	1%	1/16 W	Sets T/R to VITR transimpedance.
C_{TX}	0.15 µF	20%	10 V	ac/dc separation.

Outline Diagram

68-Pin MLCC



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Ordering Information

Device Part Number	Longitudinal Balance	Package	Comcode
AGRL9520GRS-D	61 dB	68-Pin MLCC, Dry-bagged	700012706
AGRL9520GRS-DT	61 dB	68-Pin MLCC, Dry-bagged, Tape and Reel	700012707
AGRL9520KRS-D	54 dB	68-Pin MLCC, Dry-bagged	700015100
AGRL9520KRS-DT	54 dB	68-Pin MLCC, Dry-bagged, Tape and Reel	700015101

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