LCK4973V
Low-Voltage PLL Clock Driver

Features

- Fully integrated PLL.
- Compatible with *PowerPC*® and *Pentium*® microprocessors.
- 52-pin TQFPT.
- 3.3 V power supply.
- Pin compatible with *Motorola* ® MPC973, CY7BZ9973V, and P16C2973V.
- Selectable 1 differential PECL pair or 2 single-ended TTL inputs
- 2.5 MHz—200 MHz output operation.
- Output-to-output skews <350 ps.
- Total timing budget <800 ps.
- Less than 100 ps typical cycle-to-cycle jitter.

Description

Agere Systems Inc.'s LCK4973V is a 3.3 V PLL-based clock driver for high-performance RISC or CISC processor based systems. The LCK4973V has output frequencies of 2.5 MHz—200 MHz and skews of <350 ps, making it ideal for synchronous systems. The LCK4973V contains 12 low-skew outputs which provide selectable frequency ratios of 1:1, 2:1, 3:1, 3:2, 4:3, 5:1, 5:2, 5:3, 6:1, and 6:5 between outputs.

There is an additional feedback output provided to enable the PLL to multiply the external frequency by 4, 6, 8, 10, 12, 16, or 20.

The outputs can each drive 50 Ω transmission lines; series terminated lines have the ability of driving two 50 Ω lines in parallel, effectively doubling the fan out.

A total timing budget feature is added to provide the maximum error from REFCLK to any of the outputs.

Pin Information

Pin Diagram

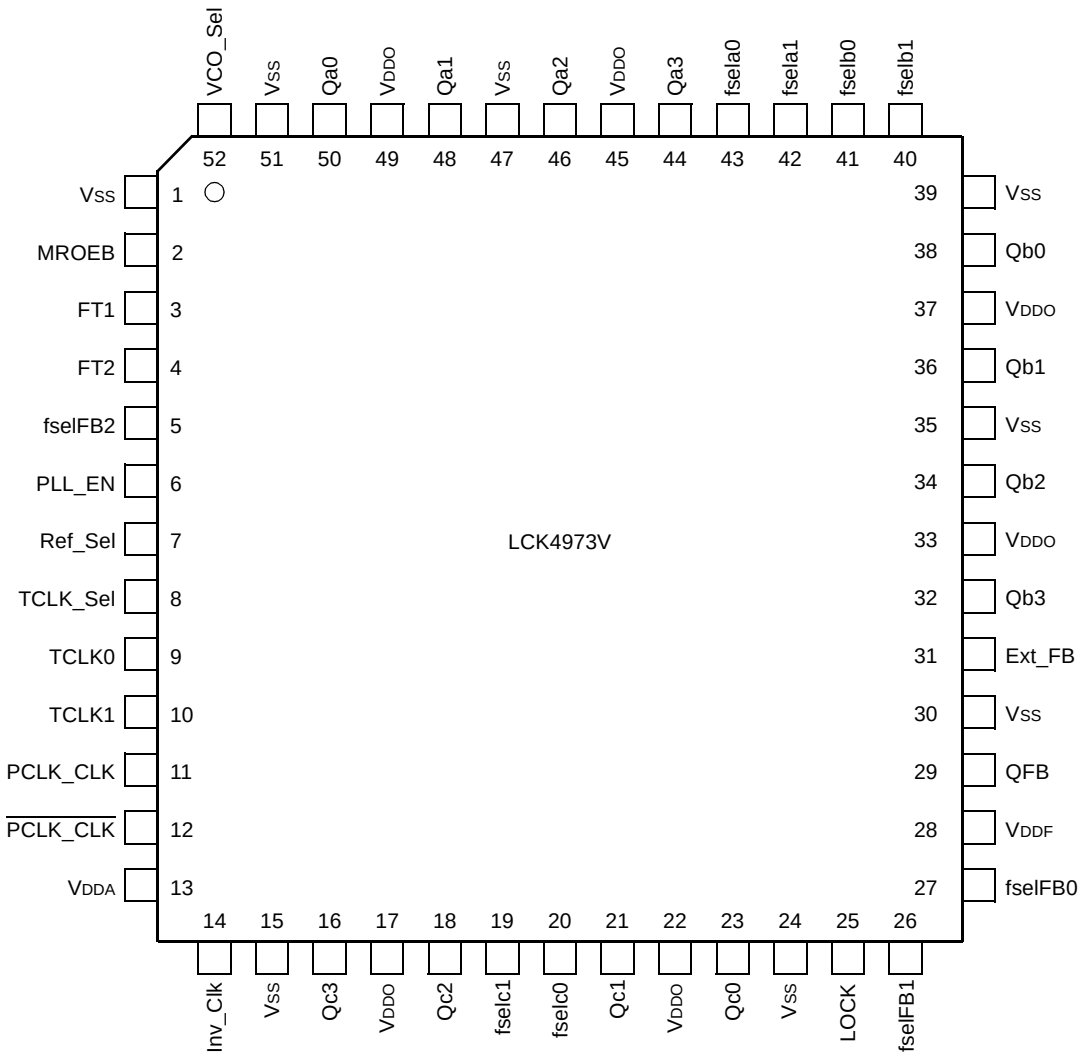


Figure 1. 52-Pin TQFPT

Pin Information (continued)

Pin Descriptions

Table 1. Pin Descriptions

Pin	Symbol	Type	I/O	Description
1, 15, 24, 30, 35, 39, 47, 51	V_{SS}	Ground	—	**PLL Ground.**
2	MROEB	LVTTL	I	**Master Reset and Output Enable Input.** **Note:** When $\overline{MR}$/OE is set high, the PLL will have been disturbed and the outputs will be at an indeterminate frequency until it is relocked.
3, 4	FT[1:2]	LVTTL	I	**Factory Test Mode.** When PLL_EN is high, these inputs are ignored and may be set to any logic level or left open.
5	fselFB2	LVTTL	I	**Feedback Output Divider Function Select.** This input, along with pins fselFB0 and fselFB1, controls the divider function of the feedback bank of outputs. See Table 3 for more details.
6	PLL_EN	LVTTL	I	**PLL Bypass Select.** 0 = The internal PLL is bypassed and the selected reference input provides the clocks to operate the device. 1 = The internal PLL provides the internal clocks to operate the device.
7	Ref_Sel	LVTTL	I	**Reference Select Input.** The Ref_Sel input controls the reference input to the PLL. 0 = The input is selected by the TCLK_Sel input. 1 = The PCLK_CLK is selected.
8	TCLK_Sel	LVTTL	I	**TTL Clock Select Input.** The TCLK_Sel input controls which TCLK input will be used as the reference input if Ref_Sel is set to 0. 0 = TCLK0 is selected. 1 = TCLK1 is selected.
9, 10	TCLK[0:1]	LVTTL	I	**LVTLL Reference Input.** These inputs provide the reference frequency for the internal PLL when selected by Ref_Sel and TCLK_Sel.
11	PCLK_CLK	LVTTL	I	**Differential Reference Input.** This low-voltage differential PECL input provides the reference frequency for the internal PLL when selected by Ref_Sel.
12	$\overline{PCLK\_CLK}$	LVTTL	I	**Differential Reference Input.** This low-voltage differential PECL input provides the reference frequency for the internal PLL when selected by Ref_Sel.
13	V_{DDA}	Power	—	**PLL Power.**
14	Inv_Clk	LVTTL	I	**Invert Mode.** This input only affects the Qc bank. 0 = All outputs of the Qc bank are in the normal phase alignment. 1 = Qc2 and Qc3 are inverted from the normal phase of Qc0 and Qc1.
16, 18, 21, 23	Qc[3:0]	LVTTL	O	**Clock Output.** These outputs, along with the Qa[0:3], Qb[0:3], and QFB outputs, provide numerous divide functions determined by the fsela[0:3], fselb[0:3], and the fselFB[0:2] See Table 2 and Table 3 for more details.
17, 22, 33, 37, 45, 49	V_{DDO}	Power	—	**Output Buffer Power.**

Pin Information (continued)

Pin Descriptions (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type	I/O	Description
19, 20	fselc[1:0]	LVTTL	I	**Output Divider Function Select.** Each pair controls the divider function of the respective bank of outputs. See Table 2 for more details.
25	LOCK	LVTTL	O	**PLL Lock Indicator.** 0 = The PLL is attempting to acquire lock. 1 = This output indicates that the internal PLL is locked to the reference signal. **Note:** If there is no activity on the selected reference input, LOCK may not accurately reflect the state of the internal PLL. This pin will drive logic, but not Thevenin terminated transmission lines. It is always active and does not go to a high impedance state. LOCK provides TEST MODE information when PLL_EN is set to 0.
26	fselFB1	LVTTL	I	**Feedback Output Divider Function Select.** This input, along with pins fselFB1 and fselFB2, controls the divider function of the feedback bank of outputs. See Table 3 for more details.
27	fselFB0	LVTTL	I	**Feedback Output Divider Function Select.** This input, along with pins fselFB0 and fselFB2, controls the divider function of the feedback bank of outputs. See Table 3 for more details.
28	V_{DDF}	Power	—	**PLL Power.**
29	QFB	LVTTL	O	**Clock Output.** This output, along with the Qa[0:3] and Qc[0:3] outputs, provide numerous divide functions determined by the fsela[0:3], fselb[0:3], and the fselFB[0:2]. See Table 2 and Table 3 for more details.
31	Ext_FB	LVTTL	I	**PLL Feedback Input.** This input is used to connect one of the clock outputs (usually QFB) to the feedback input of the PLL.
32, 34, 36, 38	Qb[3:0]	LVTTL	O	**Clock Output.** These outputs, along with the Qa[0:3], Qc[0:3], and QFB outputs, provide numerous divide functions determined by the fsela[0:3], fselb[0:3], and the fselFB[0:2]. See Table 2 and Table 3 for more details.
40, 41	fselb[1:0]	LVTTL	I	**Output Divider Function Select.** Each pair controls the divider function of the respective bank of outputs. See Table 2 for more details.
42, 43	fsela[1:0]	LVTTL	I	**Output Divider Function Select.** Each pair controls the divider function of the respective bank of outputs. See Table 2 for more details.
44, 46, 48, 50	Qa[3:0]	LVTTL	O	**Clock Output.** These outputs, along with the Qb[0:3], Qc[0:3] and QFB outputs, provide numerous divide functions determined by the fsela[0:3], fselb[0:3], and the fselFB[0:2]. See Table 2 and Table 3 for more details.
52	VCO_Sel	LVTTL	I	**VCO Frequency Select Input.** This input selects the nominal operating range of the VCO used in the PLL. 0 = The VCO range is 100 MHz—240 MHz. 1 = The VCO range is 200 MHz—480 MHz.

Functional Description

Table 2. Function Table for Qa, Qb, and Qc

fsela1	fsela0	Qa	fselb1	fselb0	Qb	fselc1	fselc0	Qc
0	0	÷4	0	0	÷4	0	0	÷2
0	1	÷6	0	1	÷6	0	1	÷4
1	0	÷8	1	0	÷8	1	0	÷6
1	1	÷12	1	1	÷10	1	1	÷8

Table 3. Function Table for QFB

fselFB2	fselFB1	fselFB0	QFB
0	0	0	÷4
0	0	1	÷6
0	1	0	÷8
0	1	1	÷10
1	0	0	÷8
1	0	1	÷12
1	1	0	÷16
1	1	1	÷20

Table 4. Function Table for Logic Selection

Control Pin	Logic 0	Logic 1
VCO_Sel	VCO/2	VCO
Ref_Sel	TCLK	PECL
TCLK_Sel	TCLK0	TCLK1
PLL_EN	Bypass PLL	Enable PLL
$\overline{MR}$/OE	Master Reset/Output High-Z	Enable Outputs
Inv_Clk	Noninverted Qc2, Qc3	Inverted Qc2, Qc3

Functional Description (continued)

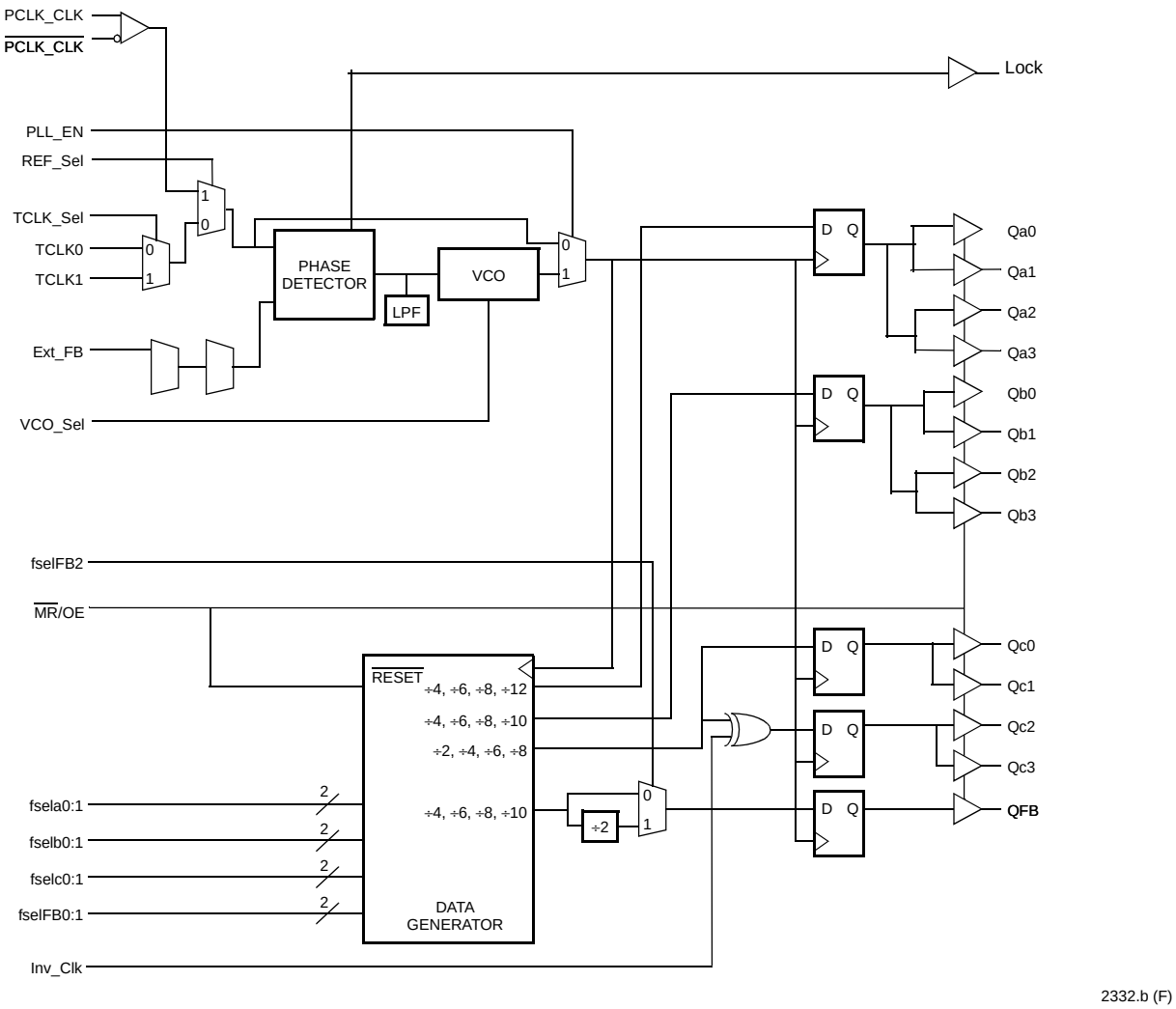


Figure 2. LCK4973V Logic Diagram

Absolute Maximum Ratings

Stresses which exceed the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods of time can adversely affect device reliability.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	–0.5	4.6	V
Input Voltage	V_I	–0.3	V_{DD} + 0.5	V
Input Current	I_{IN}	—	±20	mA
Storage Temperature Range	T_{stg}	–40	125	°C
Ambient Temperature	T_A	–40	125	°C
Output Current Into Outputs (Low)	I_{OUT}	—	40	mA
Latch-up Current	I_L	—	±200	mA

Recommended Operating Conditions

Table 6. Recommended Operating Conditions

Range	Ambient Temperature	V_{DD}
Commercial	0 °C to 70 °C	3.3 V ± 10%
Industrial	–40 °C to 85 °C	3.3 V ± 10%

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Agere Systems employs a human-body model (HBM) and charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in the defined model. No industrywide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes.

Table 7. Handling Precautions

Device	Voltage	Type
LCK4973V	>2,000 V	ESD (electrostatic discharge)

Electrical Characteristics

Table 8. PLL Input Reference Characteristics

T_A = 0 °C to 70 °C, V_{DD} = 3.3 V ± 10%.

Parameter	Symbol	Condition	Min	Max	Unit
TCLK Input Rise/Fall	tr, tf	—[1]	—	3.0	ns
Reference Input Frequency	f_{ref}	—	2.5	120	MHz
Reference Input Duty Cycle	t_{refDC}	—	25	75	%

1. Tested initially and after any design or process changes that may affect these parameters.

dc Characteristics

Table 9. dc Characteristics

T_A = 0 °C to 70 °C, V_{DD} = 3.3 V ± 5%

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	—	2.0	—	3.6	V
Input Low Voltage	V_{IL}	—	—	—	0.8	V
Peak-to-Peak Input Voltage PCLK_CLK	Vp-p	—	400	—	V_{DD}	mV
Common Mode Voltage Range (crossing) PCLK_CLK	V_{CMR}	—[1]	0.8	—	V_{DD}	V
Output High Voltage: All Q Outputs LOCK Outputs	V_{OH}	 I_{OH} = –20 mA[2] I_{OH} = –20 mA[2]	 2.4 2.4	 — —	 — —	V
Output Low Voltage: All Q Outputs LOCK Outputs	V_{OL}	 I_{OL} = 20 mA I_{OL} = 20 mA	 — —	 — —	 0.5 0.5	V
Input Current[3]	I_{IN}	All control inputs $V_{SS} < V_{IN} < V_{DD}$	—	—	±120	µA
		PCLK_CLK and TCLK[0:1] $V_{SS} < V_{IN} < V_{DD}$	—	—	±500	
Hot Insertion Input Current	I_I	PCLK_CLK and TCLK[0:1] $V_{IN} \leq 3.63$ V $V_{DD} = V_{SS}$	—	—	100	µA
Maximum Quiescent Supply Current	I_{CCQ}	Sum all V_{DD} pins PLL_EN = 0 reference off	—	50	150	mA
Maximum Dynamic Supply Current (neglecting output load current)	I_{CCD}	Outputs unloaded fselFB = 010(÷8) reference = 12.5 MHz	—	237	270	mA
Output Dynamic Supply Current	I_{CCN}	—	—	—	8.6	mA
Input Capacitance	C_{IN}	—	—	—	4	pF

1. V_{CMR} is the difference taken form the most positive side of the differential input signal. The high input within the V_{CMR} range and the input lying within the Vp-p specification designates normal operation.
3. The LCK4973V inputs can drive series of parallel terminated transmission lines on the incident edge.
3. Inputs have pull-up/pull-down resistors which affect input current.

Electrical Characteristics (continued)

ac Characteristics

Table 10. ac Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Rise Time	t_r	0.8 V to 2.0 V [1]	0.15	—	1.2	ns
Output Fall Time	t_f	2.0 V to 0.8 V [1]	0.15	—	1.2	ns
Output Duty Cycle	t_{pw}	—[2, 3]	$t_{CYCLE}/2 - 500$	$t_{CYCLE}/2 \pm 400$	$t_{CYCLE}/2 + 500$	ps
Propagation Delay (selected reference input rise to Ext_FB rise): QFB = ÷8	t_{pd}	—[3, 4]	–200	—	200	ps
Output-to-Output Skews	t_{SKEW}	—[3, 5]	—	—	350	ps
PLL V_{CO} Lock Range	f_{VCO}	—	200	—	480	MHz
Maximum Output Frequency	fmax	—	—	—	200	MHz
Cycle-to-Cycle Jitter (peak-to-peak)	t_{jitter}	—	—	—	125	ps
Output Disable Time	t_{OLZ}, t_{OHZ}	—	1	—	10	ns
Output Enable Time	t_{OZL}, t_{OZH}	—	0.5	—	14	ns
Maximum PLL Lock Time	t_{lock}	—	—	—	10	ms
Total Timing Budget	TTB	—[6]	—	—	800	ps

1 Measured no load.
2 t_{PW} measured at $V_{DD}/2$.
3 50 Ω transmission line terminated with $V_{DD}/2$.
4 t_{PD} specified for 50 MHz reference.
5 All outputs at same frequency.
6 $t_{pd} + t_{SKEW} + t_{jitter} = TTB$.

ac Test Loads

For LOCK output only:

- R1 = 910 Ω, R2 = 910 Ω, C_L < 30 pF.

For all other outputs:

- R1 = 100 Ω, R2 = 100 Ω, C_L < 25 pF or 10 pF connected to output pin.

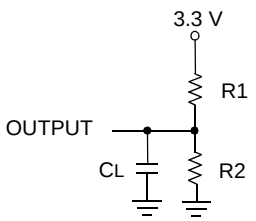
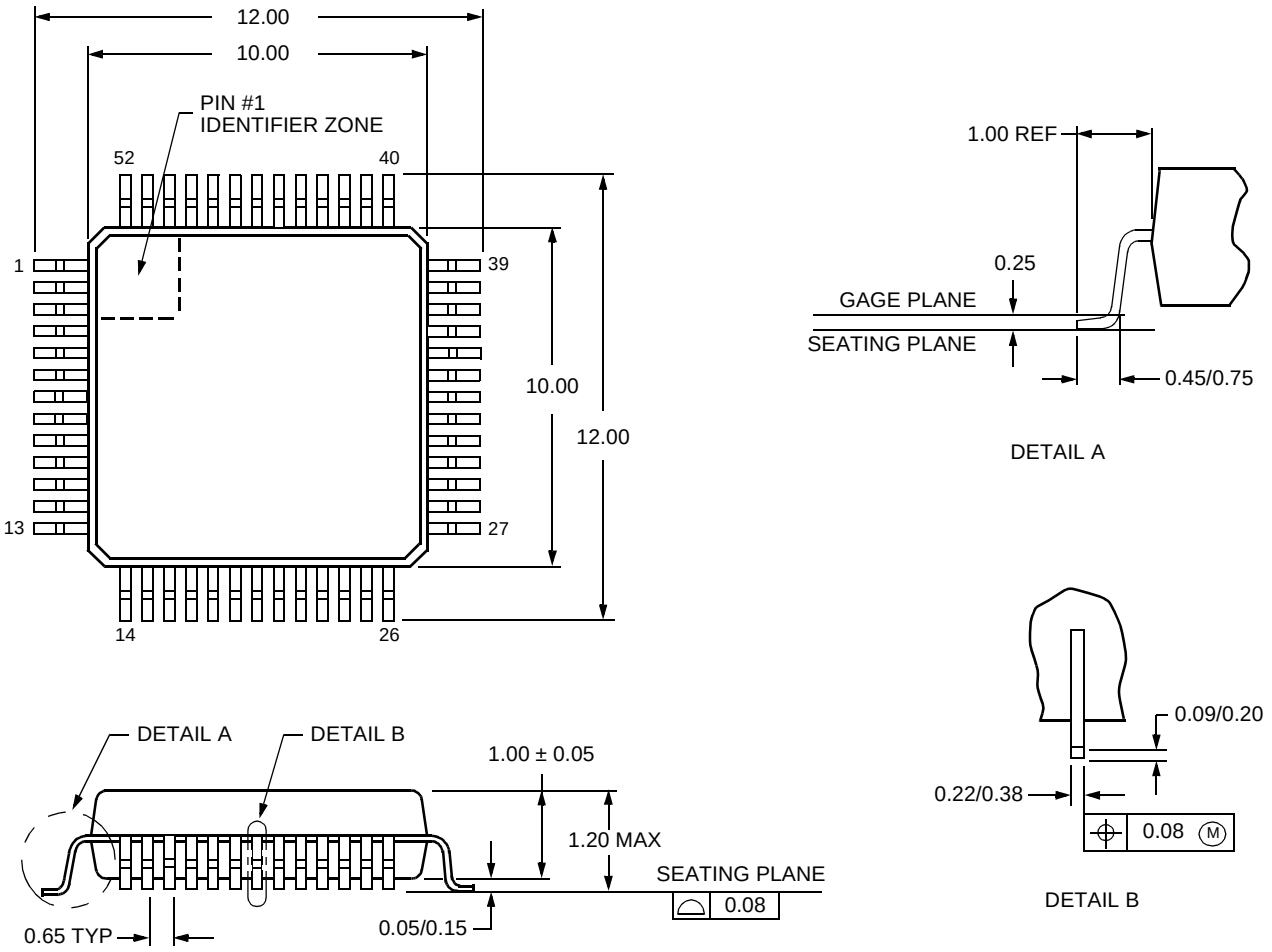


Figure 3. LVTTL ac Test Load

Outline Diagram

52-pin TQFPT package outline. All dimensions are in millimeters.



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