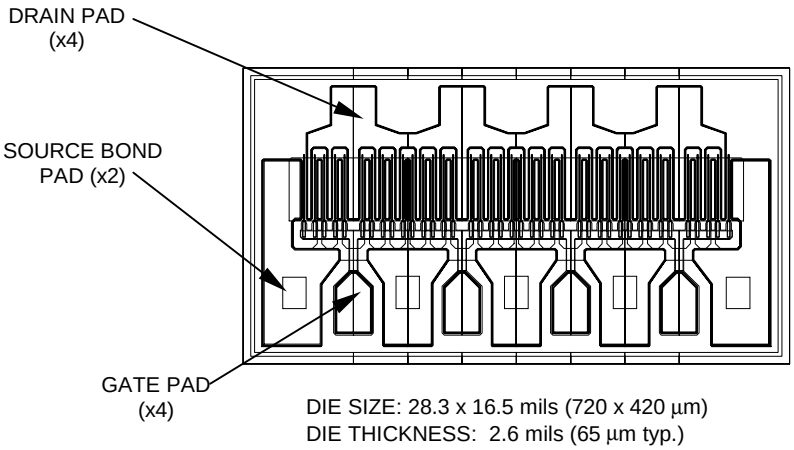
Filtronic LP3000/LPV3000

Solid State

2W Power PHEMT

FEATURES

- +33.5 dBm Typical Power at 18 GHz
- 7 dB Typical Power Gain at 18 GHz
- +30.5 dBm at 3.3V Battery Voltage
- Low Intermodulation Distortion
- 45% Power-Added-Efficiency at 18 GHz



DIE SIZE: 28.3 x 16.5 mils (720 x 420 µm)
DIE THICKNESS: 2.6 mils (65 µm typ.)
BONDING PADS: 1.9 x 2.4 mils (50 x 60 µm typ.)

DESCRIPTION AND APPLICATIONS

The LP3000 is an Aluminum Gallium Arsenide / Indium Gallium Arsenide (AlGaAs/InGaAs) Pseudomorphic High Electron Mobility Transistor (PHEMT), utilizing an Electron-Beam direct-write 0.25 µm by 3000 µm Schottky barrier gate. The recessed "mushroom" gate structure minimizes parasitic gate-source and gate resistances. The epitaxial structure and processing have been optimized for reliable high-power applications. The LP3000 also features Si_3N_4 passivation and is available with plated source via-holes (LPV 3000) as an option for improved high-frequency performance. Also available in a ceramic flanged package (P100) and ball grid array package.

Typical applications include commercial and military high-performance power amplifiers, including SATCOM uplink transmitters, PCS/Cellular low-voltage high-efficiency output amplifiers, and medium-haul digital radio transmitters. The LPV 3000/LP 3000 may be procured in a variety of grades, depending upon specific user requirements. Standard lot screening is patterned after MIL-STD-19500, JANC grade. Space-level screening to FSS JANS grade is also available.

PERFORMANCE SPECIFICATIONS (T_A = 25°C)

SYMBOLS	PARAMETERS		MIN	TYP	MAX	UNITS
I_{DSS}	Saturated Drain-Source Current V_{DS} = 2V V_{GS} = 0V		800	1060	1100	mA
P_{1dB}	Output Power at 1dB Gain Compression V_{DS} = 8.0V, I_{DS} = 50% I_{DSS} (LP. LPV)	*f* = 18 GHz	33.0	33.5		dBm
G_{1dB}	Power Gain at 1dB Gain Compression V_{DS} = 8.0V, I_{DS} = 50% I_{DSS} (LP) V_{DS} = 8.0V, I_{DS} = 50% I_{DSS} (LPV)	*f* = 18 GHz *f* = 18 GHz	4.0 6.0	6.0 7.0		dB dB
η_{ADD}	Power-Added Efficiency (typ. for Class A operation)			45		%
I_{MAX}	Maximum Drain-Source Current	V_{DS} = 2V V_{GS} = +1V		1700		mA
G_M	Transconductance	V_{DS} = 2V V_{GS} = 0V	725	900		mS
V_P	Pinch-Off Voltage	V_{DS} = 2V I_{DS} = 10mA	-0.25	-1.2	-2.0	V
I_{GSO}	Gate-Source Leakage Current	V_{GS} = -5V		15	125	µA
BV_{GS}	Gate-Source Breakdown Voltage	I_{GS} = 15mA	-12	-15		V
BV_{GD}	Gate-Drain Breakdown Voltage	I_{GD} = 15mA	-12	-16		V
Θ_J	Thermal Resistivity			20		°C/W

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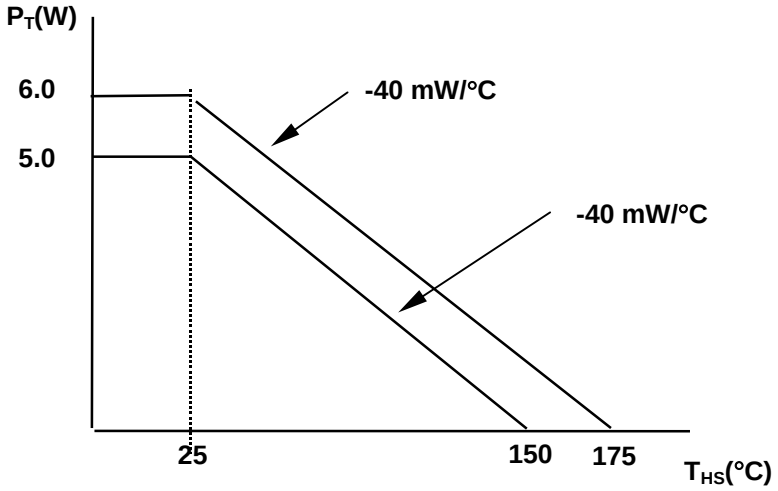
ABSOLUTE MAXIMUM RATINGS (25°C)		
SYMBOL	**PARAMETER**	**RATING[1]**
V_{DS}	Drain-Source Voltage	12V
V_{GS}	Gate-Source Voltage	-5V
I_{DS}	Drain-Source Current	2 x I_{DSS}
I_G	Gate Current	120 mA
P_{IN}	RF Input Power	1.2 W
T_{CH}	Channel Temperature	175°C
T_{STG}	Storage Temperature	-65/175°C
P_T	Power Dissipation	6.0W[3,4]

RECOMMENDED CONTINUOUS OPERATING LIMITS		
SYMBOL	**PARAMETER**	**RATING[2]**
V_{DS}	Drain-Source Voltage	8V
V_{GS}	Gate-Source Voltage	-1V
I_{DS}	Drain-Source Current	0.8 x I_{DSS}
I_G	Gate Current	40 mA
P_{IN}	RF Input Power	600 mW
T_{CH}	Channel Temperature	150°C
T_{STG}	Storage Temperature	-20/50°C
P_T	Power Dissipation	5.0 W[3,4]
G_{XdB}	Gain Compression	8 dB

NOTES:

1. Operating conditions that exceed the Absolute Maximum Ratings could result in permanent damage to the device.
2. Recommended Continuous Operating Limits should be observed for reliable device operation.
3. Power Dissipation defined as: $P_T \equiv (P_{DC} + P_{IN}) - P_{OUT}$, where: P_{DC} = DC bias power, P_{OUT} = RF output power, and P_{IN} = RF input power.
4. Power Dissipation to be de-rated as follows:
5. Specifications subject to change without notice.



Example #1 :
V_{DS} = 8V, I_{DS} = 535 mA
$P_{IN} = P_{OUT}$ = 0 dBm (quiescent condition):
$P_T = P_{DC}$ = 4.28W
Max. continuous T_{HS} = 25°C

Example #2:
V_{DS} = 8V, I_{DS} = 535 mA
P_{IN} = 26.5 dBm P_{OUT} = 33.5 dBm
P_T = (4.28+0.45) - 2.24 = 2.49W
Max. continuous T_{HS} = 88°C

HANDLING PRECAUTIONS:

PHEMT chips should be stored in a dry nitrogen environment until assembly. Care should be exercised during handling to avoid damage to the devices. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 1A (0-500V), and further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

ASSEMBLY INSTRUCTIONS:

The recommended die attach is gold/tin eutectic solder under a nitrogen atmosphere. Stage temperature should be 280-290°C; maximum time at temperature is 1 min. The recommended wire bond method is thermo-compression wedge bonding with 0.7 or 1.0 mil (0.018 or 0.025 mm) gold wire. Stage temperature should be 250-260°C.

APPLICATIONS NOTES AND DESIGN DATA:

Applications Notes are available from your local FSS Sales Representative, or directly from the factory. Complete design data, including S-parameters, Noise data, and Large-Signal models, is available on 3.5" diskette, or may be down-loaded from our Web Page.

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