Data Sheet
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microelectronics group

Lucent Technologies
Bell Labs Innovations

Voltage Feedback Op Amp (VF-OpAmp)

Features

- 55 dB dc gain
- 30 mA current drive
- Less than 1 V head/floor room
- 300 V/µs slew rate
- Capacitive load stable
- 40 kΩ input impedance
- 300 MHz unity gain bandwidth
- 7 mA biasing current
- 5.6 nV/$\sqrt{\text{Hz}}$ equivalent input noise

Introduction

In custom analog integrated circuit (IC) designs, there are many occasions where a general-purpose voltage feedback operational amplifier (VF-OpAmp) is useful. If the application calls for differential inputs, high input impedance, low output impedance, common-mode isolation, and current-drive capability, the VF-OpAmp provides a basic topology for achieving these requirements.

Very often, the most cost-effective designs employ the simplest circuits (fewest devices) that meet the design specifications. The VF-OpAmp has been chosen because of its simplicity. If its performance is satisfactory for a given application, it can be used as presented*; if not, numerous suggestions have been included for improving the performance. These suggestions can be used as needed, albeit at a cost of requiring additional devices and/or power.

A VF-OpAmp circuit, composed of an input stage, a folded cascode common-base difference-integrating stage, and a low output impedance driving stage is illustrated in Figure 1. The circuit takes advantage of the complementary nature of the CBIC process to achieve controlled and symmetrical behavior. The input stage converts the differential input voltage to differential current, the folded cascode difference-integrating stage subtracts and integrates the differential currents, and the output stage buffers the integrated current voltage for driving low impedance loads.

The VF-OpAmp is intended to be biased with the voltage and current reference (VCR) circuit macrocell. If the resistors in the op amp are selected to be of the same type as those of the VCR, the voltages across the resistors† will be proportional to the bandgap voltage (VBG). The op amp may also be biased with an external current source, albeit with degraded temperature behavior.

Further, since transistors typically have higher gains at elevated temperatures, uniform performance over temperature is best achieved by biasing the transistors with negative temperature coefficient current sources. Using negative temperature coefficient current sources, for biasing, also helps to ensure thermal stability‡ by lowering the dissipated power on the IC as the temperature increases.

In the following Description section, circuits for, and simulation performance of, the VF-OpAmp are presented to demonstrate the behavior for dc, ac, and transient behavior. The Performance Improvements section provides numerous ways to modify the VF-OpAmp to change specifications and/or improve performance. Further, this macrocell has been fabricated using the Lucent Technologies Microelectronics Group ALA110 CBIC-V2 linear array for evaluation.

* All materials presented are exclusively for reference.
† Since devices of the same type usually match each other within 1%, while absolute values vary by more than 20% in most integrated-circuit fabrication processes, it is most often advantageous to utilize circuits where accuracy is controlled by device matching rather than by the absolute value of the devices.
‡ This is especially important since most SPICE class circuit simulators cannot simulate thermal stability.

Description

An elementary voltage feedback operational amplifier circuit is illustrated in Figure 1. The circuit is composed of three parts: a differential input stage, a folded cascode difference-integrating stage, and a low output impedance unity gain driving buffer stage.

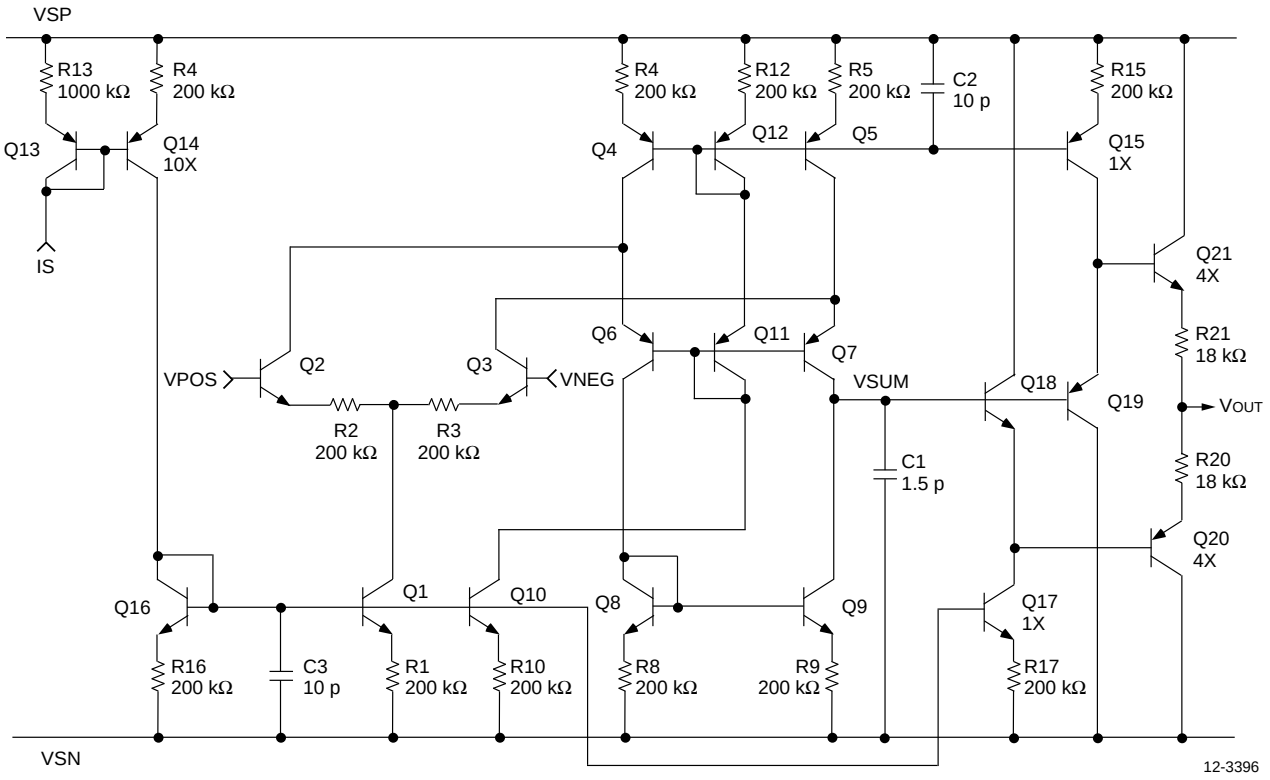

Figure 1. Voltage Feedback Operational Amplifier (VF-OpAmp) Schematic

Description (continued)

Differential Input Stage

The differential input stage is composed of transistors Q2 and Q3, which are biased by the current (I1) of transistor Q1. The difference current I2 – I3 is:

$$I2 - I3 = I1 \times \tanh\frac{VPOS - VNEG}{2 \times VT + R \times I1}$$

where R = R2 = R3. For small differential voltages and R x I1 >> 2 x VT, the differential current simplifies to:

$$I2 - I3 = \frac{VPOS - VNEG}{R}$$

Hence, the input stage behaves as a transconductance (G = 1/R) amplifier.

Folded Cascode Difference Integrating Stage

The second stage is composed of the emitters of Q6 and Q7 as inputs, Q8 and Q9 form a current mirror for the positive current, the collector currents of Q4 and Q5 bias the common-base stage, the base-collector voltage of Q11 sets the operating voltage of Q6 and Q7, and C1 integrates the differential collector currents of Q7 and Q9. The biasing currents of Q1, Q4, and Q5 are set at the same values to center the operating range. Within the voltage and current operating range of VSUM, assuming ideal devices and an infinite impedance in parallel with C1, the VSUM voltage is:

$$VSUM = \frac{1}{C}\left(\int_{t0}^{t} \frac{VPOS - VNEG}{R} dt\right)$$

For an ideal op amp, VSUM would be at 0 V if VPOS – VNEG = 0. Because of the finite impedance in parallel with C1, nonideal devices, and device mismatch, VPOS – VNEG is usually required to be offset for VSUM to equal V (i.e., offset voltage).

The rate at which VSUM varies during operation depends on the size of the differential current applied to C1. The maximum rate at which VSUM can vary (slew rate) is limited by the collector current of Q1 and the value of C1*.

* The parasitic capacitances associated with the VSUM node can often be larger than the value of C1.

A Low Output Impedance Unity Gain Driving Stage

The function of the VF-OpAmp (i.e., differential input voltage to output voltage) is essentially complete at the VSUM node. Since, in most applications, it is necessary to drive small impedances, a low output impedance driver output buffer is usually required.

The driver/output buffer stage presented in Figure 1 has a wide bandwidth (approximately the unity gain, Ft, of the transistors), an output-to-input impedance reduction of βnpn x βpnp, an output voltage swing to within 1 V of both voltage supply rails, and a current-drive capability of I15 x βnpn or I17 x βpnp.

The resistors R21 and R20 maintain the biasing current in Q21 and Q20 at the same values as Q18 and Q19 for dc operating point, and also improve the stability margin when driving capacitive loads.

Simulated Performance

dc Transfer Characteristics

Figure 2 illustrates the dc characteristics of the VF-OpAmp where V_{IN} = VPOS – VNEG. The dc gain at V_{IN} = 0 is the slope of the curve, which is approximately:

$$\frac{8\ V}{10\ mV} = 800\ (58\ dB).$$

Also, the maximum voltage swing extends slightly above 4 V and below –4 V, when operating with ±5 V supplies.

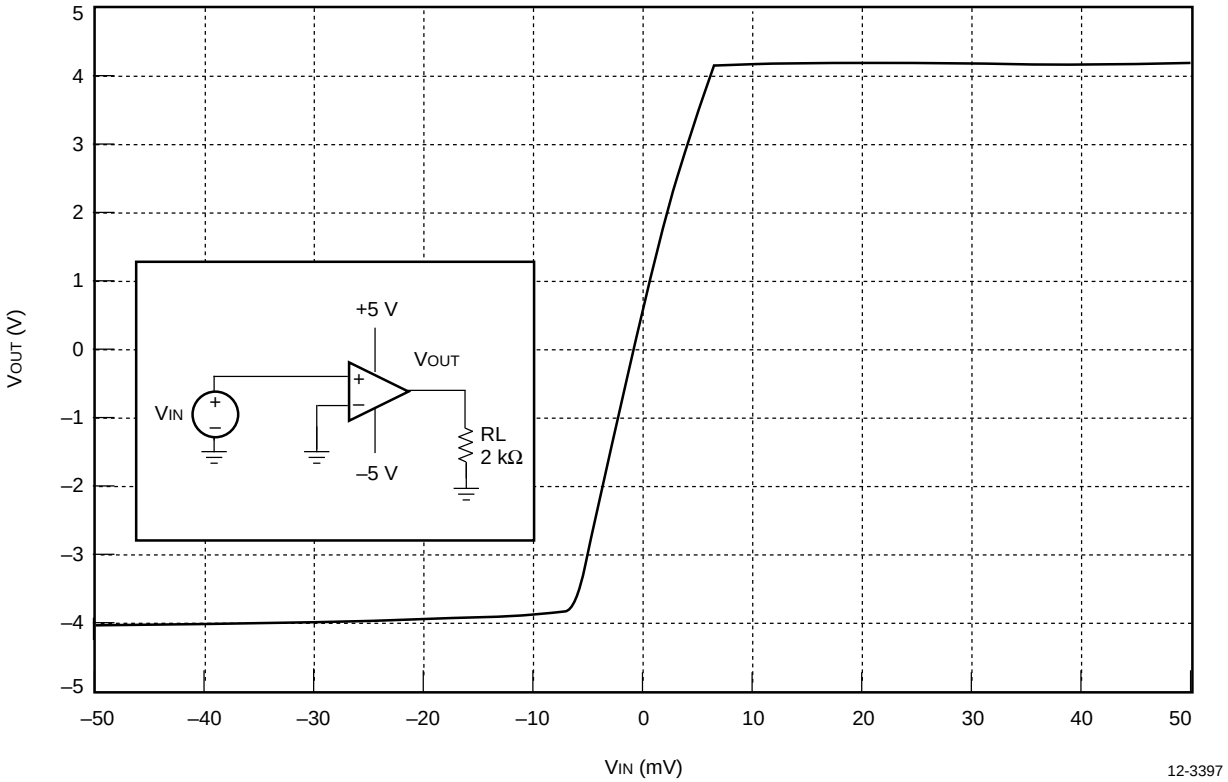

Figure 2. Simulated dc Transfer Characteristic for the VF-OpAmp

Simulated Performance (continued)

ac Gain and Phase

Figure 3 illustrates the small-signal (ac) open-loop gain and phase of the VF-OpAmp driving a 2k load*.

The ac gain at the low frequencies (left side) are about 58 dB, the same as the dc gain of Figure 2. The dc gain is set by the ratio of the resistance in parallel with C1 with R (R2, R3 in Figure 1). Since R approximately equals 200 Ω, and the gain is about 1000, the parallel resistance with C1 is approximately 100k (i.e., input impedance of output buffer in parallel with the output impedance of Q7 and Q4).

The ac unity gain occurs at approximately 200 MHz. The larger the phase and gain margin of an op amp, the greater the stability. Figure 3 shows a phase margin of 80 degrees and a gain margin of 30 dB. The bandwidth of the VF-OpAmp can be increased by improving the dc gain or reducing the value of the compensating capacitor C1. This will result in a reduction of phase and gain margins†.

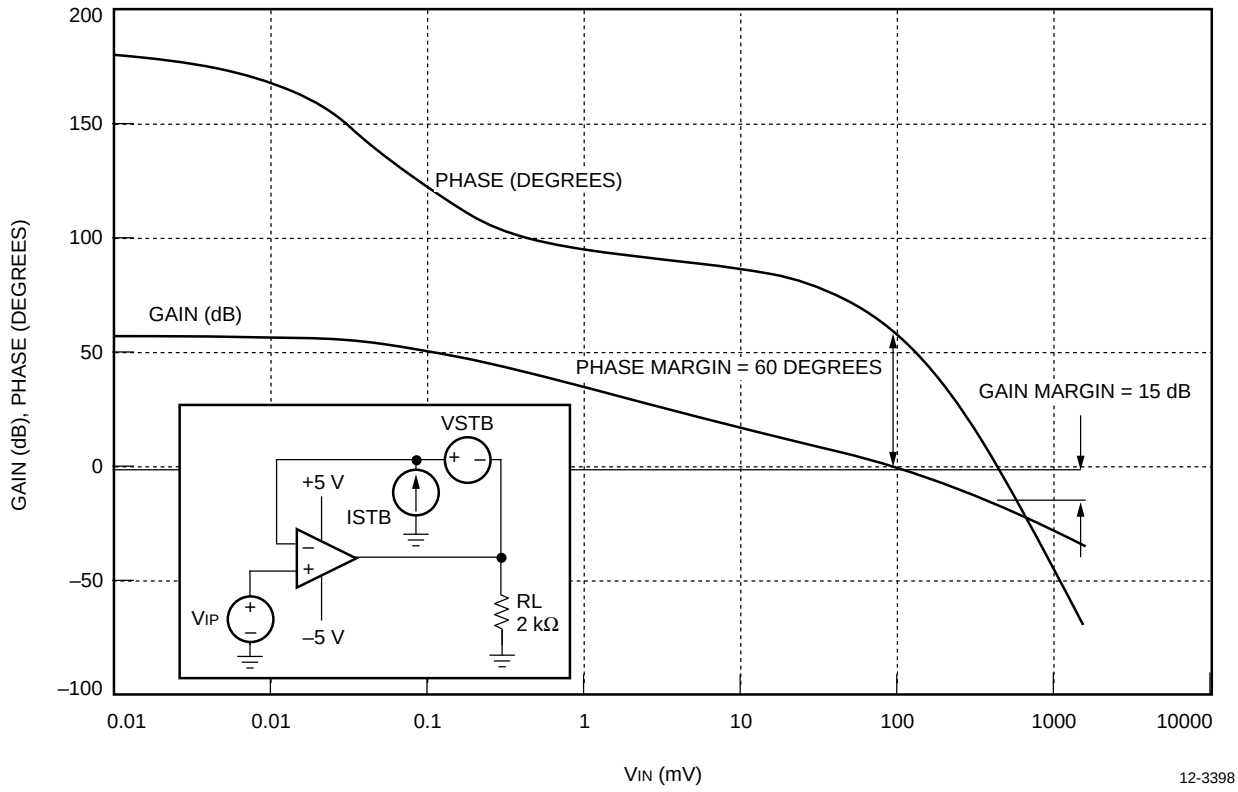

Figure 3. Simulated Loop Gain and Phase (Effectively Open Loop) for the VF-OpAmp

* The gain and phase simulations are obtained in a unity gain close-loop configuration, which is equivalent to an open-loop gain and phase measurement.
† Usually, 45 degrees of phase margin and 6 dB of gain margin is considered adequate.

Simulated Performance (continued)

Unity Gain Bandwidth

The unity gain characteristic of the VF-OpAmp is illustrated in Figure 4. The bandwidth is approximately 200 MHz, with about 0.2 dB of peaking at 150 MHz. The peak voltage occurs at the frequency where the open-loop gain is 1. This can be adjusted by changing the dc gain, or the compensation capacitor C1.

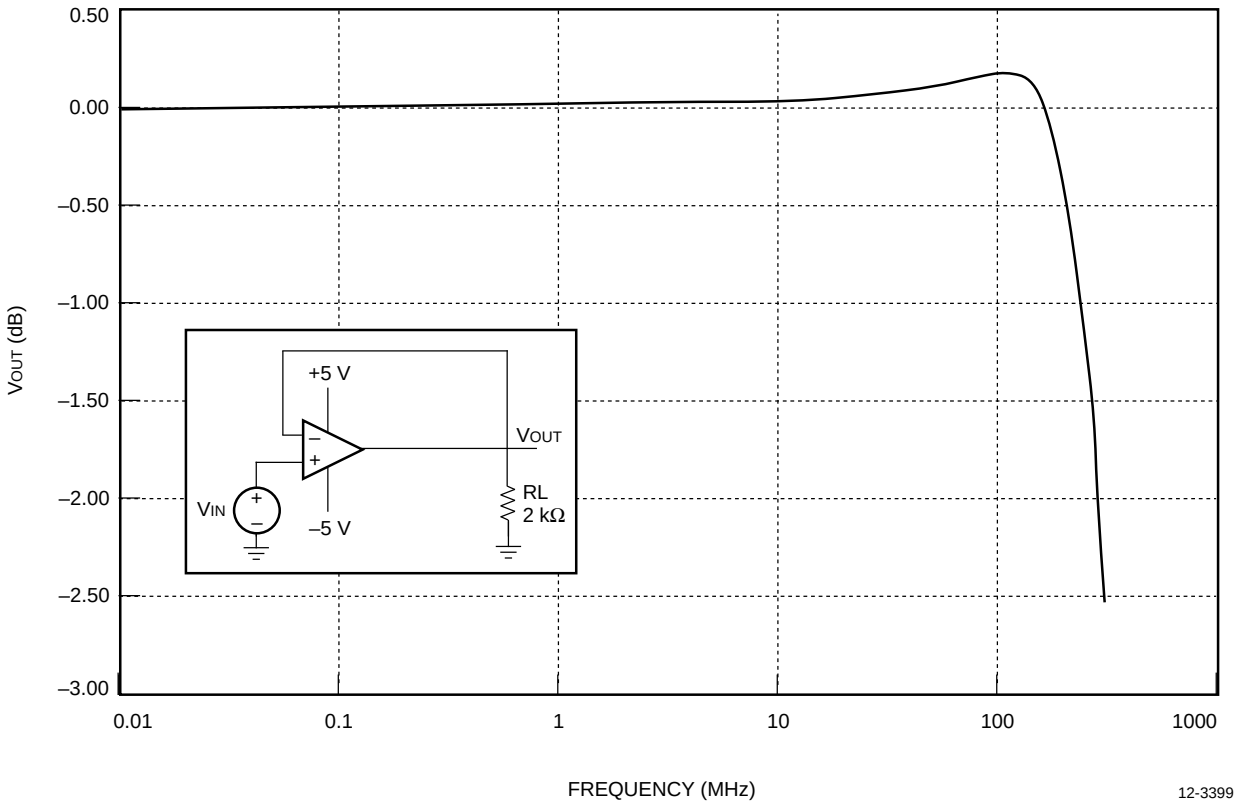

Figure 4. Simulated ac Unity Gain of the VF-OpAmp

Simulated Performance (continued)

Slew Rate Limit

The slew rate limit is illustrated in Figure 5. Two 100 MHz waveforms are passed through the VF-OpAmp, one at 0.2 V and the other at 1.0 V. The 0.2 V waveform is not slew rate limited, and the 1.0 V sine wave is seen to slew limit at about 1 V divided by 4 ns (250 V/µs). Since the slew rate is the ratio of the difference current and C1, increasing the current or reducing C1 will increase the slew rate.

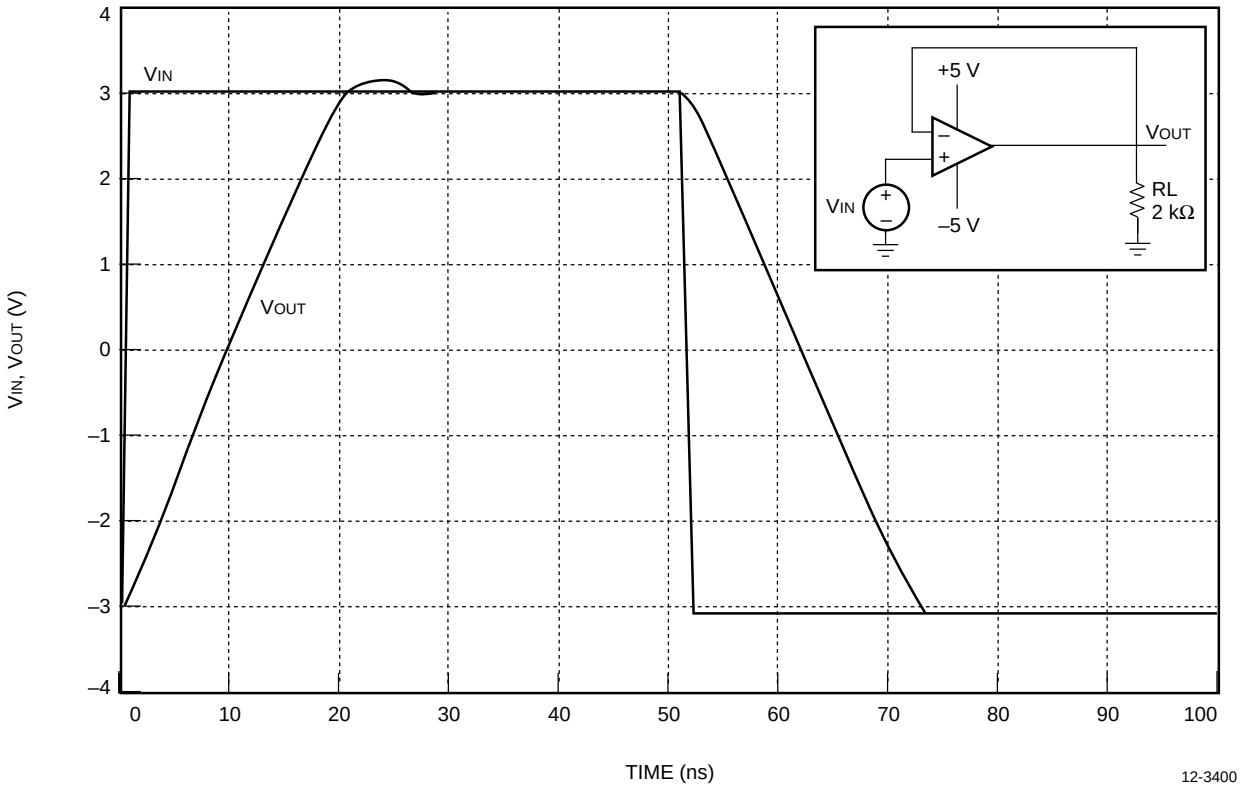

Figure 5. Simulated Transient Response of the VF-OpAmp Illustrating the Slew Rate Limit

Simulated Performance (continued)

Input Impedance

The input impedance as a function of frequency of the VF-OpAmp is illustrated in Figure 6. The input impedance is about 50 kΩ up to 10 MHz and then drops off at 20 dB per decade, reaching 1 kΩ at 1 GHz.

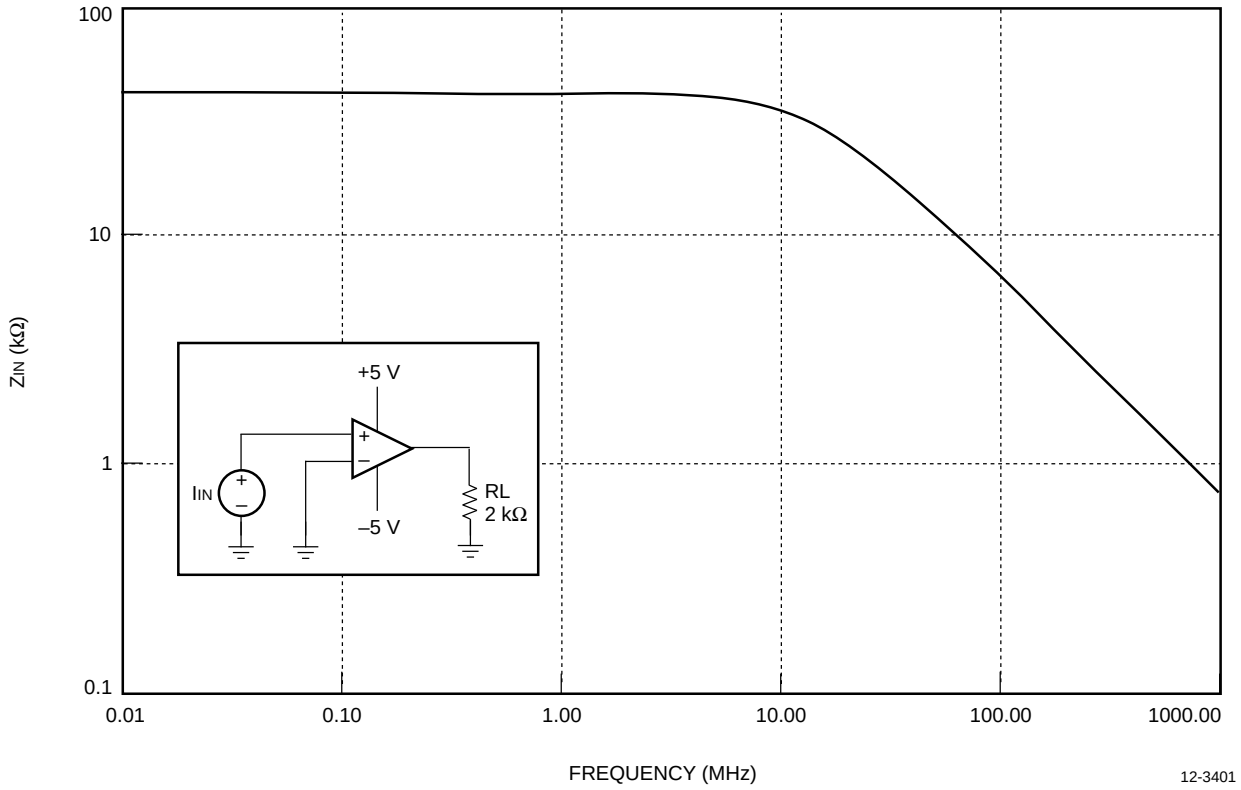

Figure 6. Simulated Input Impedance for the VF-OpAmp

Performance Improvements

Power

The dc power dissipation is related to the dc bias current times the power supply voltage, plus the drive current times the voltage drop across the IC. The ac power consumption is the power consumption plus the RMS power on the IC. The biasing current is set by the biasing circuits in the VCR macrocell. The VCR cell has been designed to compensate for process and temperature variations. The temperature variation is minimized by the use of a bandgap reference circuit, and the process variation is minimized by avoiding tolerance that depend on absolute device values.

Varying the value of the biasing current in the VF-OpAmp changes the dc power proportionally. Changing the biasing current affects the bandwidth, the slew rate, and the current-drive capability.

dc Gain

The dc gain is controlled by R (or I1 if R is small) and the impedance in parallel with C1. Hence, increasing I1, and/or reducing R, and/or increasing the impedance in parallel with C1, will increase the dc gain.

Bandwidth

The bandwidth is controlled by C1 and the resistance in parallel with C1. Increasing R x C1 lowers the bandwidth by lowering the corner frequency of the dominant pole. This also affects the open-loop unity gain. Changing the dc gain by varying R (or I1 if R is small) changes the open-loop unity gain but does not change the bandwidth.

Slew Rate

The slew rate is controlled by the difference current at the summing node and C1. Increasing the current and reducing C1 increases the slew rate. Decreasing C1 also has the adverse effect of reducing the stability of the op amp. Increasing the current improves the stability but increases the dissipated power.

Stability

Increasing C1 increases the stability but reduces the bandwidth and the slew rate. Increasing the current also increases the stability to a point, but at the expense of increasing dissipated power.

Input Impedance

The input impedance can be increased by lowering the biasing current. This also lowers the dc gain, the bandwidth, and the slew rate. An alternate approach to increasing the input impedance is to use an input-biasing current-cancellation circuit.

Current Drive

The output current drive can be increased by increasing the biasing current. This will also increase the dissipated power. An alternative is to use Darlingtons in the output stage. This will provide an extra stage of current gain, but will reduce the head room by one VBE.

Input-Referred Noise

The input-referred noise is primarily due to the thermal noise of the base resistance and the shot noise of the junction currents in the input transistors Q2 and Q3. To minimize the noise, the input devices are made as large as possible to obtain the minimum base resistance. Since large devices have more capacitances associated with them, it requires more junction current to retain the speed. An optimal point for minimum noise operation is where the base resistance thermal noise equals the junction shot noise.

Electrical Characteristics for the VF-OpAmp

Conditions: T_J = 25 °C, R_L = 2 kΩ, VSP = +5 V, VSN = –5 V

Table 1. dc Characteristics

Name	Conditions	Typical	Unit
Voltage Supply Range	—	±1 to ±5	V
Supply Current Draw	V_{IN} = 0.85 mV	6.3	mA

Table 2. dc Performance

Name	Conditions	Typical Value	Unit
Input Bias Current	V_{IN} = 0.85 mV	5.7	µA
Input Impedance	—	40	kΩ
Input Offset Voltage	—	0.85	mV
Output Voltage Swing (head/floor room)	VSP – V_{OUT}, V_{OUT} – VSN	1, 1	V
Common-mode Range (head/floor room)	VSP – V_{IN}, V_{IN} – VSN	1, 1	V
Output Current Drive	—	30	mA
dc Gain	—	56	dB

Table 3. ac Performance

Name	Conditions	Typical Value	Unit
Open-loop Unity Gain Frequency	—	200	MHz
Open-loop Bandwidth	—	350	kHz
Closed-loop Unity Gain Bandwidth	Unity Gain	250	MHz

Table 4. Dynamic Performance

Name	Conditions	Typical Value	Unit
Slew Rate	Unity Gain	300	V/µs
Noise Voltage at Input	V_{IN} = 0.85 mV, Open Loop	5.6	$nV/\sqrt{Hz}$

Notes

For additional information, contact your Microelectronics Group Account Manager or the following:

INTERNET: **http://www.lucent.com/micro**

U.S.A.: Microelectronics Group, Lucent Technologies Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18103
1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106), e-mail **docmaster@micro.lucent.com**

ASIA PACIFIC: Microelectronics Group, Lucent Technologies Singapore Pte. Ltd., 77 Science Park Drive, #03-18 Cintech III, Singapore 118256
Tel. (65) 778 8833, FAX (65) 777 7495

JAPAN: Microelectronics Group, Lucent Technologies Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan
Tel. (81) 3 5421 1600, FAX (81) 3 5421 1700

For data requests in Europe:

MICROELECTRONICS GROUP DATALINE: **Tel. (44) 1734 324 299**, FAX (44) 1734 328 148

For technical inquiries in Europe:

CENTRAL EUROPE: **(49) 89 95086 0** (Munich), NORTHERN EUROPE: **(44) 1344 865 900** (Bracknell UK),
FRANCE: **(33) 1 41 45 77 00** (Paris), SOUTHERN EUROPE: **(39) 2 6601 1800** (Milan) or **(34) 1 807 1700** (Madrid)

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