Data Sheet
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microelectronics group

Lucent Technologies
Bell Labs Innovations

Current Feedback Op Amp (CF-OpAmp)

Features

- 61 dB dc gain
- 6 mA current drive
- Less than 1 V head/floor room
- 650 V/µs slew rate
- 280 kΩ input impedance
- 450 MHz unity gain bandwidth
- Low power (1.5 mA biasing current)
- 2 nV/$\sqrt{\text{Hz}}$ equivalent input noise

Introduction

The primary advantage of current feedback operational amplifiers (CF-OpAmps), over other types of op amps, is their ability to achieve fast slew rates at small, quiescent power levels. This is especially advantageous for pulse applications where most of the power is required during the pulse edges. The way CF-OpAmps achieve fast slew rates at small, quiescent power levels is by generating the internal currents required for fast slew rates dynamically through the negative input terminal.

The primary disadvantage of this approach is that the input impedance is very low for the negative input terminal, which makes current feedback op amps poor inverting amplifiers. Conversely, the input impedance of the positive input terminal is much higher; hence, current feedback op amps are mostly used as noninverting amplifiers.

For noninverting applications that require low power, fast slew rate, low output impedance, and current-drive capability, the CF-OpAmp presented here provides a basic topology for achieving these requirements.

Very often, the most cost-effective designs employ the simplest circuits (fewest devices) that meet the design specifications. The CF-OpAmp has been chosen because of its simplicity. If its performance is satisfactory for a given application, it can be used as presented*; if not, numerous suggestions have been included for improving the performance. These suggestions can be used as needed, albeit at a cost of requiring additional devices.

A CF-OpAmp circuit, composed of an input stage, a differential current drive stage, and a low output impedance driving stage, is illustrated in Figure 1. The circuit takes advantage of the complementary nature of the CBIC process to achieve controlled and symmetrical behavior. The input stage generates a current that is equal to the current in the negative input terminal. The differential current drive stage reflects the current from the negative input to the summing node and to the output stage biasing current sources. The output stage is a wideband unity gain buffer with a low output impedance.

The CF-OpAmp is intended to be biased with the voltage and current reference (VCR) circuit macrocell. If the resistors in the CF-OpAmp are selected to be of the same type as those of the VCR, the voltages across the resistors† will be proportional to the bandgap voltage (VBG). The CF-OpAmp may also be biased with an external current source.

Since transistors typically have higher gains at elevated temperatures, uniform performance over temperature is best achieved by biasing the transistors with negative temperature coefficient current sources. Using negative temperature coefficient current sources for biasing also helps ensure thermal stability‡ by lowering the dissipated power on the IC as the temperature increases.

* Since devices of the same type usually match each other within 1%, while absolute values vary by more than 20% in most integrated-circuit fabrication processes, it is most often advantageous to utilize circuits where accuracy is controlled by device matching rather than by the absolute value of the devices.
† All materials presented are exclusively for reference.
‡ This is especially important since most SPICE class circuit simulators cannot simulate thermal stability.

Introduction (continued)

In the following Description section, the dc, ac, and transient capabilities for the current feedback operational amplifier are presented. The Performance Improvements section provides numerous ways to modify the CF-OpAmp circuit to achieve improved performance. Further, this macrocell is fabricated using the Lucent Technologies Microelectronics Group ALA110 CBIC-V2 linear array for evaluation.

Description

An elementary current feedback operational amplifier circuit is illustrated in Figure 1. The circuit is composed of three parts: a differential input stage, a differential current drive current mirror stage, and a low output impedance unity gain driving stage.

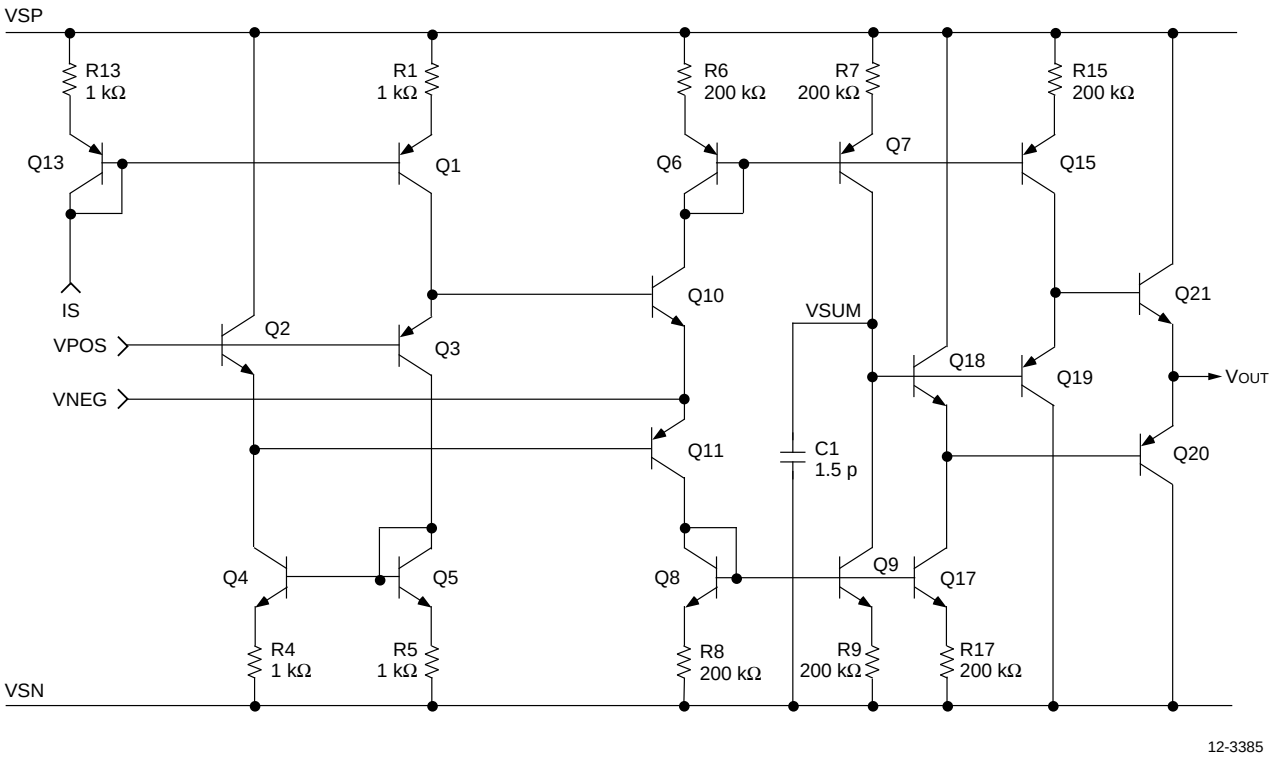

Figure 1. Current Feedback Operational Amplifier (CF-OpAmp) Schematic

Description (continued)

Differential Input Stage

The differential input stage is composed of transistors Q2 and Q3, which are biased by the currents of transistors Q1(I1) and Q4(I4), and Q10 and Q11, which are biased by transistors Q2 and Q3. The ratio of the current in the negative and positive terminal is:

$$\frac{INEG}{IPOS} = \beta npn \beta pnp$$

Operating in the noninverting mode with a resistor, R, connected from the negative terminal to gnd, the differential current at the collector of Q10 and Q11 is:

$$I10 - I11 = \frac{VNEG}{R}$$

Hence, the input stage behaves as a transconductance amplifier G = 1/R. The voltage from the positive input terminal to ground has been converted to a differential output current (I10—I11).

Differential Current Drive Stage

The second stage is composed of Q6, Q7, Q8, Q9, Q15, and Q17. Assuming perfect devices and infinite impedance in parallel with C1, the VSUM voltage is:

$$VSUM = \frac{1}{C}\left(\int_{t0}^{t} \frac{VNEG}{R}\right) dt$$

For an ideal CF-OpAmp, VSUM would equal 0 V if INEG = 0. Because of finite impedance in parallel with C1, nonideal devices, and device mismatch, INEG usually requires VPOS – VNEG to be offset for VSUM to equal 0 V (i.e., offset voltage).

The rate at which the VSUM node changes value depends on the size of the differential current applied to C1. The maximum rate at which VSUM can vary (slew rate) is limited by the collector currents of Q7 and Q9, and the value of C1*. The primary advantage of CF-OpAmp is that the collector currents of Q7 an Q9 become larger as the amplifier input slews faster. Unlike the VF-OpAmp, the biasing current of Q15 and Q17 also increases with speed, which provides more current drive. This is especially beneficial for capacitive loads.

* The parasitic capacitances associated with the VSUM node can often be larger than the value of C1.

A Low Output Impedance Unity Gain Driver Buffer Stage

The function of the CF-OpAmp is essentially complete at the VSUM node. That is, the input voltage has been converted to a single output voltage. Since, in many applications, it is necessary to drive small impedances, the addition of a low output impedance driver is desirable. Note the similarity of the input and output stages.

The driver/output buffer stage presented in Figure 1 has a wide bandwidth (approximately the unity gain, Ft, of the transistors), an output-to-input impedance reduction of βnpn x βpnp, an output voltage swing to within 1 V of both voltage supply rails, and a current-drive capability of I15 x βnpn or I17 x βpnp.

Simulated Performance

dc Transfer Characteristics

Figure 2 illustrates the dc characteristics of the CF-OpAmp, where V_{IN} = VPOS – VNEG. The dc gain at V_{IN} = 0 is the slope of the curve, which is approximately:

$\frac{8\ V}{7.9\ mV}$ = 1034 (61 dB). Also, the maximum voltage swing extends slightly above 4 V and below –4 V.

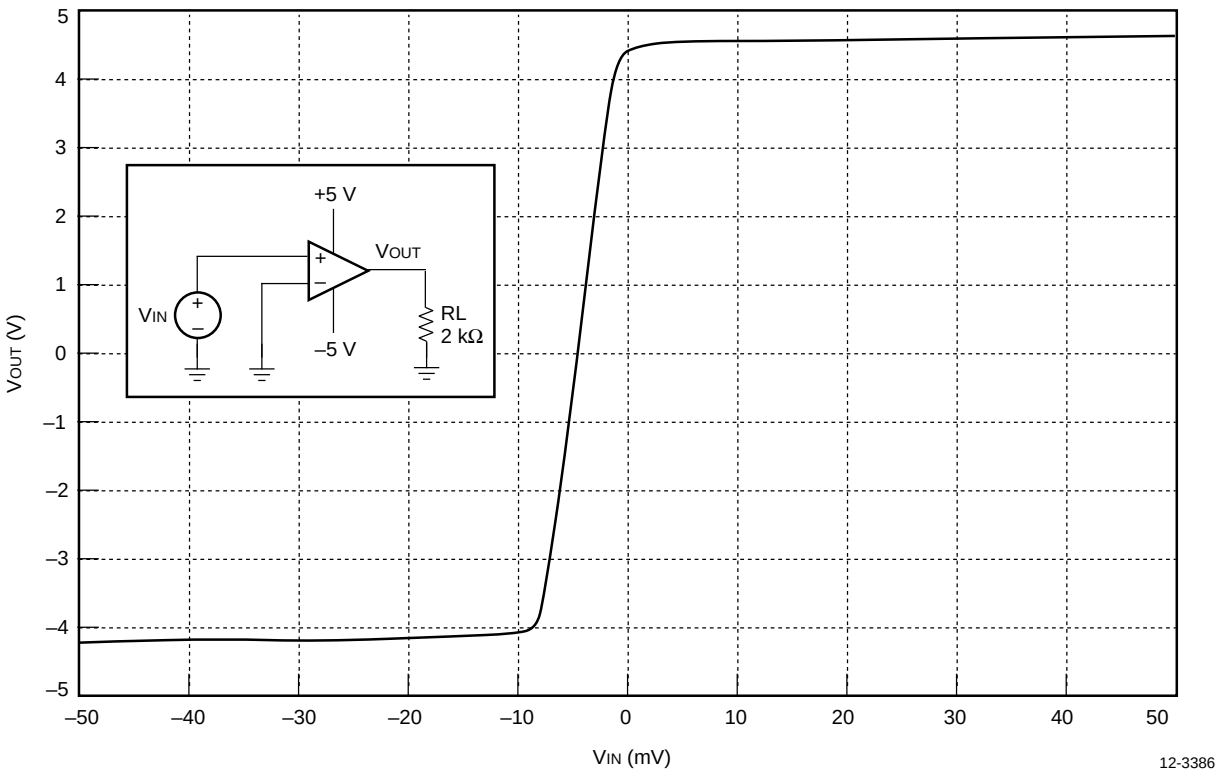

Figure 2. Simulated dc Transfer Characteristic for the CF-OpAmp

Simulated Performance (continued)

ac Gain and Phase

Figure 3 illustrates the ac gain and phase of the VF-OpAmp driving a 2k load*.

The ac gain at the low frequencies (left side of Figure 3), plus the 6 dB from the gain of two feedback loops is about 61 dB, the same as the dc gain in Figure 2.

The ac unity gain occurs at approximately 300 MHz. The larger the phase and gain margin of an op amp, the greater the stability. Figure 3 shows a phase margin of 48 degrees and a gain margin of 17 dB. The bandwidth of the CF-OpAmp can be increased by improving the dc gain or reducing the value of the compensating capacitor C1. This will result in a reduction of phase and gain margin†.

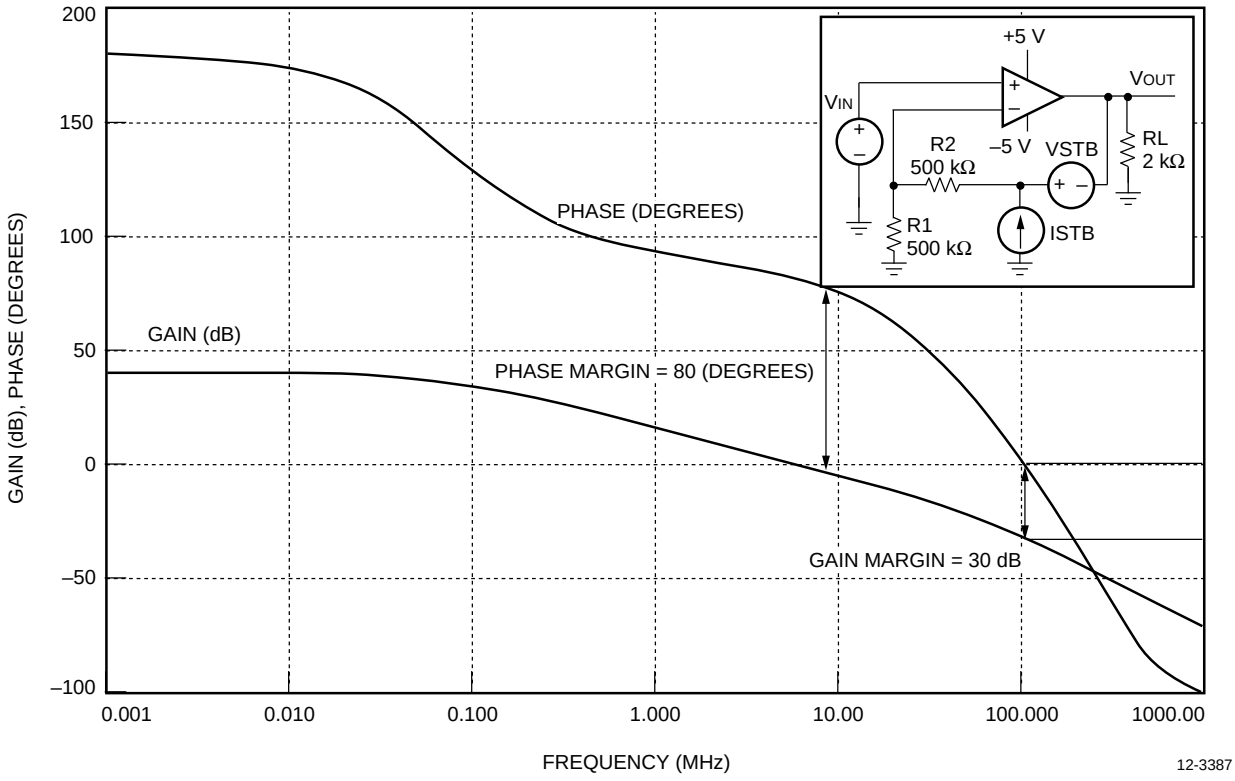

Figure 3. Simulated Loop Gain and Phase (Effectively Open Loop) for the CF-OpAmp

* The gain and phase simulations are obtained in a unity gain close-loop configuration, which is equivalent to an open-loop gain and phase measurement.

† Usually, 45 degrees of phase margin and 6 dB of gain margin is considered adequate.

Simulated Performance (continued)

Unity Gain Bandwidth

The unity gain characteristic of the CF-OpAmp is illustrated in Figure 4. The bandwidth is approximately 450 MHz, with about 0.2 dB of peaking at 200 MHz. The peak voltage occurs at the frequency where the open-loop gain is 1. This can be adjusted by changing the dc gain or the compensation capacitor C1.

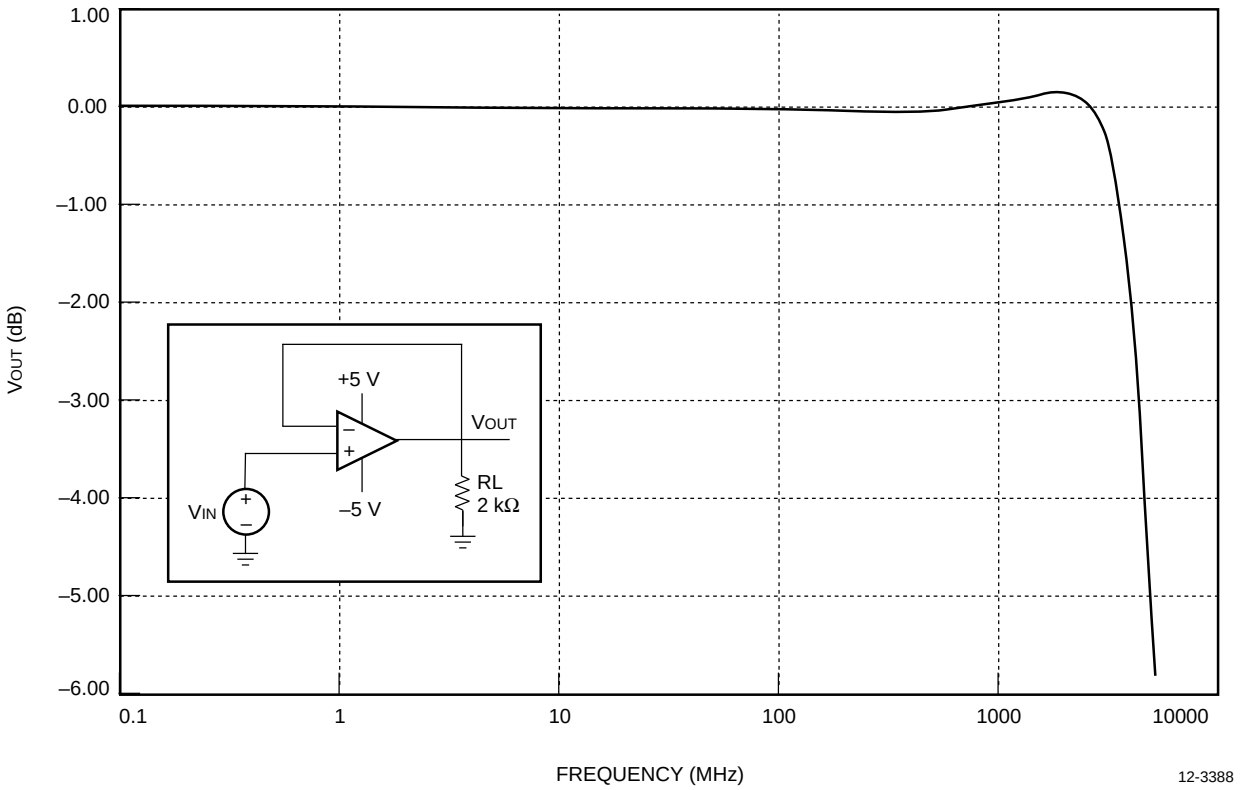

Figure 4. Simulated ac Unity Gain of the CF-OpAmp

Simulated Performance (continued)

Slew Rate Limit

The slew rate limit is illustrated in Figure 5. A 2 V input pulse is applied with a rise time of 1 ns. The CF-OpAmp produces a 4 V output pulse with a rise time of approximately 600 V/µs, and a fall time of 1800 V/µs. The mismatch in rise and fall times is attributed to the mismatches in the parasitic capacitances of the npn and pnp transistors.

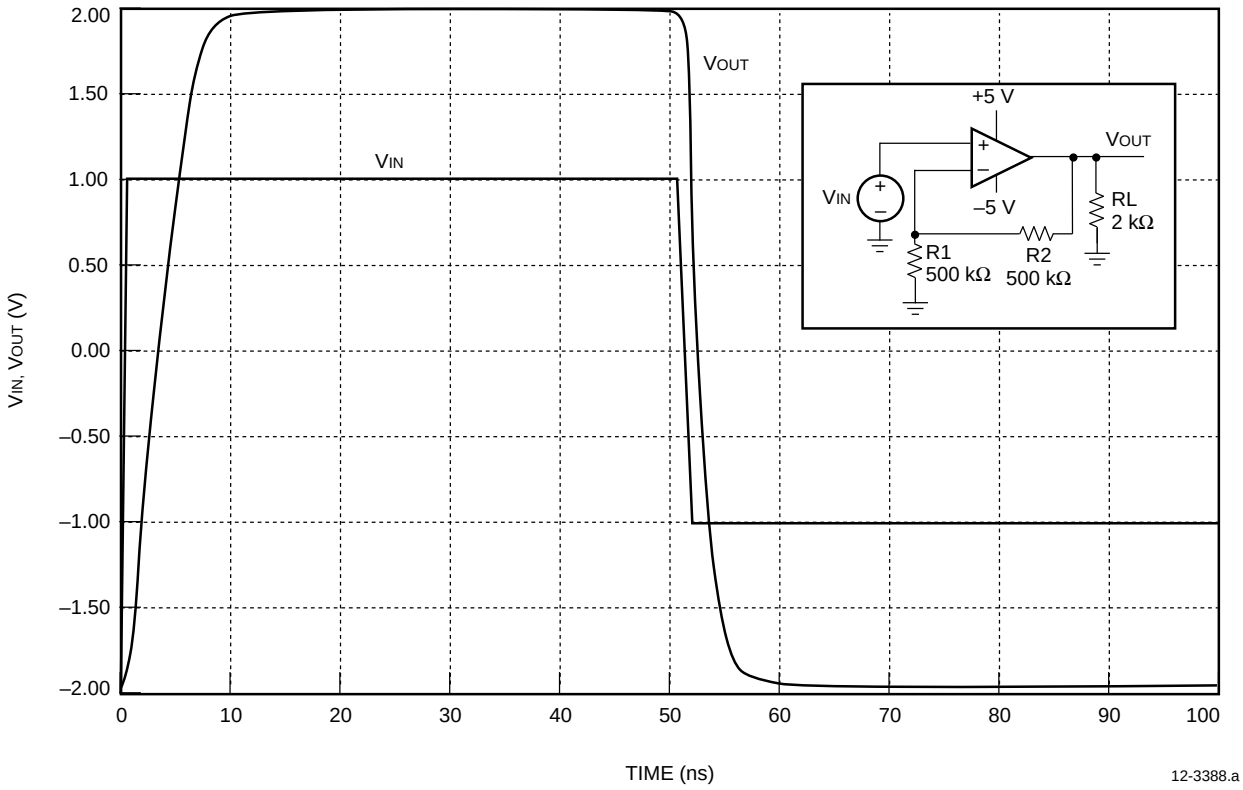

Figure 5. Simulated Transient Response of the CF-OpAmp Illustrating Slew Rate Capabilities

Simulated Performance (continued)

Input Impedance

The input impedance of the CF-OpAmp is illustrated in Figure 6. The input impedance is about 280 kΩ up to 1 MHz and then drops off at 20 dB per decade, reaching 300 Ω at 1 GHz.

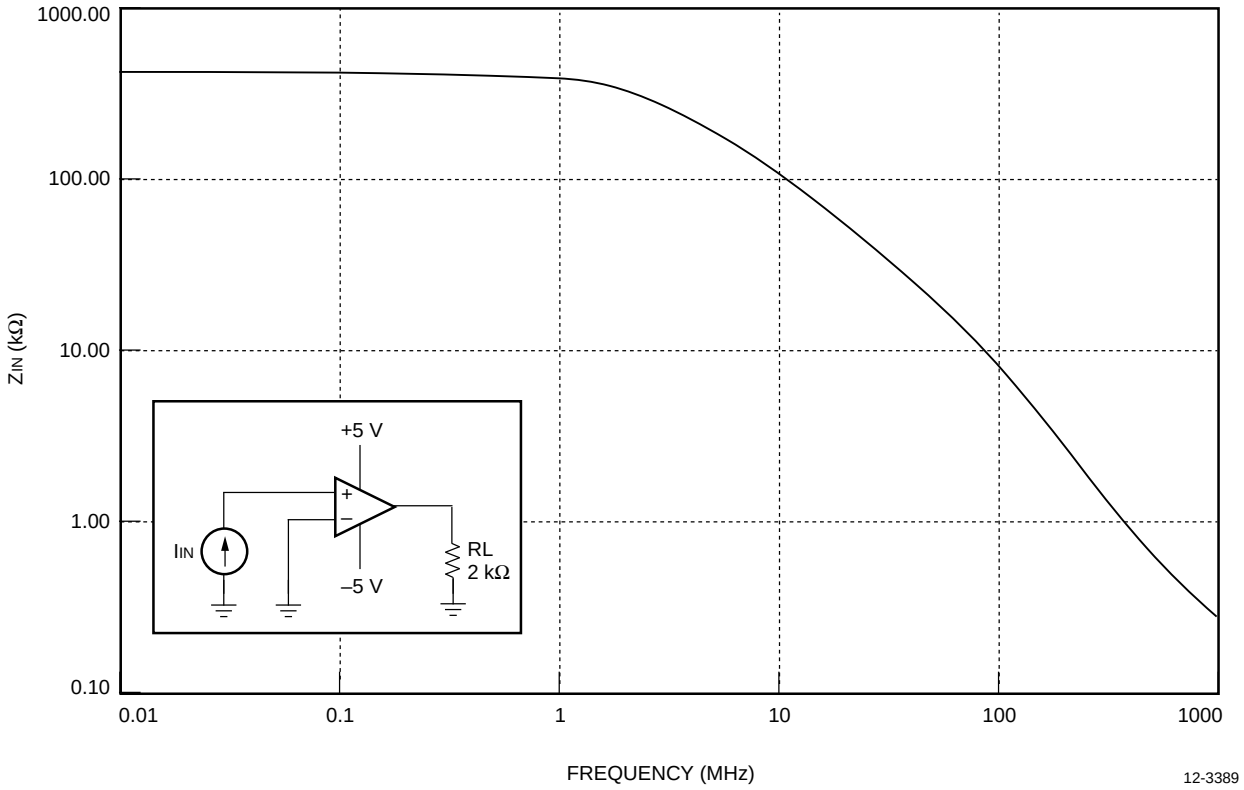

Figure 6. Simulated Input Impedance of the Positive Input for the CF-OpAmp

Performance Improvements

Power

The dc power dissipation is related to the dc bias current plus the drive current, times the voltage drop across the IC. The ac power consumption is the power consumption plus the RMS power on the IC. The biasing current is set by the biasing circuits in the VCR macrocell. The VCR cell has been designed to compensate for process and temperature variations. The temperature variation is minimized by the use of a bandgap reference circuit, and the process variation is minimized by avoiding tolerances that depend on absolute device values.

Varying the value of the biasing current in the CF-OpAmp changes the dc power proportionally. Changing the biasing current affects the bandwidth, the slew rate, and the current-drive capability.

dc Gain

The dc gain is controlled by an external resistor, R1, and the impedance in parallel with C1. Hence, reducing R1, and/or increasing the impedance in parallel with C1, will increase the dc gain.

Bandwidth

The bandwidth is controlled by C1 and the resistance in parallel with C1. Increasing R x C1 lowers the bandwidth by lowering the corner frequency of the dominant pole. This also affects the open-loop unity gain. Changing the dc gain by varying R (or I1 if R is small) changes the open-loop unity gain but does not change the bandwidth.

Slew Rate

The slew rate is controlled by the difference current at the summing node and C1. Increasing the current in the negative input terminal or reducing C1 increases the slew rate. Decreasing C1 also has the adverse effect of reducing the stability of the op amp. Increasing the current improves the stability but increases the dissipated power.

Stability

Increasing C1 increases the stability but reduces the bandwidth and the slew rate. Increasing the current also increases the stability to a point, but at the expense of increasing dissipated power.

Input Impedance

The input impedance of the positive input terminal can be increased by lowering the biasing current. This also lowers the dc gain, the bandwidth, and the slew rate. An alternate approach to increasing the input impedance is to use an input-biasing current-cancellation circuit.

Current Drive

The output current drive can be increased by increasing the biasing current. This will also increase the dissipated power. An alternative is to use Darlingtons in the output stage. This will provide an extra stage of current gain, but will reduce the head room by one VBE.

Input-Referred Noise

The input-referred noise is primarily due to the thermal noise of the base resistance and the shot noise of the junction currents in the input transistors Q10 and Q11. To minimize the noise, the input devices are made as large as possible to obtain the minimum base resistance. Since large devices have more capacitances associated with them, it requires more junction current to retain the speed. An optimal point for minimum noise operation is where the base resistance thermal noise equals the junction shot noise.

Electrical Characteristics

Conditions: T_J = 25 °C, R_L = 2 kΩ, VSP = +5 V, VSN = –5 V.

Table 1. dc Characteristics

Name	Conditions	Typical Value	Unit
Voltage Supply Range	—	±1 to ±5	V
Supply Current Draw	V_{IN} = –3.76 mV	1.5	mA

Table 2. dc Performance

Name	Conditions	Typical Value	Unit
Input Bias Current	V+/V–, V_{IN} = 3.76 mV	1.4/22.6	µA
Input Impedance	Input of V+	280	kΩ
Input Offset Voltage	—	–3.76	mV
Output Voltage Swing (head/floor room)	VSP – V_{OUT}, V_{OUT} – VSN	1, 1	V
Common-mode Range (head/floor room)	VSP – V_{IN}, V_{IN} – VSN	1, 1	V
Output Current Drive	—	6	mA
dc Gain	—	60	dB

Table 3. ac Performance

Name	Conditions	Typical Value	Unit
Open-loop Unity Gain Frequency	—	500	MHz
Open-loop Bandwidth	—	650	kHz
Closed-loop Unity Gain Bandwidth	—	450	MHz

Table 4. Dynamic Performance

Name	Conditions	Typical Value	Unit
Slew Rate	Gain of 2	600	V/µs
Noise Voltage at Input	V_{IN} = –3.76 mV, Open Loop	2.1	nV/$\sqrt{Hz}$

Notes

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