LTC4210-1/LTC4210-2

Hot Swap Controller in 6-Lead SOT-23 Package

July 2002

FEATURES

- **Allows Safe Board Insertion and Removal from a Live Backplane**
- **Adjustable Analog Current Limit with Circuit Breaker**
- **Fast Response Limits Peak Fault Current**
- Automatic Retry or Latch Off On Current Fault
- Adjustable Supply Voltage Power-Up Rate
- High Side Drive for External MOSFET Switch
- Controls Supply Voltages from 2.7V to 16.5V
- Undervoltage Lockout
- Adjustable Overvoltage Protection
- Low Profile (1mm) ThinSOT™ Package

APPLICATIONS

- Hot Board Insertion
- Electronic Circuit Breaker
- Industrial High Side Switch/Circuit Breaker

DESCRIPTION

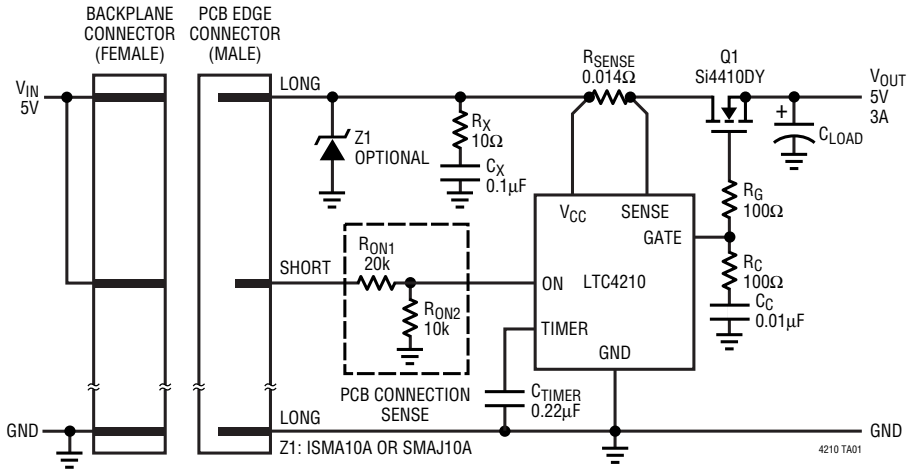
The LTC®4210 is a 6-pin SOT-23 Hot Swap™ controller that allows a board to be safely inserted and removed from a live backplane. An internal high side switch driver controls the GATE of an external N-channel MOSFET for a supply voltage ranging from 2.7V to 16.5V. The LTC4210 provides the initial timing cycle and allows the GATE to be ramped up at an adjustable rate.

The LTC4210 features a fast current limit loop providing active current limiting together with a circuit breaker timer. The signal at the ON pin turns the chip on and off and is also used for the reset function.

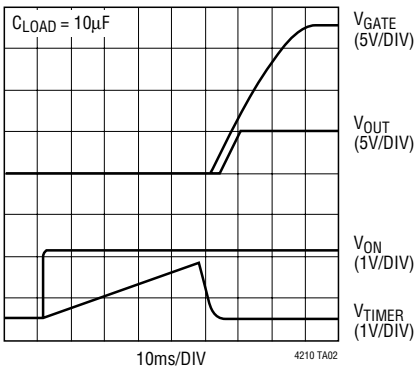
This part is available in two options: the LTC4210-1 for automatic retry on overcurrent fault and the LTC4210-2 for latch off on an overcurrent fault.

TYPICAL APPLICATION

Single Channel 5V Hot Swap Controller



Power-Up Sequence

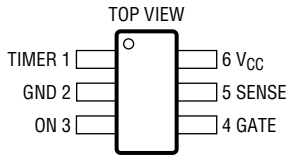


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 17V
Input Voltage (SENSE, TIMER) .. –0.3V to (V_{CC} + 0.3V)
Input Voltage (ON) ..... –0.3V to 17V
Output Voltage (GATE) ..... Internally Limited (Note 3)
Operating Temperature Range
LTC4210-1C/LTC4210-2C ..... 0°C to 70°C
LTC4210-1I/LTC4210-2I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



S6 PACKAGE
6-LEAD PLASTIC SOT-23

T_{JMAX} = 125°C, θ_{JA} = 230°C/ W

ORDER PART NUMBER
LTC4210-1CS6 LTC4210-2CS6 LTC4210-1IS6 LTC4210-2IS6
S6 PART MARKING
LTYW LTYX LTF5 LTF6

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 5V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		16.5	V
I_{CC}	V_{CC} Supply Current		●		0.65	3.5	mA
V_{LKOR}	V_{CC} Undervoltage Lockout Release	V_{CC} Rising	●	2.2	2.5	2.65	V
$V_{LKOHYST}$	V_{CC} Undervoltage Lockout Hysteresis				100		mV
I_{INON}	ON Pin Input Current		●	–10	0	10	µA
$I_{INSENSE}$	SENSE Pin Input Current	$V_{SENSE} = V_{CC}$	●	–10	5	10	µA
V_{CB}	Circuit Breaker Trip Voltage	$V_{CB} = (V_{CC} – V_{SENSE})$	●	44	50	56	mV
I_{GATEUP}	GATE Pin Pull-Up Current	V_{GATE} = 0V	●	–5	–10	–15	µA
I_{GATEDN}	GATE Pin Pull-Down Current	V_{TIMER} = 1.5V, V_{GATE} = 3V or V_{ON} = 0V, V_{GATE} = 3V or $V_{CC} – V_{SENSE}$ = 100mV, V_{GATE} = 3V			25		mA
ΔV_{GATE}	External N-Channel Gate Drive	$V_{GATE} – V_{CC}$, V_{CC} = 2.7V $V_{GATE} – V_{CC}$, V_{CC} = 3V $V_{GATE} – V_{CC}$, V_{CC} = 3.3V $V_{GATE} – V_{CC}$, V_{CC} = 5V $V_{GATE} – V_{CC}$, V_{CC} = 12V $V_{GATE} – V_{CC}$, V_{CC} = 15V	● ● ● ● ● ●	4.0 4.5 5.0 10 9.0 6.0	6.5 7.5 8.5 12 12 11	8 10 12 16 16 18	V V V V V V
$I_{TIMERUP}$	TIMER Pin Pull-Up Current	Initial Cycle, V_{TIMER} = 1V During Current Fault Condition, V_{TIMER} = 1V	● ●	–2 –25	–5 –60	–8.5 –100	µA µA
$I_{TIMERDN}$	TIMER Pin Pull-Down Current	After Current Fault Disappears, V_{TIMER} = 1V Under Normal Conditions, V_{TIMER} = 1V	●		2 100	3.5	µA µA
V_{TIMER}	TIMER Pin Threshold	High Threshold, TIMER Rising Low Threshold, TIMER Falling	● ●	1.22 0.15	1.3 0.2	1.38 0.25	V V
$V_{TMRHYST}$	TIMER Threshold Hysteresis				100		mV
V_{ON}	ON Pin Threshold	ON Threshold, ON Rising	●	1.22	1.3	1.38	V
V_{ONHYST}	ON Pin Threshold Hysteresis				80		mV

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 5V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{OFF,TMRHIGH}$	Turn-Off Time (TIMER Rise to GATE Fall)	V_{TIMER} = 0V to 2V Step, V_{CC} = V_{ON} = 5V			1		µs
$t_{OFF,ONLOW}$	Turn-Off Time (ON Fall to GATE Fall)	V_{ON} = 5V to 0V Step, V_{CC} = 5V			30		µs
$t_{OFF,VCCLOW}$	Turn-Off Time (V_{CC} Fall to IC Reset)	V_{CC} = 5V to 2V Step, V_{ON} = 5V			30		µs

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 3: An internal zener on the GATE pin clamps the charge pump voltage to a typical maximum voltage of 26V. External overdrive of the GATE pin beyond the internal zener voltage may damage the device. Without a limiting resistor, the GATE capacitance must be <0.15µF at maximum V_{CC}. If a lower GATE pin clamp voltage is desired, an external zener diode may be used.

PIN FUNCTIONS

TIMER (Pin 1): Timer Input Pin. An external capacitor C_{TIMER} programs the timing duration of this multimode TIMER function. The GATE pin turns off whenever the TIMER pin is pulled beyond the COMP2 threshold, such as for overvoltage detection with an external zener.

GND (Pin 2): Ground Pin.

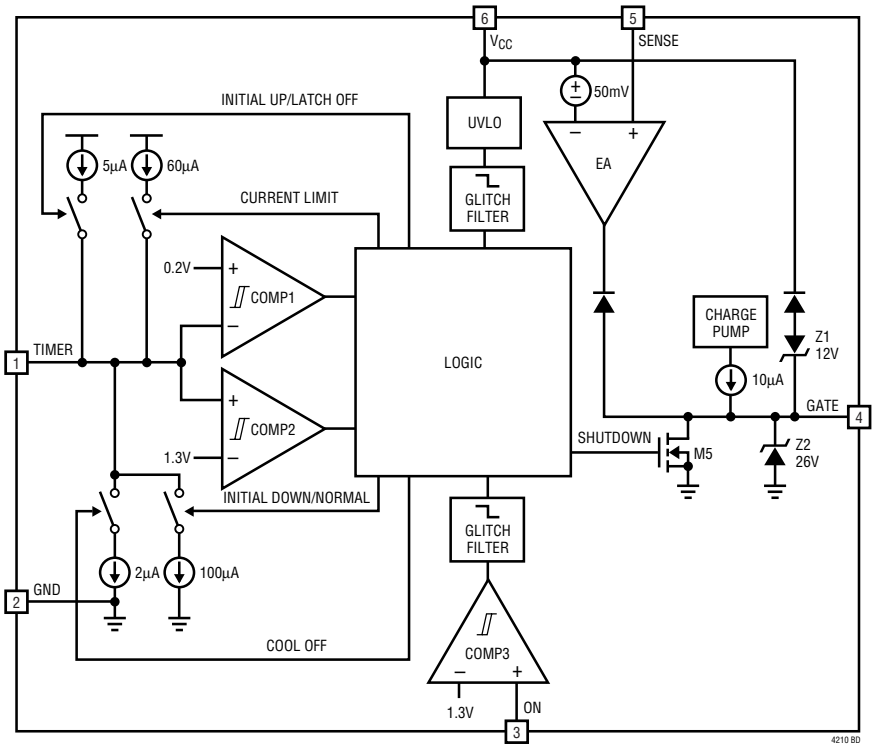
ON (Pin 3): ON Input Pin. The ON pin comparator has a low-to-high threshold of 1.3V with 80mV hysteresis and a glitch filter. When the ON pin is low, the chip is reset. When the ON pin goes high, the GATE turns on after the initial timing cycle.

GATE (Pin 4): GATE Output Pin. This pin is the high side gate drive of an external N-channel MOSFET. An internal charge pump provides a 10µA pull-up current with zener clamps to V_{CC} and ground. In overload, the EA amplifier controls the external MOSFET to maintain a constant load current. External compensation should be connected to this pin for current limit loop stability.

SENSE (Pin 5): Current Limit Sense Input Pin. A sense resistor between the V_{CC} and SENSE pins sets the analog current limit. In overload, the EA amplifier controls the external MOSFET gate to maintain the SENSE pin voltage at 50mV below V_{CC}. When the EA amplifier is maintaining current limit, the TIMER circuit breaker mode is activated. The current limit loop/circuit breaker mode can be disabled by connecting the SENSE pin to the V_{CC} pin.

V_{CC} (Pin 6): Positive Supply Input Pin. The operating supply voltage range is between 2.7V to 16.5V. An undervoltage lockout (UVLO) circuit with a glitch filter resets the LTC4210 when a low supply voltage is detected.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Hot Circuit Insertion

When circuit boards are inserted into live backplanes, the supply bypass capacitors can draw large transient currents from the backplane power bus as they charge. Such transient currents can cause permanent damage to connector pins, glitches on the system supply or reset other boards in the system.

The LTC4210 is designed to turn a printed circuit board's supply voltage ON and OFF in a controlled manner, allowing the circuit board to be safely inserted into or removed from a live backplane. The LTC4210 can reside either on the backplane or on the daughter board for hot circuit insertion applications.

Overview

The LTC4210 is designed to operate over a range of supplies from 2.7V to 16.5V. Upon insertion, an undervoltage lockout circuit determines if sufficient supply voltage is present. When the ON pin goes high an initial timing cycle assures that the board is fully seated in the backplane before the FET is turned on. A single timer capacitor sets the periods for all of the timer functions. After the initial timing cycle the LTC4210 can either start up in current limit or with a lower load current. Once the external MOSFET is fully enhanced and the supply has ramped up, the LTC4210 monitors the load current through an external sense resistor. Overcurrent faults are actively limited to $50mV/R_{SENSE}$ for a specified circuit breaker timer limit. The LTC4210-1 will automatically retry after a current limit fault while the LTC4210-2 latches off. The timer function limits the retry duty cycle to allow for MOSFET cooling.

Undervoltage Lockout

An internal undervoltage lockout (UVLO) circuit resets the LTC4210 if the V_{CC} supply is too low for normal operation. UVLO has a low-to-high threshold of 2.5V, a 100mV hysteresis and a high-to-low glitch filter of 30µs. Above 2.5V supply voltage, the LTC4210 will start if the ON pin conditions are met. A short supply dip below 2.4V for less than 30µs is ignored to allow for bus supply transients.

APPLICATIONS INFORMATION

ON Function

The ON pin is the input to a comparator which has a low-to-high threshold of 1.3V, an 80mV hysteresis and a high-to-low glitch filter of 30µs. A low input on the ON pin resets the LTC4210 TIMER status and turns off the external MOSFET by pulling the GATE pin to ground. A low-to-high transition on the ON pin starts an initial cycle followed by a start-up cycle. A 10k pull-up resistor connecting the ON pin to the supply is recommended. The 10k resistor shunts any potential static charge on the backplane and reduces the overvoltage stress at the ON pin during hot swapping. Alternatively, an external resistor divider at the ON pin can be used to program an undervoltage lockout value higher than the internal UVLO circuit. An RC filter can be added at the ON pin to increase the delay time at card insertion if the internal glitch filter delay is insufficient.

GATE Function

During hot insertion of the PCB, an abrupt application of supply voltage charges the external MOSFET drain/gate capacitance. This can cause an unwanted gate voltage spike. An internal proprietary circuit holds GATE low before the internal circuitry wakes up. This reduces the MOSFET current surges substantially at insertion. The GATE pin is held low in reset mode and during the initial timing cycle. In the start-up cycle the GATE pin is pulled up by a 10µA current source. During an overcurrent fault condition, the error amplifier servoes the GATE pin to maintain a constant current to the load until the circuit breaker trips. When the circuit breaker trips, the GATE pin shuts down abruptly.

Current Limit Circuit Breaker Function

The LTC4210 features a current limiting circuit breaker instead of the traditional comparator circuit breaker. When there is a sudden load current surge, such as a low impedance fault, the bus supply voltage can drop significantly to a point where the power to an adjacent card is affected, causing system malfunctions. The LTC4210 fast response error amplifier (EA) instantly limits current by reducing the external MOSFET GATE pin voltage. This minimizes the bus supply voltage drop and permits power budgeting and fault isolation without affecting neighboring cards. A compensation circuit should be connected to the GATE pin for current limit loop stability.

Sense Resistor Consideration

The nominal fault current limit is determined by a sense resistor connected between V_{CC} and the SENSE pin as given by Equation 1.

$$I_{LIMIT(NOM)} = \frac{V_{CB(NOM)}}{R_{SENSE(NOM)}} = \frac{50mV}{R_{SENSE(NOM)}} \qquad (1)$$

The power rating of the sense resistor should be rate at fault current level. Table 2 in the Appendix lists some common sense resistors.

For proper circuit breaker operation, Kelvin-sense PCB connections between the sense resistor and the LTC4210 V_{CC} and SENSE pins are strongly recommended. The drawing in Figure 1 illustrates the connections between the LTC4210 and the sense resistor. PCB layout should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistor should include good thermal management techniques for optimal sense resistor power dissipation.

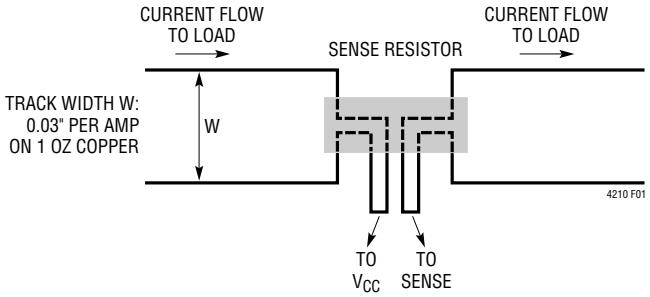


Figure 1. Making PCB Connections to the Sense Resistor

APPLICATIONS INFORMATION

Calculating Current Limit

For a selected R_{SENSE}, the nominal load current is given by Equation 1. The minimum load current is given by Equation 2:

$$I_{LIMIT(MIN)} = \frac{V_{CB(MIN)}}{R_{SENSE(MAX)}} = \frac{44mV}{R_{SENSE(MAX)}} \quad (2)$$

where

$$R_{SENSE(MAX)} = R_{SENSE} \bullet \left(1 + \frac{R_{TOL}}{100}\right)$$

The maximum load current is given by Equation 3:

$$I_{LIMIT(MAX)} = \frac{V_{CB(MAX)}}{R_{SENSE(MIN)}} = \frac{56mV}{R_{SENSE(MIN)}} \quad (3)$$

where

$$R_{SENSE(MIN)} = R_{SENSE} \bullet \left(1 - \frac{R_{TOL}}{100}\right)$$

If a 7mΩ sense resistor with ±1% tolerance is used for current limiting, the nominal current limit is 7.14A. From Equations 2 and 3, $I_{LIMIT(MIN)}$ = 6.22A and $I_{LIMIT(MAX)}$ = 8.08A. For proper operation, the minimum current limit must exceed the circuit maximum operating load current with margin for start-up; viz. average $I_{CLOAD} > 0$ and $t_{CBDELAY}$ requirement in Equation 13 met. The sense resistor power rating must exceed $V_{CB(MAX)}^2/R_{SENSE(MIN)}$.

Frequency Compensation

A compensation circuit should be connected to the GATE pin for current limit loop stability.

Method 1

The simplest frequency compensation network consists of R_C and C_C (Figure 2a). The total GATE capacitance is:

$$C_{GATE} = C_{ISS} + C_C \quad (4)$$

A general rule is $5\Omega \le R_C \le 1k\Omega$ and $C_C \ge 10nF$.

Method 2

Figure 2b compensation network is similar to the circuitry used in method 1 but with an additional gate resistor R_G. The R_G resistor helps to minimize high frequency parasitic oscillations frequently associated with the power MOSFET. In some applications, the user may find that R_G helps in short-circuit transient recovery as well. However, too large of an R_G value will slow down the turn-off time. The recommended R_G range is between 5Ω and 500Ω. Usually, method 2 is preferred when the input supply voltage is greater than 10V. R_G limits the current flow into the GATE pin's internal zener clamp during transient events. The recommended R_C and C_C values are the same as method 1. The parasitic compensation capacitor C_P is required when 0.2µF < load capacitance C_L < 9µF, otherwise it is optional.

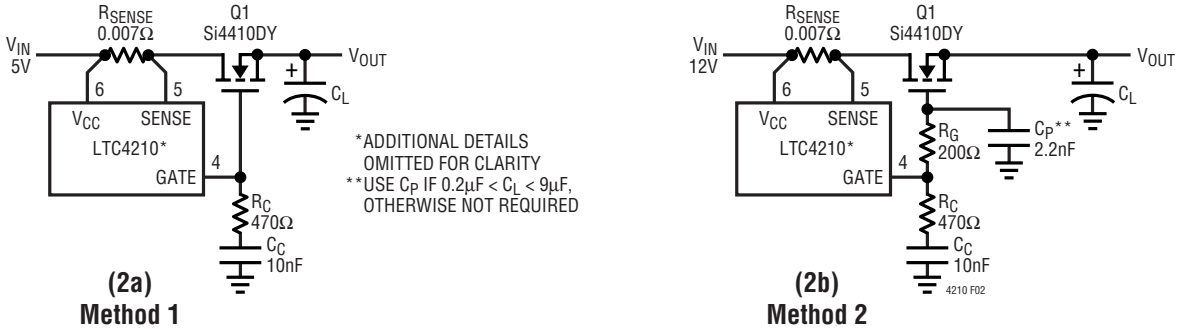


Figure 2. Frequency Compensation

APPLICATIONS INFORMATION

Parasitic MOSFET Oscillation

There are two possible parasitic oscillations when the MOSFET operates as a source follower at power-up ramp or during current limiting. The first type of oscillation occurs at high frequencies, typically above 1MHz. This high frequency oscillation is easily damped with R_G as mentioned in method 2.

The second type of oscillation occurs at frequencies between 200kHz and 800kHz when the load capacitance is between 0.2µF and 9µF, the presence of R_G and R_C resistance, the absence of a drain bypass capacitor, a combination of bus wiring inductance and bus supply output impedance. There are several ways to prevent this second type of oscillation. The simplest way is to avoid load capacitance below 10µF, the second choice is connecting an external $C_P > 1.5nF$.

Whichever method of compensation is used, board level short-circuit testing is highly recommended as board layout can affect transient performance. Beside frequency compensation, the total gate capacitance C_{GATE} also determines the GATE start-up as in Equation 6. The C_{GATE} should be kept below 0.15µF at high supply operation as the capacitive energy ($0.5 \bullet C_{GATE} \bullet V_{GATE}^2$) is discharged by LTC4210's internal pull-down transistor. This prevents the internal pull-down transistor from overheating when GATE turns off and/or is servoing during current limiting.

Timer Function

The TIMER pin handles several key functions with an external capacitor, C_{TIMER}. There are two comparator thresholds: COMP1 (0.2V) and COMP2 (1.3V). The four timing current sources are:

5µA pull-up
60µA pull-up
2µA pull-down
100µA pull-down

The 100µA is a nonideal current source approximating a 7k resistor below 0.4V, or approximately 85µA average current between the COMP1 and COMP2 thresholds.

Initial Timing Cycle

When the card is being inserted into the bus connector, the long pins mate first which brings up the supply V_{IN} at time point 1 of Figure 3. The LTC4210 is in reset mode as the ON pin is low. GATE is pulled low and the TIMER pin is pulled low with a 100µA source. At time point 2, the short pin makes contact and ON is pulled high. At this instant, a start-up check requires that the supply voltage be above UVLO, the ON pin be above 1.3V and the TIMER pin voltage be less than 0.2V. When these three conditions are fulfilled, the initial cycle begins and the TIMER pin is pulled high with 5µA. At time point 3, the TIMER reaches the COMP2 threshold and the first portion of the initial cycle ends. An approximately 85µA source then pulls down the TIMER pin until it reaches 0.2V at time point 4. The initial cycle delay is:

$$t_{INITIAL} \approx \left(1.3V \bullet \frac{C_{TIMER}}{5\mu A}\right) + \left(1.1V \bullet \frac{C_{TIMER}}{85\mu A}\right) \quad (5)$$

$$= 0.27 \bullet C_{TIMER}\ [s/\mu F]$$

When the initial cycle terminates, a start-up cycle is activated and the GATE pin ramps high. The TIMER pin continues to be pulled down by the 100µA source.

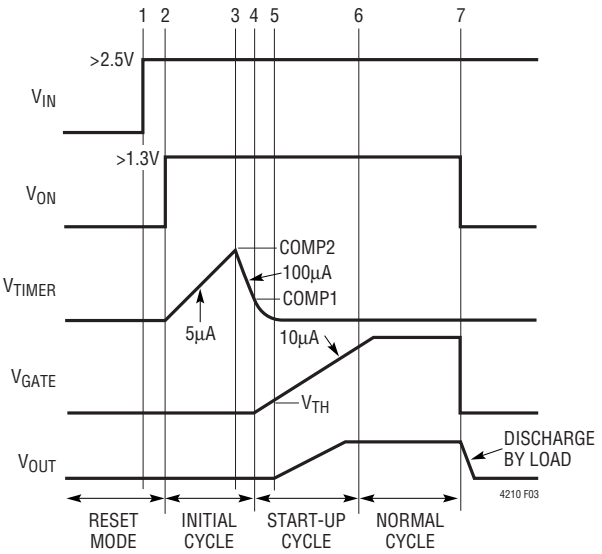


Figure 3. Normal Operating Sequence

APPLICATIONS INFORMATION

Start-Up Cycle Without Current Limit

The GATE is released with a 10µA pull-up at time point 4 of Figure 3. At time point 5, GATE reaches the external MOSFET threshold and V_{OUT} starts to follow the GATE ramp up. If the R_{SENSE} current is below current limit, the GATE ramps at a constant rate of:

$$\frac{\Delta V_{GATE}}{\Delta T} = \frac{I_{GATE}}{C_{GATE}} \quad (6)$$

where C_{GATE} is the total capacitance at the GATE pin.

The current through R_{SENSE} can be divided into two components; I_{CLOAD} due to the total load capacitance (C_{LOAD}) and I_{LOAD} due to the noncapacitive load elements. The load bypass capacitance typically dominates C_{LOAD}.

For a successful start-up without current limit, $I_{RSENSE} < I_{LIMIT}$:

$$I_{RSENSE} = \left(C_{LOAD} \bullet \frac{\Delta V_{OUT}}{\Delta T} \right) + I_{LOAD} \quad (8)$$

Due to the voltage follower configuration, the V_{OUT} ramp rate approximately tracks V_{GATE}:

$$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{CLOAD}}{C_{LOAD}} \approx \frac{\Delta V_{GATE}}{\Delta T} = \frac{I_{GATE}}{C_{GATE}} \quad (9)$$

At time point 6, V_{OUT} is approximately V_{IN} but GATE ramp-up continues until it reaches a maximum voltage. This maximum voltage is determined either by the charge pump or the internal clamp.

Start-Up Cycle With Current Limit

If the duration of the current limit is brief during start-up (Figure 4) and it did not last beyond the circuit breaker function time out, the GATE behaves the same as in start-up without current limit except for the time interval between time point 5A and time point 5B. The servo amplifier limits I_{RSENSE} by decreasing the I_{GATE} current (<10µA).

$$I_{RSENSE} = I_{LIMIT} = \frac{50mV}{R_{SENSE}} \quad (10)$$

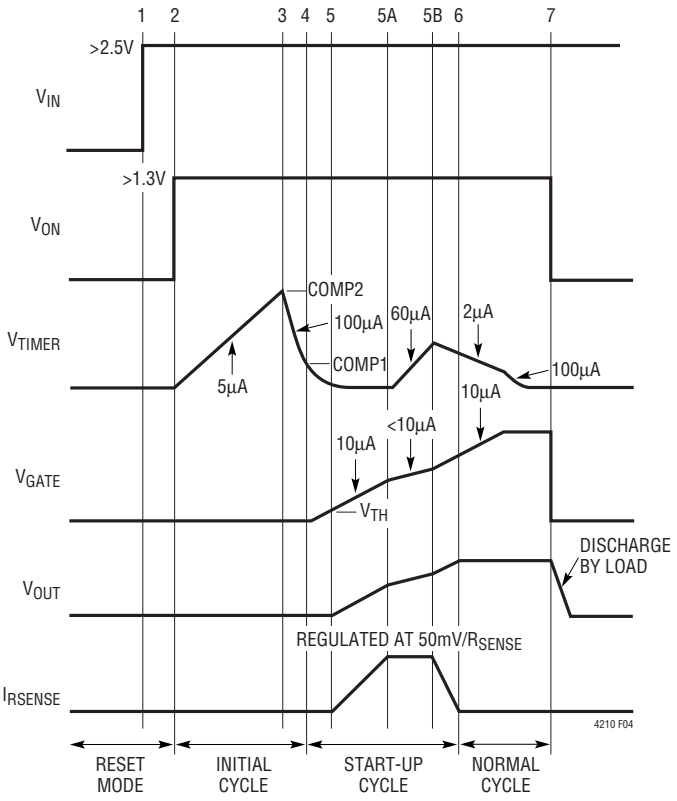


Figure 4. Operating Sequence with Current Limiting at Start-Up Cycle

Equations 8 and 9 are applicable but with a lower GATE and V_{OUT} ramp rate. If there is a shortfall in I_{LOAD} during current limiting, C_{LOAD} will supply this shortfall resulting in V_{OUT} drop. While the servo amplifier is active, the circuit breaker function simultaneously sources 60µA into the TIMER pin. For successful completion of a current limit start-up cycle, the average $I_{CLOAD} > 0$ and the duration of the current limit < $t_{CBDELAY}$ of Equation 14. Multiple intermittent faults are possible but TIMER must not exceed the COMP2 threshold during start-up to prevent premature termination by the GATE pulling low when the TIMER pin reaches COMP2 threshold.

Gate Start-Up Time

The start-up time without current limit is given by:

$$t_{STARTUP} = C_{GATE} \bullet \frac{V_{TH} + V_{IN}}{I_{GATE}} \quad (11)$$

$$t_{STARTUP} = C_{GATE} \bullet \frac{V_{TH}}{I_{GATE}} + C_{GATE} \bullet \frac{V_{IN}}{I_{GATE}}$$

APPLICATIONS INFORMATION

During current limiting, the second term in Equation 11 is partly modified from $C_{GATE} \bullet V_{IN}/I_{GATE}$ to $C_{LOAD} \bullet V_{IN}/I_{CLOAD}$. To ensure the LTC4210 will start up, consider the extreme case of current limited start-up with a constant I_{LOAD}. The start-up is given by:

$$t_{STARTUP} = C_{GATE} \bullet \frac{V_{TH}}{I_{GATE}} + C_{LOAD} \bullet \frac{V_{IN}}{I_{CLOAD}} \quad (12)$$

$$= C_{GATE} \bullet \frac{V_{TH}}{I_{GATE}} + C_{LOAD} \bullet \frac{V_{IN}}{I_{RSENSE} - I_{LOAD}}$$

The circuit will fail to start up for this extreme case if the average of $I_{CLOAD} \leq 0$ and:

$$t_{CBDELAY} = 1.3V \bullet \frac{C_{TIMER}}{60\mu A} > \quad (13)$$

$$C_{LOAD} \bullet \frac{V_{IN}}{I_{RSENSE} - I_{LOAD}}$$

As constant load current is rare in application, Equation 13 is a good guide for ensuring start-up.

Circuit Breaker Timer Operation

When a current limit fault is encountered at time point A in Figure 5, the circuit breaker timing is activated with a 60µA pull-up. The circuit breaker trips at time point B if the fault is still present and the TIMER pin voltage reaches the COMP2 threshold and the LTC4210 shuts down. For a continuous fault, the circuit breaker delay is:

$$t_{CBDELAY} = 1.3V \bullet \frac{C_{TIMER}}{60\mu A} \quad (14)$$

Intermittent overloads may exceed current limit as in Figure 6, but if the duration is sufficiently short, the TIMER pin may not reach the COMP2 threshold and the LTC4210 will not shut down. To handle this situation, the TIMER discharges with 2µA whenever (V_{CC} – SENSE) voltage is below the 50mV limit and the TIMER voltage is between the COMP1 and COMP2 thresholds. When the TIMER voltage falls below the COMP1 threshold, the TIMER pin is discharged with an equivalent 7k resistor (normal mode, 100µA source) when (V_{CC} – SENSE) voltage is below the 50mV limit. If the TIMER pin does not drop below the COMP1 threshold, any intermittent overload with an aggregate duty cycle of more than 3.2% will eventually trip the circuit breaker. Figure 7 shows the circuit breaker response time in seconds normalized to 1µF. The asymmetric charging and discharging of TIMER is a fair gauge of MOSFET heating.

$$\frac{t}{C_{TIMER}}(\mu F) = \frac{1.3V}{(60\mu A \bullet D) - 2\mu A} \quad (15)$$

When the circuit breaker trips, the GATE pin is pulled low. The TIMER enters latchoff mode with a 5µA pull-up for the

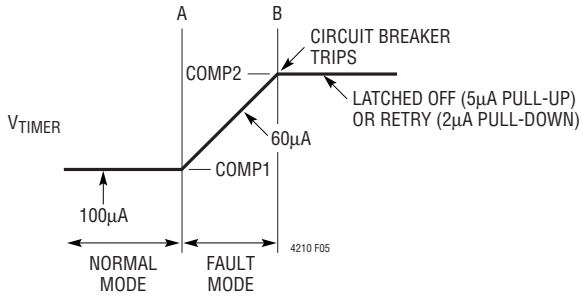


Figure 5. A Continuous Fault Timing

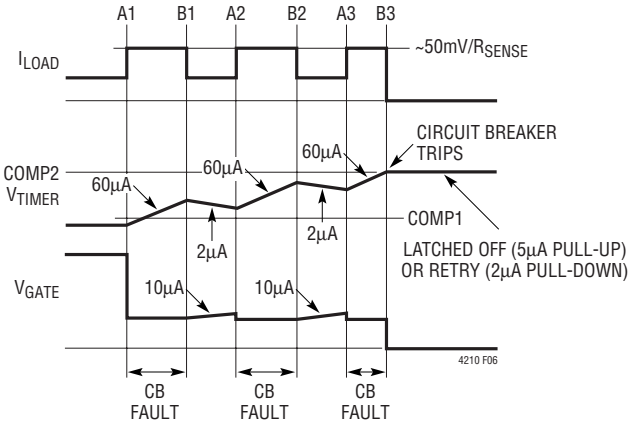


Figure 6. Mulitple Intermittent Overcurrent Conditon

APPLICATIONS INFORMATION

LTC4210-2 (latched-off version), while an autoretry "cool-off" cycle begins with a 2µA pull-down for the LTC4210-1 (autoretry version). An autoretry cool-off delay of the LTC4210-1 between COMP2 and COMP1 thresholds takes:

$$t_{COOLOFF} = 1.1V \bullet \frac{C_{TIMER}}{2\mu A} \quad (16)$$

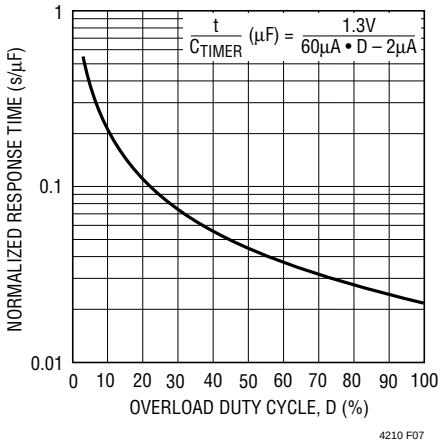


Figure 7. Circuit Breaker Timer Response for Intermittent Overload

Autoretry After Current Fault (LTC4210-1)

Figure 8 shows the waveforms of the LTC4210-1 (autoretry version) during a circuit breaker fault. At time point B1, the TIMER trips the COMP2 threshold of 1.3V. The GATE pin pulls to ground while TIMER begins a "cool-off" cycle with a 2µA pull-down to the COMP1 threshold of 0.2V. At time point C1, the TIMER pin pulls down with approximately a 7k resistor to ground and a GATE start-up cycle is initiated. If the fault persists, the fault autoretry duty cycle is approximately 3.2%. Pulling the ON pin low for more than 30µs will stop the autoretry function and put the chip in reset mode.

Latch-Off After Current Fault (LTC4210-2)

Figure 9 shows the waveforms of the LTC4210-2 (latch-off version) during a circuit breaker fault. At time point B, the TIMER trips the COMP2 threshold. The GATE pin pulls to ground while the TIMER pin is latched high by a 5µA pull-up. The TIMER pin eventually reaches the soft-clamped voltage (V_{CLAMP}) of 2.3V if there is no external current bias. To clear the latchoff mode, the user can either pull the

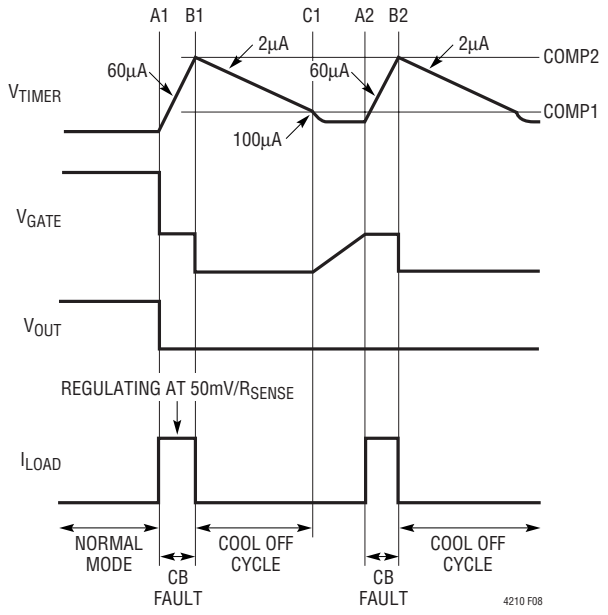


Figure 8. Automatic Retry After Overcurrent Fault

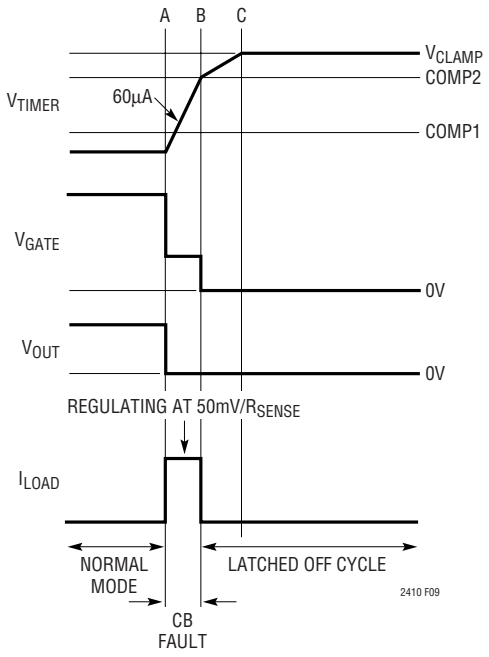


Figure 9. Latchoff After Overcurrent Fault

APPLICATIONS INFORMATION

TIMER pin to below 0.2V externally or cycle the ON pin low for more than 30µs.

Normal Mode/External Timer Control

Whenever the TIMER pin voltage drops below the COMP1 threshold, but is not in reset mode, the TIMER enters normal (100µA source) mode with an equivalent 7k resistive pull-down. Table 1 shows the relationship of $t_{INITIAL}$, $t_{CBDELAY}$, $t_{COOLOFF}$ vs C_{TIMER}.

If the TIMER pin is pulled beyond the COMP2 threshold, the GATE pin is pulled to ground immediately. This allows the TIMER pin to be used for overvoltage detection, see Figure 11.

Externally forcing the TIMER pin below the COMP1 threshold will reset the TIMER to normal mode. During overvoltage detection, the TIMER's 100µA pull-down current will continue to be on if (V_{CC} – SENSE) voltage is below 50mV. If the (V_{CC} – SENSE) voltage exceeds 50mV during the overvoltage detection, the TIMER current will be the same as described for latched-off or autoretry mode. See the section SUPPLY OVERVOLTAGE DETECTION USING TIMER PIN for details of the application.

Table 1: $t_{INITIAL}$, $t_{CBDELAY}$, $t_{COOLOFF}$ vs C_{TIMER}

C_{TIMER} (µF)	$t_{INITIAL}$ (ms)	$t_{CBDELAY}$ (ms)	$t_{COOLOFF}$ (ms)
0.033	9.0	0.7	18.2
0.047	12.8	1	25.9
0.068	18.6	1.5	37.4
0.082	22.4	1.8	45.1
0.1	27.3	2.2	55
0.22	60.0	4.8	121
0.33	90.1	7.2	181.5
0.47	128.3	10.2	258.5
0.68	185.6	14.7	374
0.82	223.8	17.8	451
1	272.9	21.7	550
2.2	600.5	47.7	1210
3.3	900.7	71.5	1815

Power-Off Cycle

The system can be reset by toggling the ON pin low for more than 30µs as shown at time point 7 of Figure 3. The GATE pin is pulled to ground. The TIMER pin is also discharged to ground. C_{LOAD} discharges through the load. Alternatively, the TIMER pin can be externally driven above the COMP2 threshold to turn off the GATE pin.

POWER MOSFET SELECTION

Power MOSFETs can be classified by R_{DSON} at V_{GS} gate drive ratings of 10V, 4.5V, 2.5V and 1.8V. Those rated for R_{DSON} at 10V V_{GS} usually have a higher V_{GS} absolute maximum rating than those at 4.5V and 2.5V. At low supply voltages, the LTC4210 can drive any MOSFET rated with 4.5V or 2.5V gate drive. For higher supply voltages up to 15V, the LTC4210 can drive any MOSFET rated with a 10V or 4.5V gate drive. At 15V, the LTC4210 can drive any MOSFET rated with 4.5V gate drive.

The selected MOSFET should fulfill two V_{GS} criteria:

1. Positive V_{GS} absolute maximum rating > LTC4210's maximum ΔV_{GATE}, and
2. Negative V_{GS} absolute maximum rating > supply voltage. The gate of the MOSFET can discharge faster than V_{OUT} when shutting down the MOSFET with a large C_{LOAD}.

If one of the conditions cannot be met, an external zener clamp shown on Figure 10a or Figure 10b can be used. The selection of R_G should be within the allowed LTC4210 package dissipation when discharging V_{OUT} via the zener clamp.

APPLICATIONS INFORMATION

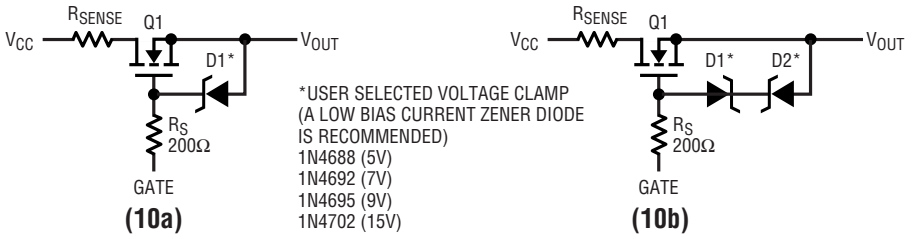


Figure 10. Gate Protection Zener Clamp

A MOSFET with a V_{GS} absolute maximum rating of ±20V meets the two criteria for all the LTC4210 applications ranges from 2.7V to 16.5V. Typically most 10V gate rated MOSFETs have V_{GS} absolute maximum ratings of ±20V or greater, so no external V_{GS} zener clamp is needed. There are 4.5V gate rated MOSFETs with V_{GS} absolute maximum ratings of ±20V.

In addition to the MOSFET gate drive rating and V_{GS} absolute maximum rating, other criteria such as V_{BDSS}, $I_{D(MAX)}$, $R_{DS(ON)}$, P_D, θ_{JA}, $T_{J(MAX)}$ and maximum safe operating area should also be carefully reviewed. V_{BDSS} should exceed the maximum supply voltage inclusive of spikes and ringing. $I_{D(MAX)}$ should be greater than the current limit, I_{LIMIT}. $R_{DS(ON)}$ determines the MOSFET V_{DS} which together with V_{CB} yields an error in the V_{OUT} voltage. At 2.7V supply voltage, the total of $V_{DS} + V_{CB}$ of 0.1V yields 3.7% V_{OUT} error.

The maximum power dissipated in the MOSFET is $I_{LIMIT}^2 \bullet R_{DS(ON)}$ and this should be less than the maximum power dissipation, P_D allowed in that package. Given power dissipation, the MOSFET junction temperature, T_J can be computed from the operating temperature (T_A) and the MOSFET package thermal resistance (θ_{JA}). The operating T_J should be less than the $T_{J(MAX)}$ specification.

Next review the short-circuit condition under maximum supply $V_{IN(MAX)}$ conditions and maximum current limit, $I_{LIMIT(MAX)}$ during the circuit breaker time-out interval of $t_{CBDELAY}$ with the maximum safe operating area of the MOSFET. The operation during output short-circuit conditions must be well within the manufacturer's recommended safe operating region with sufficient margin. To ensure a reliable design, fault tests should be evaluated in the laboratory.

V_{IN} TRANSIENT PROTECTION

Unlike most circuits, Hot Swap controllers typically are not allowed the good engineering practice of supply bypass capacitors, since controlling the surge current to bypass capacitors at plug-in is the primary motivation for the Hot Swap controller. Although wire harness, backplane and PCB trace inductances are usually small, these can create large spikes when large currents are suddenly drawn, cut-off or limited. This can cause detrimental damage to board components unless measures are taken. Abrupt intervention can prevent subsequent damage caused by a catastrophic fault but it does cause a large supply transient. The energy stored in the lead/trace inductance is easily controlled with snubbers and/or transient voltage suppressors. Even when ferrite beads are used for electromagnetic interference (EMI) control, the low saturating current of ferrite will not pose a major problem if the transient voltage suppressors with adequate ratings are used. The transient associated with the GATE turn off can be controlled with a snubber and/or transient voltage suppressor. Snubbers such as RC networks are effective especially at low voltage supplies. The choice of RC is usually determined experimentally. The value of the snubber capacitor is usually chosen between 10 to 100 times the MOSFET C_{OSS}. The value of the snubber resistor is typically between 3Ω to 100Ω. When the supply exceeds 7V or EMI beads exist in the wire harness, a transient voltage suppressor and snubber are recommended to clip off large spikes and reduce the ringing. For supply voltages of 6V or below, a snubber network should be sufficient to protect against transient voltages. In many cases, a simple short-circuit test can be performed to determine the need of the transient voltage suppressor.

APPLICATIONS INFORMATION

OVERVOLTAGE DETECTION USING THE TIMER PIN

Figure 11 shows a supply side overvoltage detection circuit. A zener diode, a diode and COMP2 threshold sets the overvoltage threshold. Resistor R_B biases the zener diode voltage. Diode D1 blocks forward current in the zener during start-up or output short-circuit. R_{TIMER} with C_{TIMER} sets the overload noise filter.

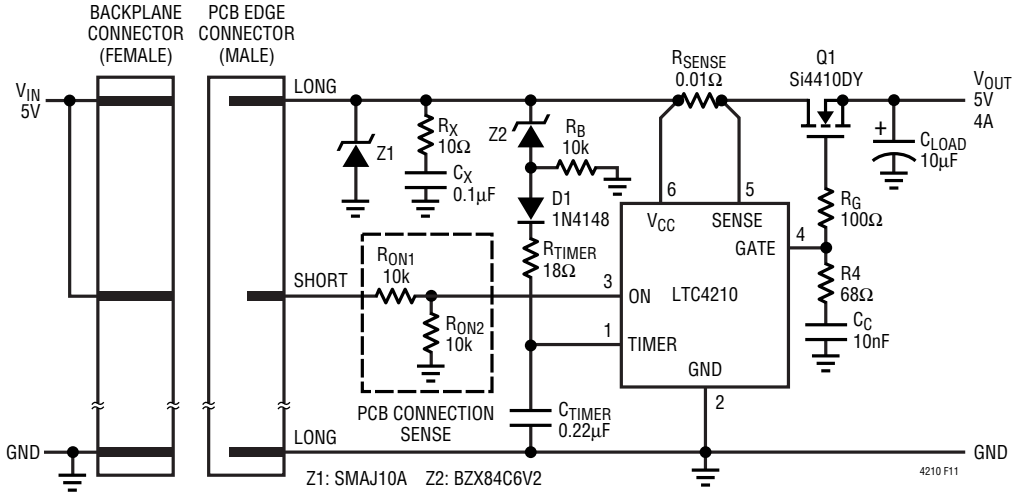


Figure 11. Supply Side Overvoltage Protection

APPENDIX

Table 2 lists some current sense resistors that can be used with the circuit breaker. Table 3 lists some power MOSFETs that are available. Table 4 lists the web sites of several manufacturers. Since this information is subject to change, please verify the part numbers with the manufacturer.

Table 2. Sense Resistor Selection Guide

CURRENT LIMIT VALUE	PART NUMBER	DESCRIPTION	MANUFACTURER
1A	LR120601R050	0.05Ω 0.5W 1% Resistor	IRC-TT
2A	LR120601R025	0.025Ω 0.5W 1% Resistor	IRC-TT
2.5A	LR120601R020	0.02Ω 0.5W 1% Resistor	IRC-TT
3.3A	WSL2512R015F	0.015Ω 1W 1% Resistor	Vishay-Dale
5A	LR251201R010F	0.01Ω 1.5W 1% Resistor	IRC-TT
10A	WSR2R005F	0.005Ω 2W 1% Resistor	Vishay-Dale

Table 3. N-Channel Selection Guide

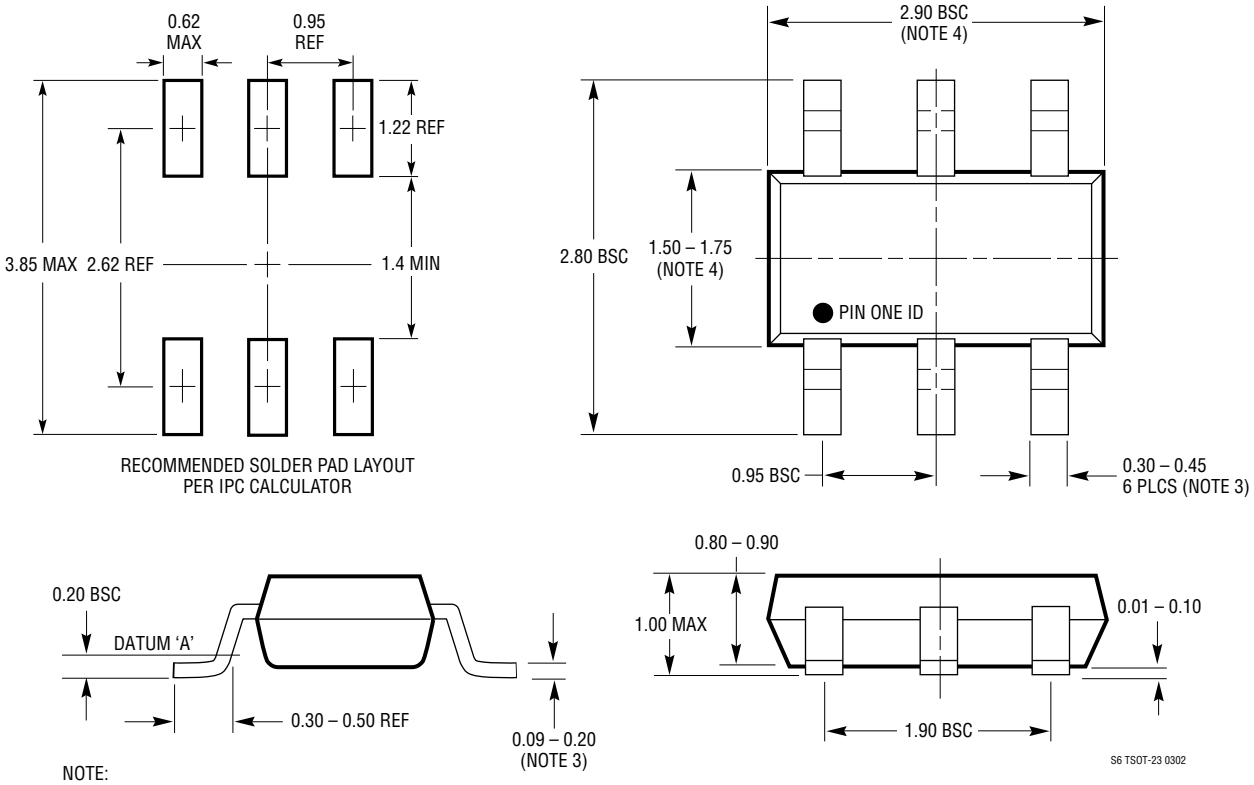
CURRENT LEVEL (A)	PART NUMBER	DESCRIPTION	MANUFACTURER
0 to 2	MMDF3N02HD	Dual N-Channel SO-8 $R_{DS(ON)}$ = 0.1Ω, C_{ISS} = 455pF	ON Semiconductor
2 to 5	MMSF5N02HD	Single N-Channel SO-8 $R_{DS(ON)}$ = 0.025Ω, C_{ISS} = 1130pF	ON Semiconductor
5 to 10	MTB50N06V	Single N-Channel DD Pak $R_{DS(ON)}$ = 0.028Ω, C_{ISS} = 1570pF	ON Semiconductor
10 to 20	MTB75N05HD	Single N-Channel DD Pak $R_{DS(ON)}$ = 0.0095Ω, C_{ISS} = 2600pF	ON Semiconductor

Table 4. Manufacturers' Web Sites

MANUFACTURER	WEB SITE
TEMIC Semiconductor	www.temic.com
International Rectifier	www.irf.com
ON Semiconductor	www.onsemi.com
Harris Semiconductor	www.semi.harris.com
IRC-TT	www.irctt.com
Vishay-Dale	www.vishay.com
Vishay-Siliconix	www.vishay.com
Diodes, Inc.	www.diodes.com

PACKAGE DESCRIPTION

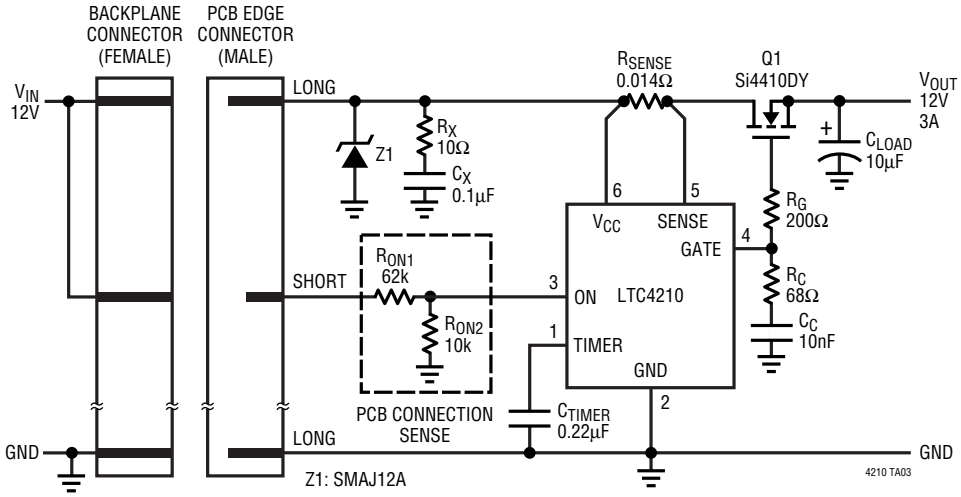
S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

TYPICAL APPLICATION

12V Hot Swap Application



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1421	Two Channel, Hot Swap Controller	Operates from 3V to 12V and Supports –12V
LTC1422	Single Channel, Hot Swap Controller in SO-8	Operates from 2.7V to 12V, Reset Output
LT1640AL/LT1640AH	Negative Voltage Hot Swap Controller in SO-8	Operates from –10V to –80V
LTC1642	Single Channel, Hot Swap Controller	Overvoltage Protection to 33V, Foldback Current Limiting
LTC1643AL/LTC1643AH	PCI Hot Swap Controller	3.3V, 5V, Internal FETs for ±12V
LTC1647	Dual Channel, Hot Swap Controller	Operates from 2.7V to 16.5V, Separate ON pins for Sequencing
LTC4211	Single Channel, Hot Swap Controller	2.5V to 16.5V, Multifunction Current Control
LTC4230	Triple Channel, Hot Swap Controller	1.7V to 16.5V, Multifunction Current Control
LTC4251	–48V Voltage Hot Swap Controller in SOT-23	Floating Supply, Three-Level Current Limiting
LTC4252	–48V Hot Swap Controller in MSOP	Floating Supply, Power Good, Three-Level Current Limiting
LTC4253	–48V Hot Swap Controller with Triple Supply Sequencing	Floating Supply, Three-Level Current Limiting

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