

LRS1370

Stacked Chip

16M (x16) Flash and 2M (x16) SRAM

(Model No.: LRS1370)

Spec No.: EL12Y030

Issue Date: November 10, 2000

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Contents

1. Description	2
2. Pin Configuration	3
3. Truth Table	5
4. Block Diagram	5
5. Command Definitions for Flash Memory	6
5.1 Command Definitions	6
5.2 Identifier Codes	7
5.3 Write Protection Alternatives	7
6. Status Register Definition	8
7. Memory Map for Flash Memory	9
8. Absolute Maximum Ratings	10
9. Recommended DC Operating Conditions	10
10. Pin Capacitance	10
11. DC Electrical Characteristics	11
12. AC Electrical Characteristics for Flash Memory	13
12.1 AC Test Conditions	13
12.2 Read Cycle	13
12.3 Write Cycle (F- \overline{WE} Controlled)	14
12.4 Write Cycle (F- \overline{CE} Controlled)	15
12.5 Block Erase, Full Chip Erase, Word Write and Lock-Bits Configuration Performance	16
12.6 Flash Memory AC Characteristics Timing Chart	17
12.7 Reset Operations	20
13. AC Electrical Characteristics for SRAM	21
13.1 AC Test Conditions	21
13.2 Read Cycle	21
13.3 Write Cycle	22
13.4 SRAM AC Characteristics Timing Chart	23
14. Data Retention Characteristics for SRAM	27
15. Notes	28
16. Flash Memory Data Protection	29
17. Design Considerations	30
18. Related Document Information	30
19. Package and Packing Specification	31

1. Description

The LRS1370 is a combination memory organized as $1,048,576 \times 16$ bit flash memory and $131,072 \times 16$ bit static RAM in one package.

Features

- | | | |
|--|---------|----------------|
| - Power supply | • • • • | 2.7V to 3.6V |
| - Operating temperature | • • • • | -25°C to +85°C |
| - Not designed or rated as radiation hardened | | |
| - 72 pin CSP (LCSP072-P-0811) plastic package | | |
| - Flash memory has P-type bulk silicon, and SRAM has P-type bulk silicon | | |

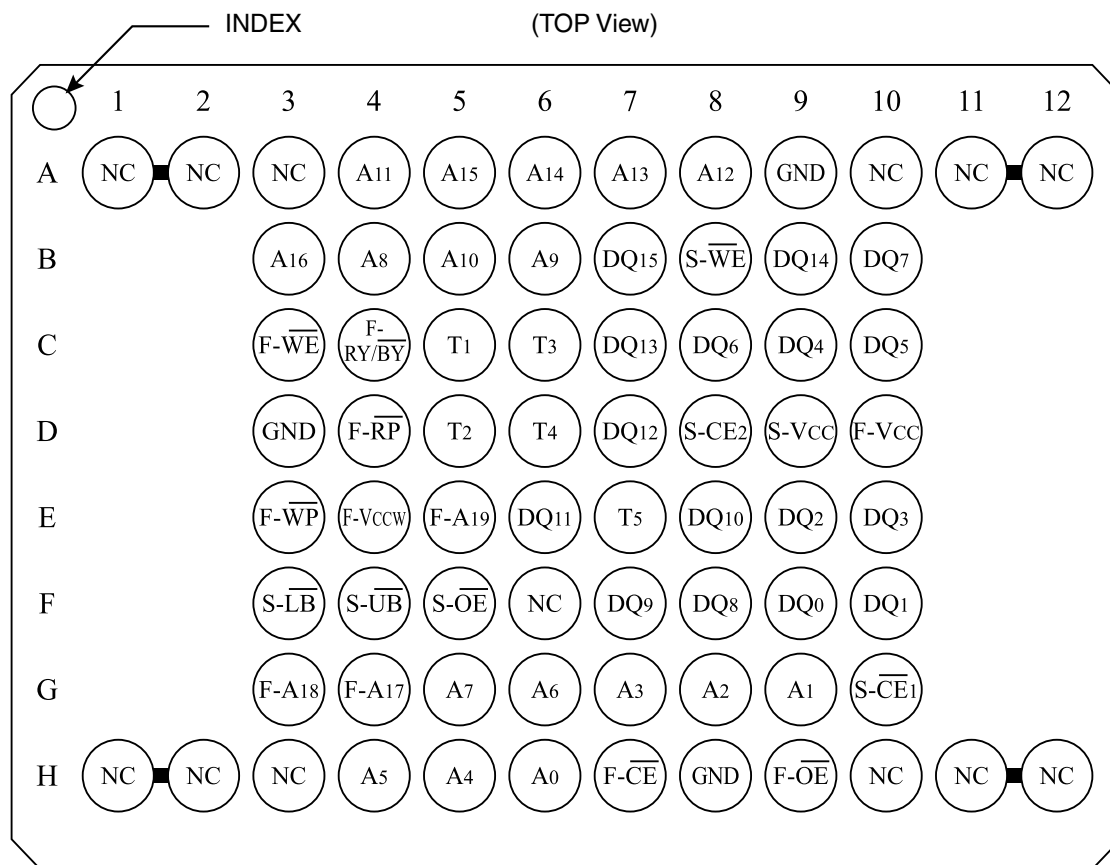
Flash Memory

- | | | | |
|---|---------|--------------------------------------|--|
| - Access Time | • • • • | 90 ns | (Max.) |
| - Power Supply current (The current for F-V _{CC} pin and F-V _{CCW} pin) | | | |
| Read | • • • • | 25 mA | (Max. t _{CYCLE} = 200ns, CMOS Input) |
| Word write | • • • • | 57 mA | (Max.) |
| Block erase | • • • • | 42 mA | (Max.) |
| Reset Power-Down | • • • • | 20 μA | (Max. F- \overline{RP} = GND ± 0.2V,
I _{OUT} (F-RY/ \overline{BY}) = 0mA) |
| Standby | • • • • | 30 μA | (Max. F- \overline{CE} = F- \overline{RP} = F-V _{CC} ± 0.2V) |
| - Optimized Array Blocking Architecture | | | |
| Two 4k-word Boot Blocks | | | |
| Six 4k-word Parameter Blocks | | | |
| Thirty-one 32k-word Main Blocks | | | |
| Bottom Boot Location | | | |
| - Extended Cycling Capability | | | |
| 100,000 Block Erase Cycles | | (F-V _{CCW} = 2.7 to 3.6V) | |
| 1,000 Block Erase Cycles and total 80 hours | | (F-V _{CCW} = 11.7 to 12.3V) | |
| - Enhanced Automated Suspend Options | | | |
| Word Write Suspend to Read | | | |
| Block Erase Suspend to Word Write | | | |
| Block Erase Suspend to Read | | | |

SRAM

- | | | | |
|------------------------|---------|------------|---|
| - Access Time | • • • • | 85 ns | (Max.) |
| - Power Supply current | | | |
| Operating current | • • • • | 45 mA | (Max. t_{RC}, t_{WC} = Min.) |
| | • • • • | 8 mA | (Max. t_{RC}, t_{WC} = 1 μ s, CMOS Input) |
| Standby current | • • • • | 10 μ A | (Max.) |
| Data retention current | • • • • | 10 μ A | (Max. $S-V_{CC}$ = 3.0V) |

2. Pin Configuration



Note) From T1 to T5 pins are needed to be open.
 Two NC pins at the corner are connected.
 Do not float any GND pins.

Pin	Description	Type
A ₀ to A ₁₆	Address Inputs (Common)	Input
F-A ₁₇ to F-A ₁₉	Address Inputs (Flash)	Input
F- $\overline{\text{CE}}$	Chip Enable Inputs (Flash)	Input
S- $\overline{\text{CE}}_1$, S- $\overline{\text{CE}}_2$	Chip Enable Inputs (SRAM)	Input
F- $\overline{\text{WE}}$	Write Enable Input (Flash)	Input
S- $\overline{\text{WE}}$	Write Enable Input (SRAM)	Input
F- $\overline{\text{OE}}$	Output Enable Input (Flash)	Input
S- $\overline{\text{OE}}$	Output Enable Input (SRAM)	Input
S- $\overline{\text{LB}}$	SRAM Byte Enable Input (DQ ₀ to DQ ₇)	Input
S- $\overline{\text{UB}}$	SRAM Byte Enable Input (DQ ₈ to DQ ₁₅)	Input
F- $\overline{\text{RP}}$	Reset Power Down Input (Flash) Block erase and Write : V _{IH} Read : V _{IH} Reset Power Down : V _{IL}	Input
F- $\overline{\text{WP}}$	Write Protect Input (Flash) Two Boot Blocks Locked : V _{IL}	Input
F-RY/ $\overline{\text{BY}}$	Ready/Busy Output (Flash) During an Erase or Write operation : V _{OL} Block Erase and Write Suspend : High-Z (High impedance)	Open Drain Output
DQ ₀ to DQ ₁₅	Data Inputs and Outputs (Common)	Input / Output
F-V _{CC}	Power Supply (Flash)	Power
S-V _{CC}	Power Supply (SRAM)	Power
F-V _{CCW}	Write, Erase Power Supply (Flash) Block Erase and Write : F-V _{CCW} = V _{CCWH1/2} All Blocks Locked : F-V _{CCW} < V _{CCWLK}	Power
GND	GND (Common)	Power
NC	Non Connection (Should be all open)	-
T ₁ to T ₅	Test pins (Should be all open)	-

3. Truth Table⁽¹⁾

Flash	SRAM	Notes	F- $\overline{\text{CE}}$	F- $\overline{\text{RP}}$	F- $\overline{\text{OE}}$	F- $\overline{\text{WE}}$	S- $\overline{\text{CE}}_1$	S-CE ₂	S- $\overline{\text{OE}}$	S- $\overline{\text{WE}}$	S- $\overline{\text{LB}}$	S- $\overline{\text{UB}}$	DQ ₀ to DQ ₁₅
Read	Standby	3,5	L	H	L	H	(6)		X	X	(6)		D _{OUT}
Output Disable		5			H								High-Z
Write		2,3,4,5			H								L
Standby	Read	5	H	H	X	X	L	H	L	H	(7)		
	Output Disable	5							H	H	X	X	High-Z
									X	X	H	H	
	Write	5							X	L	(7)		
Reset Power Down	Read	5	X	L	X	X	L	H	L	H	(7)		
	Output Disable	5							H	H	X	X	High-Z
									X	X	H	H	
	Write	5							X	L	(7)		
Standby	Standby	5	H	H	X	X	(6)		X	X	(6)		High-Z
Reset Power Down		5	X	L									

Notes:

1. L = V_{IL}, H = V_{IH}, X = H or L. Refer to DC Characteristics. High-Z = High impedance.
2. Command Writes involving block erase, full chip erase, word write, or lock-bit configuration are reliably executed when F-V_{CCW} = V_{CCWH1/2} and F-V_{CC} = 2.7V to 3.6V.
Block erase, full chip erase, word write, or lock-bit configuration with F-V_{CCW} < V_{CCWH1/2} (Min.) produce spurious results and should not be attempted.
3. Never hold F- $\overline{\text{OE}}$ low and F- $\overline{\text{WE}}$ low at the same timing.
4. Refer Section 5. Command Definitions for Flash Memory valid D_{IN} during a write operation.
5. F- $\overline{\text{WP}}$ set to V_{IL} or V_{IH}.

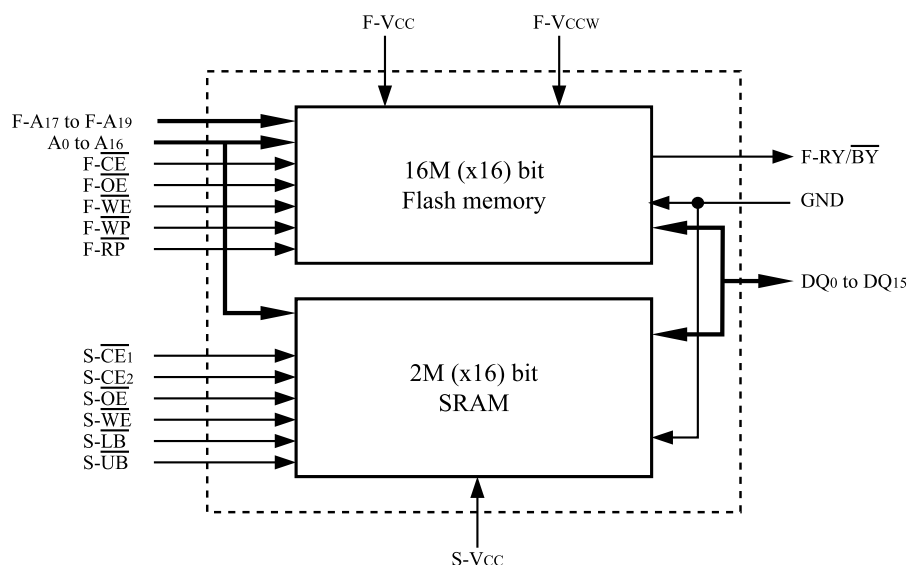
6. SRAM Standby Mode

S- $\overline{\text{CE}}_1$	S- CE_2	S- $\overline{\text{LB}}$	S- $\overline{\text{UB}}$
H	X	X	X
X	L	X	X
X	X	H	H

7. S- $\overline{\text{UB}}$, S- $\overline{\text{LB}}$ Control Mode

S- $\overline{\text{LB}}$	S- $\overline{\text{UB}}$	DQ ₀ to DQ ₇	DQ ₈ to DQ ₁₅
L	L	D _{OUT} /D _{IN}	D _{OUT} /D _{IN}
L	H	D _{OUT} /D _{IN}	High-Z
H	L	High-Z	D _{OUT} /D _{IN}

4. Block Diagram



5. Command Definitions for Flash Memory⁽¹⁾

5.1 Command Definitions

Command	Bus Cycles Required	Note	First Bus Cycle			Second Bus Cycle		
			Oper ⁽²⁾	Address ⁽³⁾	Data	Oper ⁽²⁾	Address ⁽³⁾	Data ⁽³⁾
Read Array / Reset	1		Write	XA	FFH			
Read Identifier Codes	≥ 2	4	Write	XA	90H	Read	IA	ID
Read Status Register	2		Write	XA	70H	Read	XA	SRD
Clear Status Register	1		Write	XA	50H			
Block Erase	2	5	Write	XA	20H	Write	BA	D0H
Full Chip Erase	2	5	Write	XA	30H	Write	XA	D0H
Word Write	2	5	Write	XA	40H or 10H	Write	WA	WD
Block Erase and Word Write Suspend	1	5,9	Write	XA	B0H			
Block Erase and Word Write Resume	1	5,9	Write	XA	D0H			
Set Block Lock Bit	2	7	Write	XA	60H	Write	BA	01H
Clear Block Lock Bits	2	6,7	Write	XA	60H	Write	XA	D0H
Set Permanent Lock Bit	2	8	Write	XA	60H	Write	XA	F1H

Notes:

- Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.
- Bus operations are defined in 3. Truth Table.
- XA = Any valid address within the device.
IA = Identifier code address.
BA = Address within the block being erased.
WA = Address of memory location to be written.
SRD = Data read from status register (See 6. Status Register Definition).
WD = Data to be written at location WA. Data is latched on the rising edge of F-WE or F-CE (whichever goes high first).
ID = Data read from identifier codes (See 5.2 Identifier Codes).
- See Identifier Codes at next page.
- See Write Protection Alternatives in section 5.3.
- The clear block lock-bits operation simultaneously clears all block lock-bits.
- If the permanent lock-bit is set, Set Block Lock-Bit and Clear Block Lock-Bits commands can not be done.
- Once the permanent lock-bit is set, it cannot be cleared.
- If the time between writing the Block Erase Resume command and writing the Block Erase Suspend command is shorter than 15ms and both commands are written repeatedly, a longer time is required than standard block erase until the completion of the operation.

5.2 Identifier Codes⁽³⁾

Codes	Address [A ₁₉ - A ₀]	Data [DQ ₁₅ - DQ ₀]
Manufacture Code	00000H	00B0H
Device Code	00001H	00E9H
Block Lock Configuration ⁽²⁾	BA ⁽¹⁾ + 2	DQ ₀ = 0 : Unlocked DQ ₀ = 1 : Locked
Permanent Lock Configuration ⁽²⁾	00003H	DQ ₀ = 0 : Unlocked DQ ₀ = 1 : Locked

Notes:

1. BA selects the specific block lock configuration code to be read.
2. DQ₁₅ - DQ₁ are reserved for future use.
3. Read Identifier Codes command is defined in 5.1 Command Definitions.

5.3 Write Protection Alternatives

Operation	F-V _{CCW}	F-RP	F-WP	Permanent Lock-Bit	Block Lock-Bit	Effect
Block Erase or Word Write	≤V _{CCWLK}	X	X	X	X	All Blocks Locked.
	>V _{CCWLK} ⁽¹⁾	V _{IL}	X	X	X	All Blocks Locked.
		V _{IH}	V _{IL}	X	0	2 Boot Blocks Locked.
			V _{IH}			Block Erase and Word Write Enabled.
			V _{IL}		1	Block Erase and Word Write Disabled.
			V _{IH}			Block Erase and Word Write Disabled.
Full Chip Erase	≤V _{CCWLK}	X	X	X	X	All Blocks Locked.
	>V _{CCWLK} ⁽¹⁾	V _{IL}	X	X	X	All Blocks Locked.
		V _{IH}	V _{IL}	X	X	All Unlocked Blocks are Erased. 2 Boot Blocks and Locked Blocks are Not Erased.
			V _{IH}			All Unlocked Blocks are Erased. Locked Blocks are Not Erased.
Set Block Lock-Bit	≤V _{CCWLK}	X	X	X	X	Set Block Lock-Bit Disabled.
	>V _{CCWLK} ⁽¹⁾	V _{IL}	X	X	X	Set Block Lock-Bit Disabled.
		V _{IH}	X	0	X	Set Block Lock-Bit Enabled.
			X	1	X	Set Block Lock-Bit Disabled.
Clear Block Lock-Bits	≤V _{CCWLK}	X	X	X	X	Clear Block Lock-Bits Disabled.
	>V _{CCWLK} ⁽¹⁾	V _{IL}	X	X	X	Clear Block Lock-Bits Disabled.
		V _{IH}	X	0	X	Clear Block Lock-Bits Enabled.
			X	1	X	Clear Block Lock-Bits Disabled.
Set Permanent Lock-Bit	≤V _{CCWLK}	X	X	X	X	Set Permanent Lock-Bit Disabled.
	>V _{CCWLK} ⁽¹⁾	V _{IL}	X	X	X	Set Permanent Lock-Bit Disabled.
		V _{IH}	X	X	X	Set Permanent Lock-Bit Enabled.

Note:

1. F-V_{CCW} is guaranteed only with the nominal voltages.

6. Status Register Definition

WSMS	BESS	ECBLBS	WWSLBS	VCCWS	WWSS	DPS	R
7	6	5	4	3	2	1	0
SR.7= WRITE STATE MACHINE STATUS (WSMS) 1= Ready 0= Busy SR.6= BLOCK ERASE SUSPEND STATUS (BESS) 1= Block Erase Suspended 0= Block Erase in Progress/Completed SR.5= ERASE AND CLEAR BLOCK LOCK-BITS STATUS (ECBLBS) 1= Error in Block Erase, Full Chip Erase or Clear Block Lock-Bits 0= Successful Block Erase, Full Chip Erase or Clear Block Lock-Bits SR.4= WORD WRITE AND SET LOCK-BIT STATUS (WWSLBS) 1= Error in Word Write or Set Block/Permanent Lock-Bit 0= Successful Word Write or Set Block/Permanent Lock-Bit SR.3= F-V _{CCW} STATUS (VCCWS) 1= F-V _{CCW} Low Detect, Operation Abort 0= F-V _{CCW} OK SR.2= WORD WRITE SUSPEND STATUS (WWSS) 1= Word Write Suspended 0= Word Write in Progress/Completed SR.1= DEVICE PROTECT STATUS (DPS) 1= Block Lock-Bit, Permanent Lock-Bit and/or F- \overline{WP} Lock Detected, Operation Abort 0= Unlocked SR.0= RESERVED FOR FUTURE ENHANCEMENTS (R)				Notes: Check SR.7 or F-RY/ \overline{BY} to determine Block Erase, Full Chip Erase, Word Write or Lock-Bit configuration completion. SR.6 - SR.0 are invalid while SR.7 = "0". If both SR.5 and SR.4 are "1"s after a Block Erase, Full Chip Erase or Lock-Bit configuration attempt, an improper command sequence was entered. SR.3 does not provide a continuous indication of F-V _{CCW} level. The WSM (Write State Machine) interrogates and indicates the F-V _{CCW} level only after Block Erase, Full Chip Erase, Word Write, or Lock-Bit Configuration command sequences. SR.3 is not guaranteed to reports accurate feedback only when F-V _{CCW} \neq V _{CCWH1/2} . SR.1 does not provide a continuous indication of permanent and block lock-bit and F- \overline{WP} values. The WSM interrogates the permanent lock-bit, block lock-bit and F- \overline{WP} only after Block Erase, Full Chip Erase, Word Write, or Lock-Bit Configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set, permanent lock-bit is set and/or F- \overline{WP} is V _{IL} . Reading the block lock and permanent lock configuration codes after writing the Read Identifier Codes command indicates permanent and block lock-bit status. SR.0 is reserved for future use and should be masked out when polling the status register.			

7. Memory Map for Flash Memory

Bottom Boot

[A19 ~ A0]

FFFF	32K-word Main Block 30
F8000	
F7FFF	32K-word Main Block 29
F0000	
FFFF	32K-word Main Block 28
E8000	
E7FFF	32K-word Main Block 27
E0000	
DFFFF	32K-word Main Block 26
D8000	
D7FFF	32K-word Main Block 25
D0000	
CFFFF	32K-word Main Block 24
C8000	
C7FFF	32K-word Main Block 23
C0000	
BFFFF	32K-word Main Block 22
B8000	
B7FFF	32K-word Main Block 21
B0000	
AFFFF	32K-word Main Block 20
A8000	
A7FFF	32K-word Main Block 19
A0000	
9FFFF	32K-word Main Block 18
98000	
97FFF	32K-word Main Block 17
90000	
8FFFF	32K-word Main Block 16
88000	
87FFF	32K-word Main Block 15
80000	
7FFFF	32K-word Main Block 14
78000	
77FFF	32K-word Main Block 13
70000	
6FFFF	32K-word Main Block 12
68000	
67FFF	32K-word Main Block 11
60000	
5FFFF	32K-word Main Block 10
58000	
57FFF	32K-word Main Block 9
50000	
4FFFF	32K-word Main Block 8
48000	
47FFF	32K-word Main Block 7
40000	
3FFFF	32K-word Main Block 6
38000	
37FFF	32K-word Main Block 5
30000	
2FFFF	32K-word Main Block 4
28000	
27FFF	32K-word Main Block 3
20000	
1FFFF	32K-word Main Block 2
18000	
17FFF	32K-word Main Block 1
10000	
0FFFF	32K-word Main Block 0
08000	
07FFF	4K-word Parameter Block 5
07000	
06FFF	4K-word Parameter Block 4
06000	
05FFF	4K-word Parameter Block 3
05000	
04FFF	4K-word Parameter Block 2
04000	
03FFF	4K-word Parameter Block 1
03000	
02FFF	4K-word Parameter Block 0
02000	
01FFF	4K-word Boot Block 1
01000	
00FFF	4K-word Boot Block 0
00000	

8. Absolute Maximum Ratings

Symbol	Parameter	Notes	Ratings	Unit
V_{CC}	Supply voltage	1,2	-0.2 to +4.6	V
V_{IN}	Input voltage	1,2,3,5	-0.2 to +3.9	V
T_A	Operating temperature		-25 to +85	°C
T_{STG}	Storage temperature		-65 to +125	°C
F- V_{CCW}	F- V_{CCW} voltage	1,3,4	-0.3 to +13.0	V

Notes:

1. The maximum applicable voltage on any pins with respect to GND.
2. Except F- V_{CCW} .
3. -1.0V undershoot and $V_{CC} + 1.0V$ overshoot are allowed when the pulse width is less than 20 nsec.
4. Applying $12V \pm 0.3V$ to F- V_{CCW} during erase/write can only be done for a maximum of 1000 cycles on each block. F- V_{CCW} may be connected to $12V \pm 0.3V$ for total of 80 hours maximum. +13.0V overshoot is allowed when the pulse width is less than 20nsec.
5. V_{IN} should not be over $V_{CC} + 0.3V$.

9. Recommended DC Operating Conditions

 $(T_A = -25^{\circ}C \text{ to } +85^{\circ}C)$

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	2	2.7	3.0	3.6	V
V_{IH}	Input Voltage	1	2.0		$V_{CC} + 0.2$	V
V_{IL}	Input Voltage		-0.2		0.4	V

Notes:

1. V_{CC} is the lower of F- V_{CC} or S- V_{CC} .
2. V_{CC} includes both F- V_{CC} and S- V_{CC} .

10. Pin Capacitance⁽¹⁾ $(T_A = 25^{\circ}C, f = 1MHz)$

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Condition
C_{IN}	Input capacitance				10	pF	$V_{IN} = 0V$
$C_{I/O}$	I/O capacitance				20	pF	$V_{I/O} = 0V$

Note:

1. Sampled but not 100% tested.

11. DC Electrical Characteristics⁽⁶⁾

DC Electrical Characteristics

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Notes	Min.	Typ. ⁽¹⁾	Max.	Unit	Conditions	
I _{LI}	Input Leakage Current				±1.5	μA	V _{IN} = V _{CC} or GND	
I _{LO}	Output Leakage Current				±1.5	μA	V _{OUT} = V _{CC} or GND	
I _{CCS}	F-V _{CC} Standby Current	4		2	15	μA	CMOS Input F- $\overline{\text{CE}}$ = F- $\overline{\text{RP}}$ = F-V _{CC} ± 0.2V	
				0.2	2	mA	TTL Input F- $\overline{\text{CE}}$ = F- $\overline{\text{RP}}$ = V _{IH}	
I _{CCAS}	F-V _{CC} Auto Power-Save Current	3,4		2	15	μA	CMOS Input F- $\overline{\text{CE}}$ = GND ± 0.2V	
I _{CCD}	F-V _{CC} Reset Power-Down Current	4		2	15	μA	F- $\overline{\text{RP}}$ = GND ± 0.2V I _{OUT} (F-RY/ $\overline{\text{BY}}$) = 0mA	
I _{CCR}	F-V _{CC} Read Current	4		15	25	mA	CMOS Input F- $\overline{\text{CE}}$ = GND, f = 5MHz, I _{OUT} = 0mA	
					30	mA	TTL Input F- $\overline{\text{CE}}$ = V _{IL} , f = 5MHz, I _{OUT} = 0mA	
I _{CCW}	F-V _{CC} Word Write or Set Lock-Bit Current	8		5	17	mA	F-V _{CCW} = V _{CCWH1}	
				5	12	mA	F-V _{CCW} = V _{CCWH2}	
I _{CCE}	F-V _{CC} Block Erase, Full Chip Erase or Clear Block Lock-Bits Current	8		4	17	mA	F-V _{CCW} = V _{CCWH1}	
				4	12	mA	F-V _{CCW} = V _{CCWH2}	
I _{CCWS} I _{CCES}	F-V _{CC} Word Write or Block Erase Suspend Current			1	6	mA	F- $\overline{\text{CE}}$ = V _{IH}	
I _{CCWS} I _{CCWR}	F-V _{CCW} Standby or Read Current	4		±2	±15	μA	F-V _{CCW} ≤ F-V _{CC}	
				10	200	μA	F-V _{CCW} > F-V _{CC}	
I _{CCWAS}	F-V _{CCW} Auto Power-Save Current	3,4		0.1	5	μA	CMOS Input F- $\overline{\text{CE}}$ = GND ± 0.2V	
I _{CCWD}	F-V _{CCW} Reset Power-Down Current	4		0.1	5	μA	F- $\overline{\text{RP}}$ = GND ± 0.2V	
I _{CCWW}	F-V _{CCW} Word Write or Set Lock-Bit Current	8		12	40	mA	F-V _{CCW} = V _{CCWH1}	
					30	mA	F-V _{CCW} = V _{CCWH2}	
I _{CCWE}	F-V _{CCW} Block Erase, Full Chip Erase or Clear Block Lock-Bits Current	8		8	25	mA	F-V _{CCW} = V _{CCWH1}	
					20	mA	F-V _{CCW} = V _{CCWH2}	
I _{CCWWS} I _{CCWES}	F-V _{CCW} Word Write or Block Erase Suspend Current			10	200	μA	F-V _{CCW} = V _{CCWH1/2}	
I _{SB}	S-V _{CC} Standby Current			0.5	10	μA	S- $\overline{\text{CE}}$ ₁ , S-CE ₂ ≥ S-V _{CC} - 0.2V or S-CE ₂ ≤ 0.2V	
I _{SB1}	S-V _{CC} Standby Current				3	mA	S- $\overline{\text{CE}}$ ₁ = V _{IH} or S-CE ₂ = V _{IL}	
I _{CC1}	S-V _{CC} Operation Current				45	mA	S- $\overline{\text{CE}}$ ₁ = V _{IL} , S-CE ₂ = V _{IH} V _{IN} = V _{IL} or V _{IH}	t _{CYCLE} =Min. I _{I/O} = 0mA
I _{CC2}	S-V _{CC} Operation Current				8	mA	S- $\overline{\text{CE}}$ ₁ = 0.2V, S-CE ₂ = SV _{CC} -0.2V, V _{IN} = S-V _{CC} -0.2V or 0.2V	t _{CYCLE} =1μA I _{I/O} = 0mA

DC Electrical Characteristics (Continue)

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Notes	Min.	Typ. ⁽¹⁾	Max.	Unit	Conditions
V _{IL}	Input Low Voltage	8	-0.2		0.4	V	
V _{IH}	Input High Voltage	8	2		V _{CC} +0.2	V	
V _{OL}	Output Low Voltage	2,8			0.4	V	I _{OL} = 0.5mA
V _{OH}	Output High Voltage	2,8	2			V	I _{OH} = -0.5mA
V _{CCWLK}	F-V _{CCW} Lockout during Normal Operations	5,8			1.5	V	
V _{CCWH1}	F-V _{CCW} during Block Erase, Full Chip Erase, Word Write, or Lock-Bit configuration Operations		2.7		3.6	V	
V _{CCWH2}	F-V _{CCW} during Block Erase, Full Chip Erase, Word Write, or Lock-Bit configuration Operations	7	11.7		12.3	V	
V _{LKO}	F-V _{CC} Lockout Voltage		2			V	

Notes:

1. All currents are in RMS unless otherwise noted. Reference values at V_{CC} = 3.0V and T_A = +25°C.
2. Includes F-RY/ $\overline{\text{BY}}$.
3. The Automatic Power Savings (APS) feature is placed automatically power save mode that addresses not switching more than 300ns while read mode.
4. CMOS inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL inputs are either V_{IL} or V_{IH}.
5. Block erases, full chip erase, word writes and lock-bits configurations are inhibited when F-V_{CCW} ≤ V_{CCWLK} and not guaranteed in the range between V_{CCWLK} (Max.) and V_{CCWH} (Min.), and above V_{CCWH} (Max.).
6. V_{CC} includes both F-V_{CC} and S-V_{CC}.
7. Applying V_{CCWH2} to F-V_{CCW} during erase/write can only be done for a maximum of 1000 cycles on each block. F-V_{CCW} may be connected to V_{CCWH2} for a total of 80 hours maximum.
8. Sampled, not 100% tested.

12. AC Electrical Characteristics for Flash Memory

12.1 AC Test Conditions

Input pulse level	0V to 2.7V
Input rise and fall time	10ns
Input and Output timing Ref. level	1.35V
Output load	1TTL + C _L (50pF)

12.2 Read Cycle

(T_A = -25°C to +85°C, F-V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t _{AVAV}	Read Cycle Time		90		ns
t _{AVQV}	Address to Output Delay			90	ns
t _{ELQV}	F- $\overline{\text{CE}}$ to Output Delay	1		90	ns
t _{PHQV}	F- $\overline{\text{RP}}$ High to Output Delay			600	ns
t _{GLQV}	F- $\overline{\text{OE}}$ to Output Delay	1		40	ns
t _{ELQX}	F- $\overline{\text{CE}}$ to Output in Low-Z		0		ns
t _{EHQZ}	F- $\overline{\text{CE}}$ High to Output in High-Z			40	ns
t _{GLQX}	F- $\overline{\text{OE}}$ to Output in Low-Z		0		ns
t _{GHQZ}	F- $\overline{\text{OE}}$ High to Output in High-Z			15	ns
t _{OH}	Output Hold form Address, F- $\overline{\text{CE}}$ or F- $\overline{\text{OE}}$ Change, Whichever Occurs First		0		ns

Note:

1. F- $\overline{\text{OE}}$ may be delayed up to t_{ELQV} - t_{GLQV} after the falling edge of F- $\overline{\text{CE}}$ without impact on t_{ELQV}.

12.3 Write Cycle (F- $\overline{\text{WE}}$ Controlled)^(1,5)(T_A = -25°C to +85°C, F-V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t _{AVAV}	Write Cycle Time		90		ns
t _{PHWL}	F- $\overline{\text{RP}}$ High Recovery to F- $\overline{\text{WE}}$ Going Low	2	1		μs
t _{ELWL}	F- $\overline{\text{CE}}$ Setup to F- $\overline{\text{WE}}$ Going Low		10		ns
t _{WLWH}	F- $\overline{\text{WE}}$ Pulse Width		50		ns
t _{SHWH}	F- $\overline{\text{WP}}$ V _{IH} Setup to F- $\overline{\text{WE}}$ Going High	2	100		ns
t _{VPWH}	F-V _{CCW} Setup to F- $\overline{\text{WE}}$ Going High	2	100		ns
t _{AVWH}	Address Setup to F- $\overline{\text{WE}}$ Going High	3	50		ns
t _{DVWH}	Data Setup to F- $\overline{\text{WE}}$ Going High	3	50		ns
t _{WHDX}	Data Hold from F- $\overline{\text{WE}}$ High		0		ns
t _{WHAX}	Address Hold from F- $\overline{\text{WE}}$ High		0		ns
t _{WHEH}	F- $\overline{\text{CE}}$ Hold from F- $\overline{\text{WE}}$ High		10		ns
t _{WHWL}	F- $\overline{\text{WE}}$ Pulse Width High		30		ns
t _{WHRL}	F- $\overline{\text{WE}}$ going High to F-RY/ $\overline{\text{BY}}$ Going Low			100	ns
t _{WHGL}	Write Recovery before Read		0		ns
t _{QVVL}	F-V _{CCW} Hold from Valid SRD, F-RY/ $\overline{\text{BY}}$ High-Z	2,4	0		ns
t _{QVSL}	F- $\overline{\text{WP}}$ V _{IH} Hold from Valid SRD, F-RY/ $\overline{\text{BY}}$ High-Z	2,4	0		ns

Notes:

1. Read timing characteristics during block erase, full chip erase, word write and lock-bit configurations are the same as during read-only operations. Refer to AC Characteristics for read cycle.
2. Sampled, not 100% tested.
3. Refer to Section 5. Command Definitions for Flash Memory for valid A_{IN} and D_{IN} for block erase, full chip erase, word write or lock-bit configuration.
4. F-V_{CC} should be held at V_{CCWH1/2} until determination of block erase, full chip erase, word write or lock-bit configuration success (SR.1/3/4/5 = 0).
5. It is written when F- $\overline{\text{CE}}$ and F- $\overline{\text{WE}}$ are active. The address and data needed to execute a command are latched on the rising edge of F- $\overline{\text{WE}}$ or F- $\overline{\text{CE}}$ (Whichever goes high first).

12.4 Write Cycle (F- $\overline{\text{CE}}$ Controlled)^(1,5)(T_A = -25°C to +85°C, F-V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t _{AVAV}	Write Cycle Time		90		ns
t _{PHEL}	F- $\overline{\text{RP}}$ High Recovery to F- $\overline{\text{CE}}$ Going Low	2	1		μs
t _{WLEL}	F- $\overline{\text{WE}}$ Setup to F- $\overline{\text{CE}}$ Going Low		0		ns
t _{ELEH}	F- $\overline{\text{CE}}$ Pulse Width		65		ns
t _{SHEH}	F- $\overline{\text{WP}}$ V _{IH} Setup to F- $\overline{\text{CE}}$ Going High	2	100		ns
t _{VPEH}	F-V _{CCW} Setup to F- $\overline{\text{CE}}$ Going High	2	100		ns
t _{AVEH}	Address Setup to F- $\overline{\text{CE}}$ Going High	3	50		ns
t _{DVEH}	Data Setup to F- $\overline{\text{CE}}$ Going High	3	50		ns
t _{EHDH}	Data Hold from F- $\overline{\text{CE}}$ High		0		ns
t _{EHAX}	Address Hold from F- $\overline{\text{CE}}$ High		0		ns
t _{EHWH}	F- $\overline{\text{WE}}$ Hold from F- $\overline{\text{CE}}$ High		0		ns
t _{EHEL}	F- $\overline{\text{CE}}$ Pulse Width High		25		ns
t _{EHRL}	F- $\overline{\text{CE}}$ going High to F-RY/ $\overline{\text{BY}}$ Going Low or SR.7 Going "0"			100	ns
t _{EHGL}	Write Recovery before Read		0		ns
t _{QVVL}	F-V _{CC} Hold from Valid SRD, F-RY/ $\overline{\text{BY}}$ High-Z	2,4	0		ns
t _{QVSL}	F- $\overline{\text{WP}}$ V _{IH} Hold from Valid SRD, F-RY/ $\overline{\text{BY}}$ High-Z	2,4	0		ns

Notes:

1. In systems where F- $\overline{\text{CE}}$ defines the write pulse width (within a longer F- $\overline{\text{WE}}$ timing waveform), all setup, hold and inactive F- $\overline{\text{WE}}$ times should be measured relative to the F- $\overline{\text{CE}}$ waveform.
2. Sampled, not 100% tested.
3. Refer to Section 5. Command Definitions for Flash Memory for valid A_{IN} and D_{IN} for block erase, full chip erase, word write or lock-bit configuration.
4. F-V_{CCW} should be held at V_{CCWH1/2} until determination of block erase, full chip erase, word write or lock-bit configuration success (SR.1/3/4/5=0).
5. It is written when F- $\overline{\text{CE}}$ and F- $\overline{\text{WE}}$ are active. The address and data needed to execute a command are latched on the rising edge of F- $\overline{\text{WE}}$ or F- $\overline{\text{CE}}$ (Whichever goes high first).

12.5 Block Erase, Full Chip Erase, Word Write and Block Lock-Bits Configuration Performance⁽³⁾(T_A = -25°C to +85°C, F-V_{CC} = 2.7V to 3.6V)

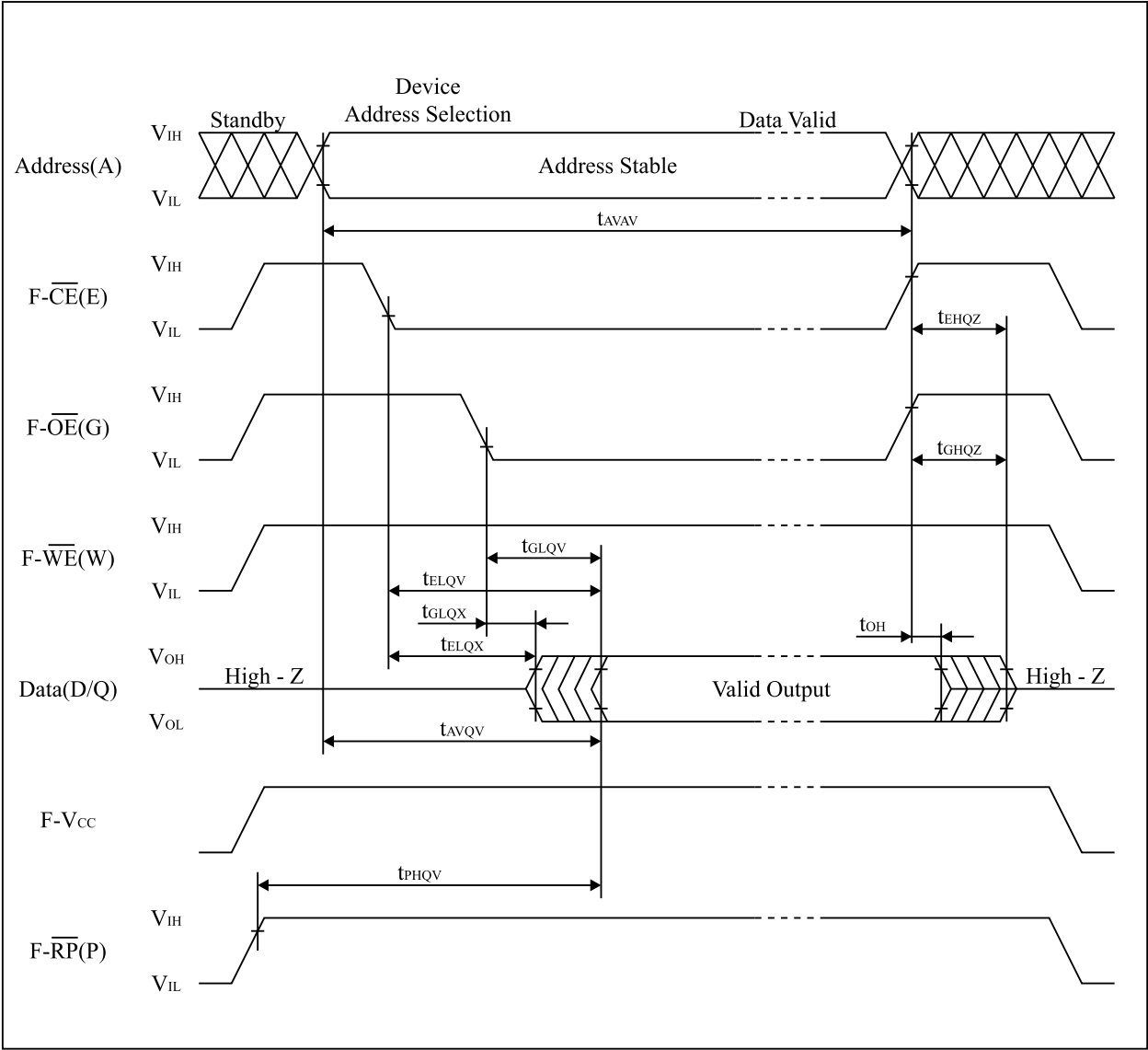
Symbol	Parameter		Notes	F-V _{CCW} = 2.7V to 3.6V		F-V _{CCW} = 11.7V to 12.3V		Unit
				Typ. ⁽¹⁾	Max.	Typ. ⁽¹⁾	Max.	
t _{WHQV1} t _{EHQV1}	Word Write Time	32K-Word Block	2	33	200	20		μs
		4K-Word Block	2	36	200	27		μs
	Block Write Time	32K-Word Block	2	1.1	4	0.66		s
		4K-Word Block	2	0.15	0.5	0.12		s
t _{WHQV2} t _{EHQV2}	Block Erase Time	32K-Word Block	2	1.2	6	0.9		s
		4K-Word Block	2	0.6	5	0.5		s
	Full Chip Erase Time		2	42	210	32		s
t _{WHQV3} t _{EHQV3}	Set Lock-Bit Time		2	56	200	42		μs
t _{WHQV4} t _{EHQV4}	Clear Block Lock-Bits Time		2	1	5	0.69		s
t _{WHRZ1} t _{EHRZ1}	Word Write Suspend Latency Time to Read		4	6	15	6	15	μs
t _{WHRZ2} t _{EHRZ2}	Erase Suspend Latency Time to Read		4	16	30	16	30	μs

Notes:

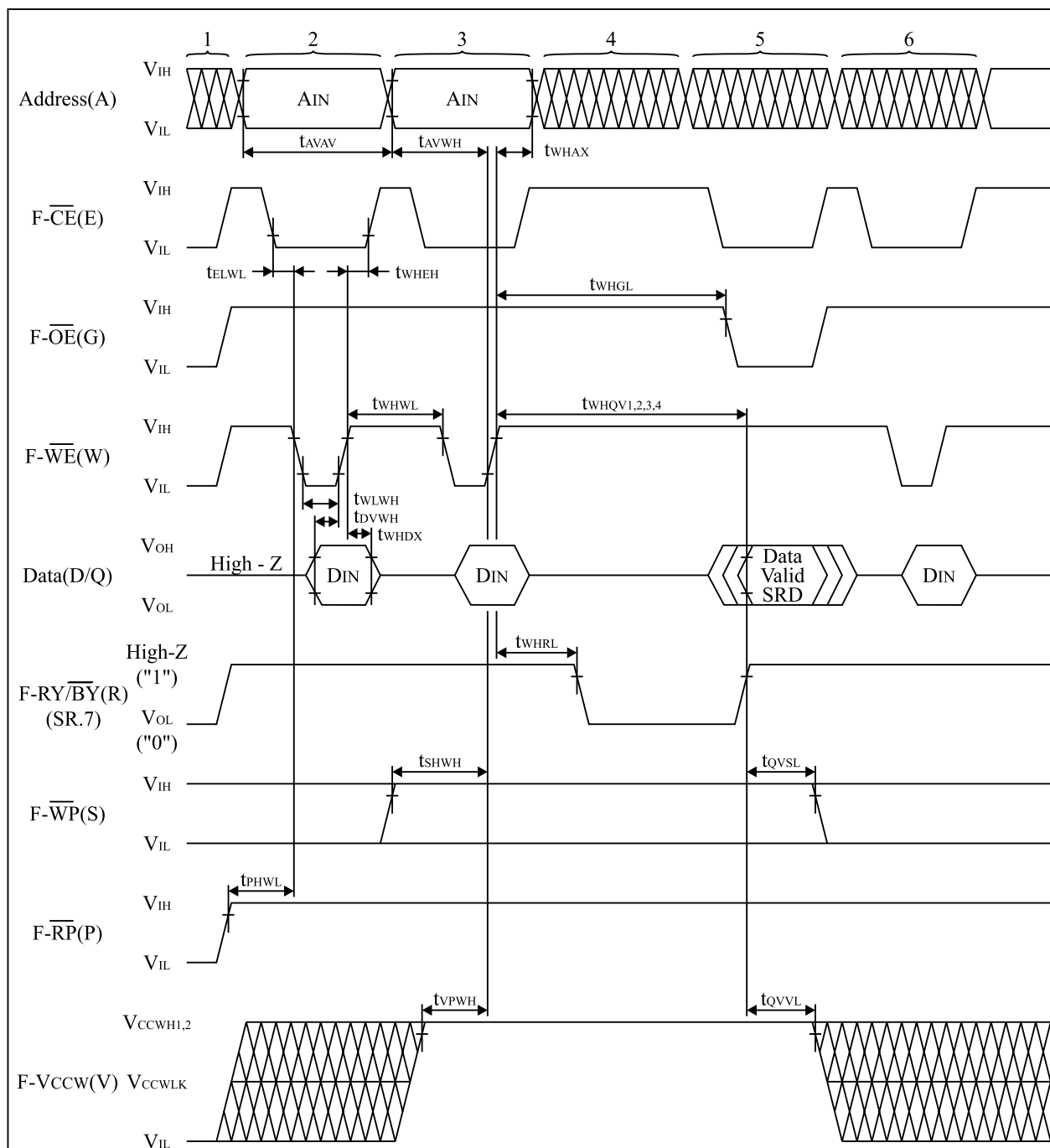
1. Reference values at T_A = +25°C and F-V_{CC} = 3.0V, F-V_{CCW} = 3.0V or 12.0V. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. Sampled, not 100% tested.
4. A Latency time is required from issuing suspend command (F- $\overline{\text{WE}}$ or F- $\overline{\text{CE}}$ going high) until F-RY/ $\overline{\text{BY}}$ going High-Z or SR.7 going “1”.

12.6 Flash Memory AC Characteristics Timing Chart

Read Cycle Timing Chart

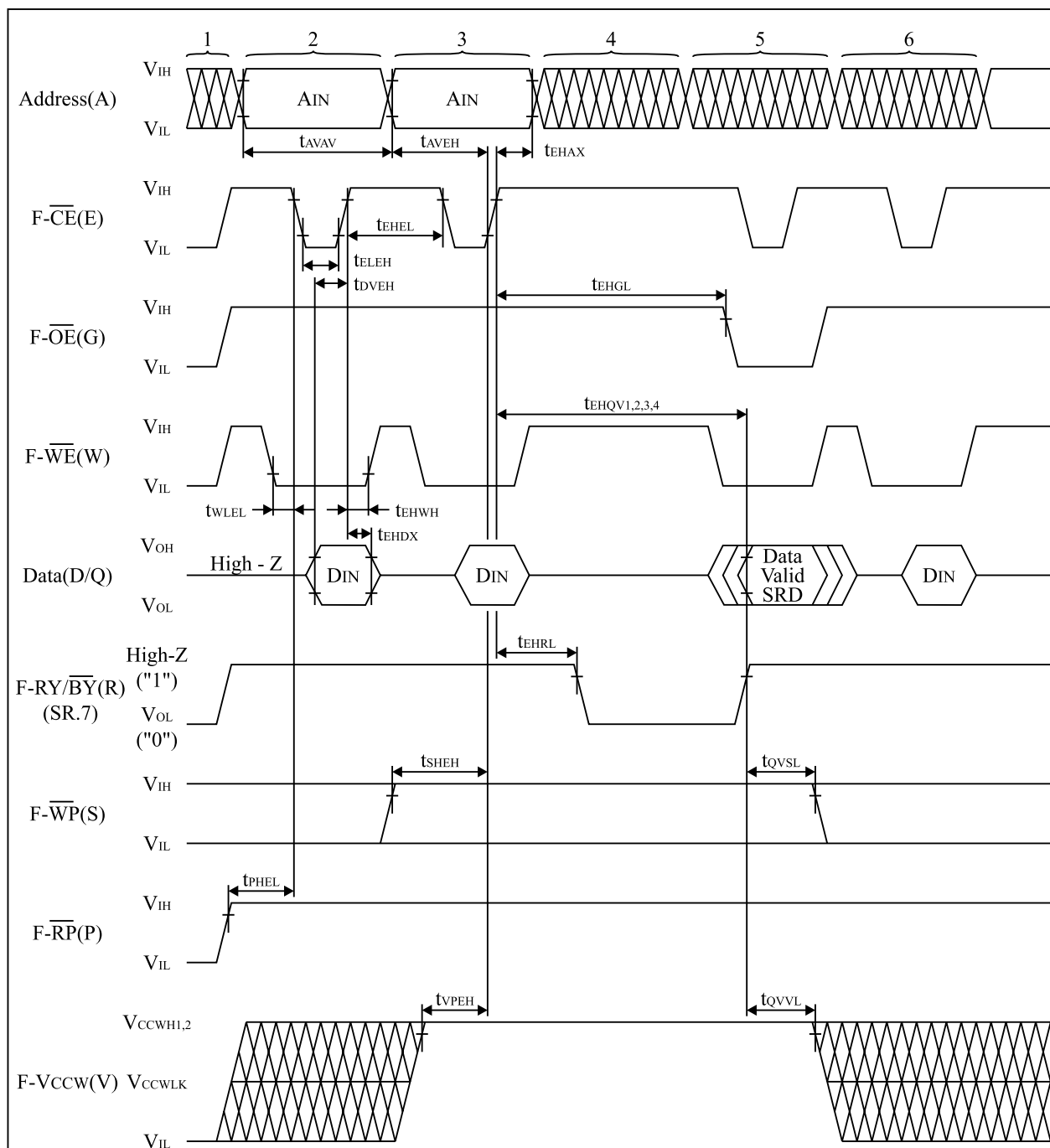


Write Cycle Timing Chart (F-WE Controlled)



Notes:

1. F-VCC power-up and standby.
2. Write each setup command.
3. Write each confirm command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

Write Cycle Timing Chart (F- $\overline{\text{CE}}$ Controlled)

Notes:

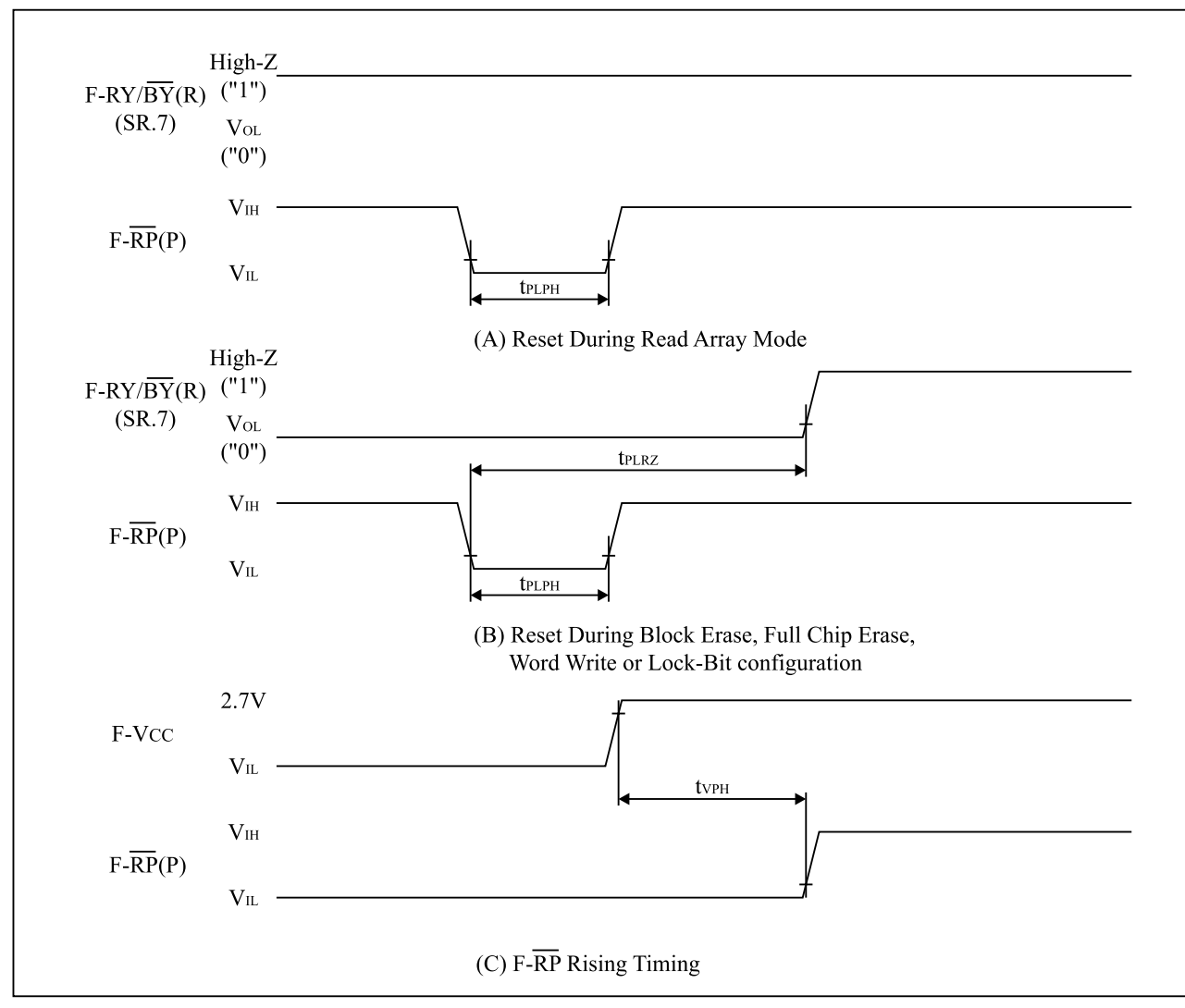
1. F-VCC power-up and standby.
2. Write each setup command.
3. Write each confirm command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

12.7 Reset Operations^(1,2)(T_A = -25°C to +85°C, F-V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t _{PLPH}	F- $\overline{\text{RP}}$ Pulse Low Time (If F- $\overline{\text{RP}}$ is tied to V _{CC} , this specification is not applicable.)		100		ns
t _{PLRZ}	F- $\overline{\text{RP}}$ Low to Reset during Block Erase, Full Chip Erase, Word Write or lock-bit configuration			30	μs
t _{VPH}	F-V _{CC} = 2.7V to F- $\overline{\text{RP}}$ High	3	100		ns

Notes:

1. If F- $\overline{\text{RP}}$ is asserted while a block erase, full chip erase, word write or lock-bit configuration operation is not executing, the reset will complete within 100ns.
2. A reset time, t_{PHQV}, is required from the later of F-RY/ $\overline{\text{BY}}$ (SR.7) going High-Z ("1") or F- $\overline{\text{RP}}$ going high until outputs are valid. Refer to AC Characteristics-Read Cycle for t_{PHQV}.
3. When the device power-up, holding F- $\overline{\text{RP}}$ low minimum 100ns is required after F-V_{CC} has been in predefined range and also has been in stable there.

AC Waveform for Reset Operation

13. AC Electrical Characteristics for SRAM

13.1 AC Test Conditions

Input pulse level	0.4V to 2.2V
Input rise and fall time	5ns
Input and Output timing Ref. level	1.5V
Output load	1TTL + C _L (30pF) ⁽¹⁾

Note:

1. Including scope and socket capacitance.

13.2 Read Cycle

(T_A = -25°C to +85°C, S-V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t _{RC}	Read Cycle Time		85		ns
t _{AA}	Address access time			85	ns
t _{ACE1}	Chip enable access time (S- $\overline{\text{CE}}_1$)			85	ns
t _{ACE2}	Chip enable access time (S-CE ₂)			85	ns
t _{BE}	Byte enable access time			85	ns
t _{OE}	Output enable to output valid			45	ns
t _{OH}	Output hold from address change		15		ns
t _{LZ1}	S- $\overline{\text{CE}}_1$ Low to output active	1	10		ns
t _{LZ2}	S-CE ₂ High to output active	1	10		ns
t _{OLZ}	S- $\overline{\text{OE}}$ Low to output active	1	5		ns
t _{BLZ}	S- $\overline{\text{UB}}$ or S- $\overline{\text{LB}}$ Low to output active	1	10		ns
t _{HZ1}	S- $\overline{\text{CE}}_1$ High to output in High-Z	1	0	25	ns
t _{HZ2}	S-CE ₂ Low to output in High-Z	1	0	25	ns
t _{OHZ}	S- $\overline{\text{OE}}$ High to output in High-Z	1	0	25	ns
t _{BHZ}	S- $\overline{\text{UB}}$ or S- $\overline{\text{LB}}$ High to output in High-Z	1	0	25	ns

Note:

1. Active output to High-Z and High-Z to output active tests specified for a $\pm 200\text{mV}$ transition from steady state levels into the test load.

13.3 Write Cycle

(T_A = -25°C to +85°C, S-V_{CC} = 2.7V to 3.6V)

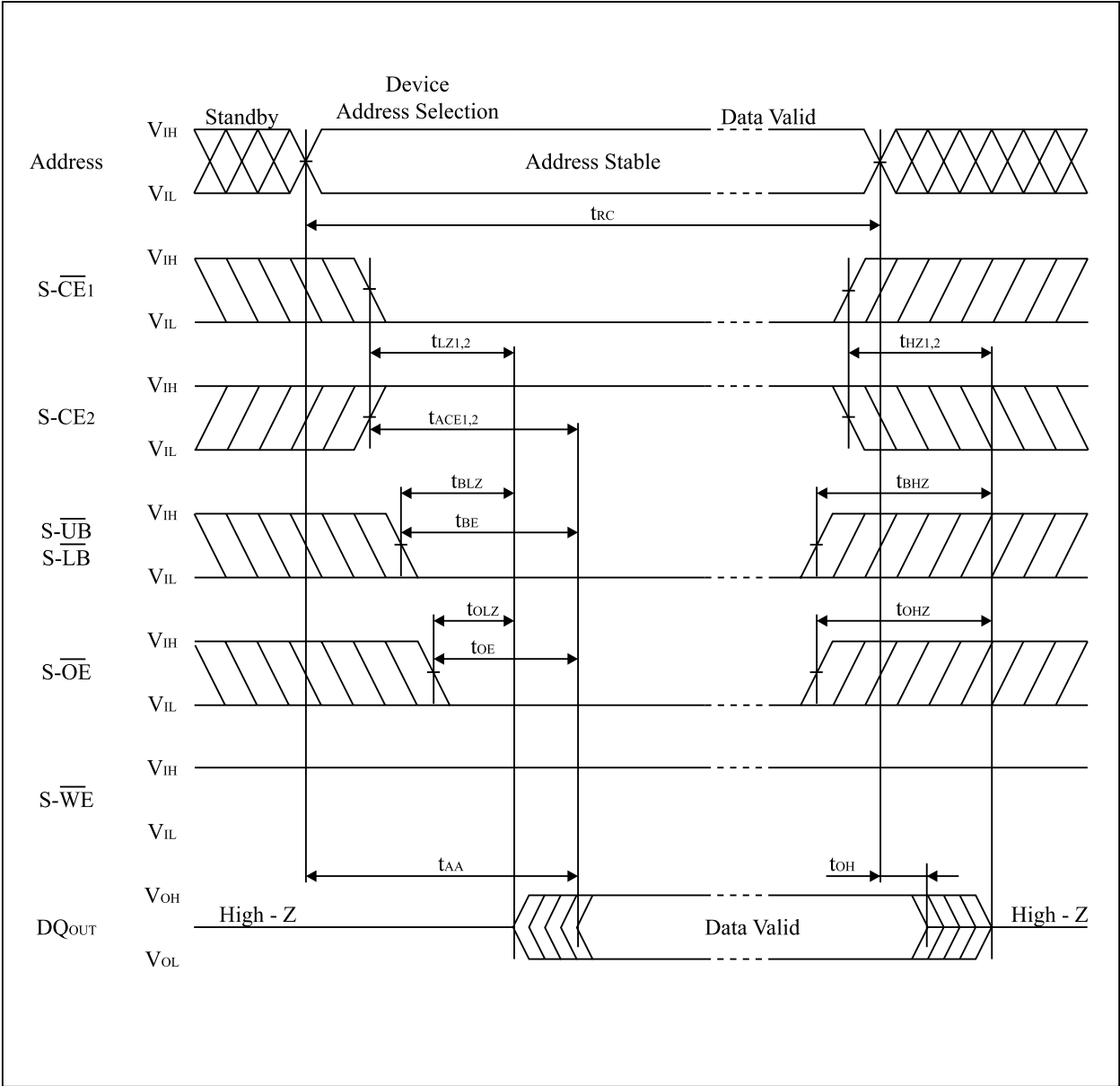
Symbol	Parameter	Notes	Min.	Max.	Unit
t _{WC}	Write cycle time		85		ns
t _{CW}	Chip enable to end of write		70		ns
t _{AW}	Address valid to end of write		70		ns
t _{BW}	Byte select time		70		ns
t _{AS}	Address setup time		0		ns
t _{WP}	Write pulse width		60		ns
t _{WR}	Write recovery time		0		ns
t _{DW}	Input data setup time		35		ns
t _{DH}	Input data hold time		0		ns
t _{OW}	S- $\overline{\text{WE}}$ High to output active	1	5		ns
t _{WZ}	S- $\overline{\text{WE}}$ Low to output in High-Z	1	0	25	ns

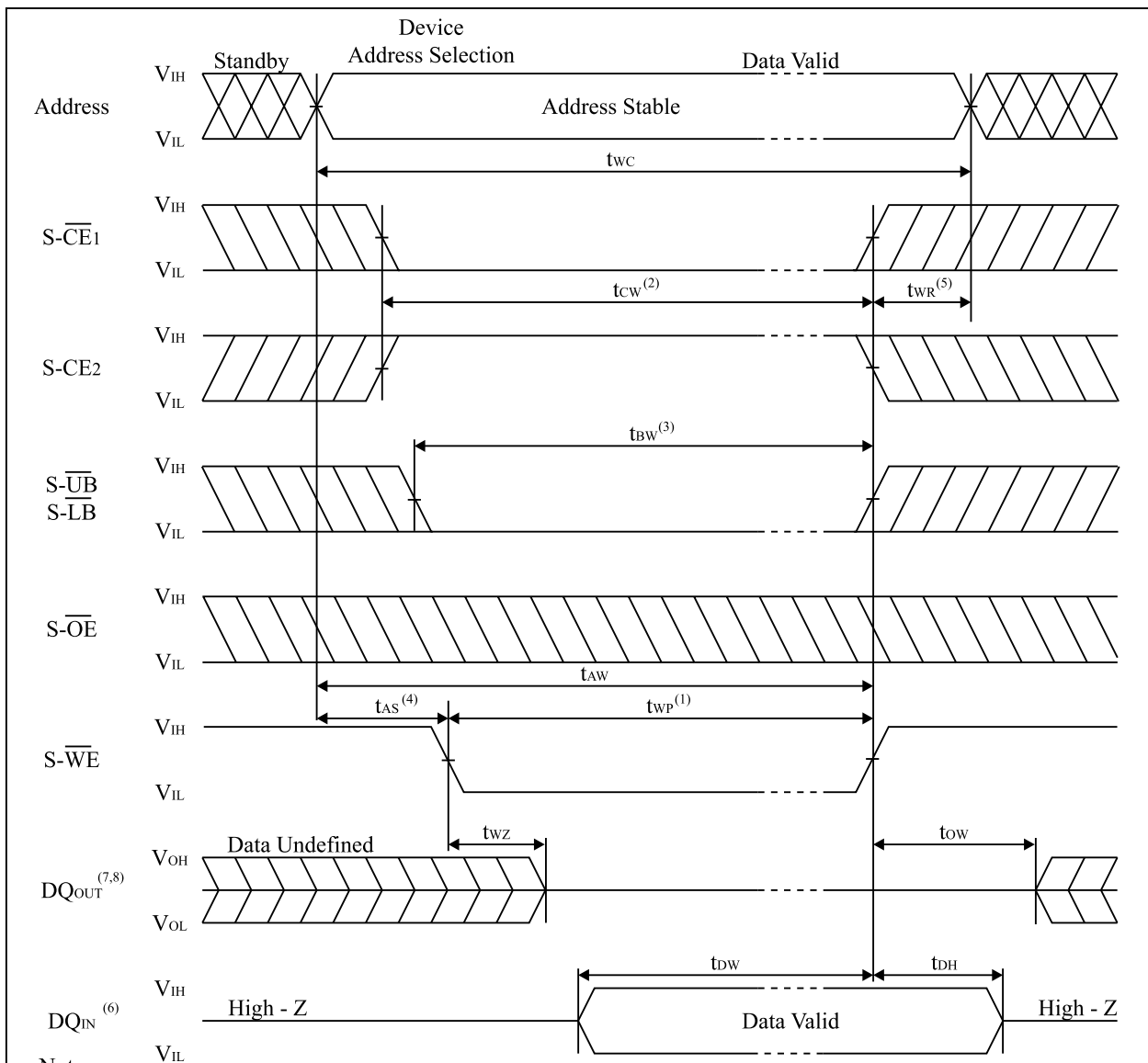
Note:

1. Active output to High-Z and High-Z to output active tests specified for a $\pm 200\text{mV}$ transition from steady state levels into the test load.

13.4 SRAM AC Characteristics Timing Chart

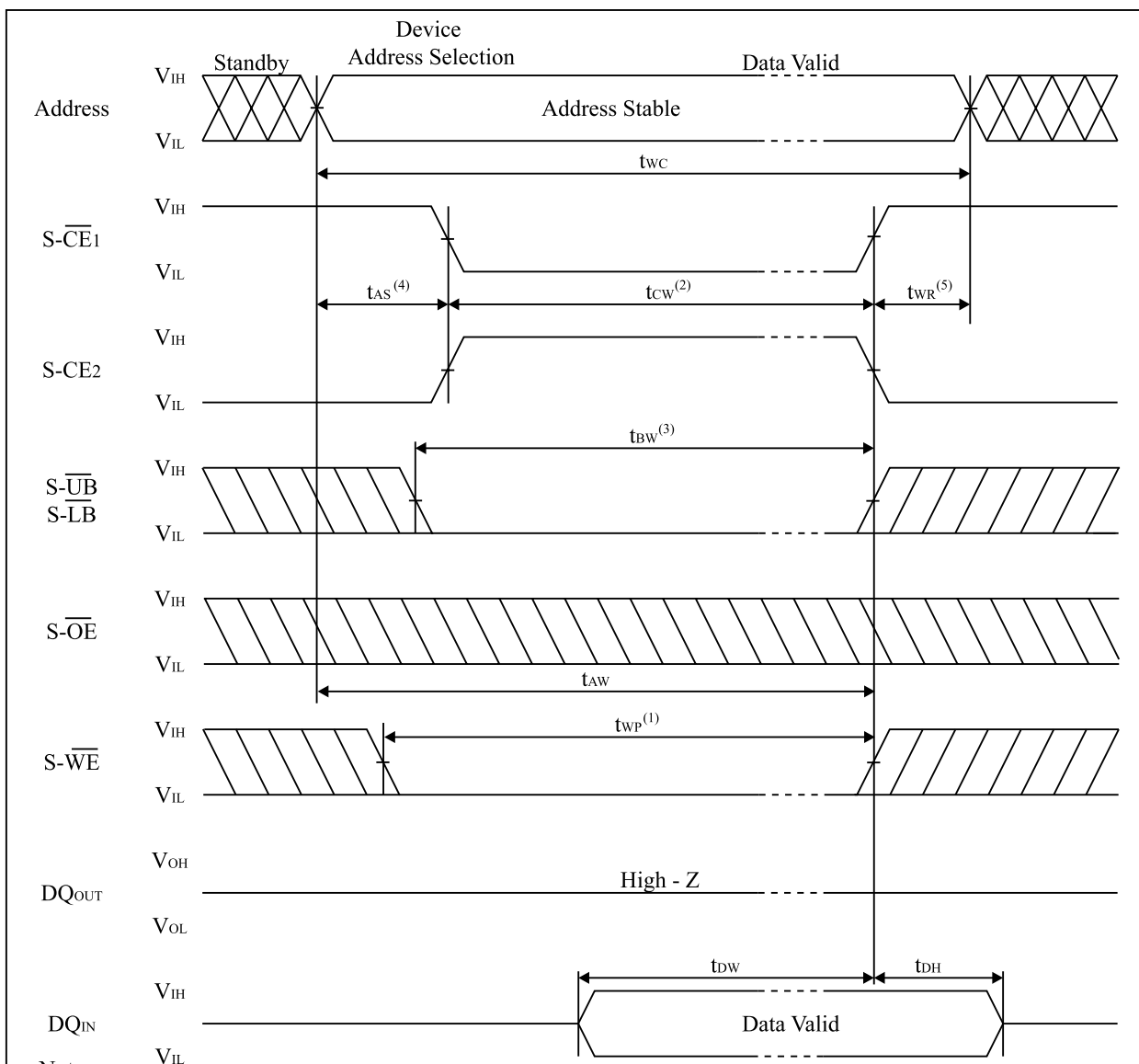
Read cycle timing chart



Write cycle timing chart (S- $\overline{\text{WE}}$ Controlled)

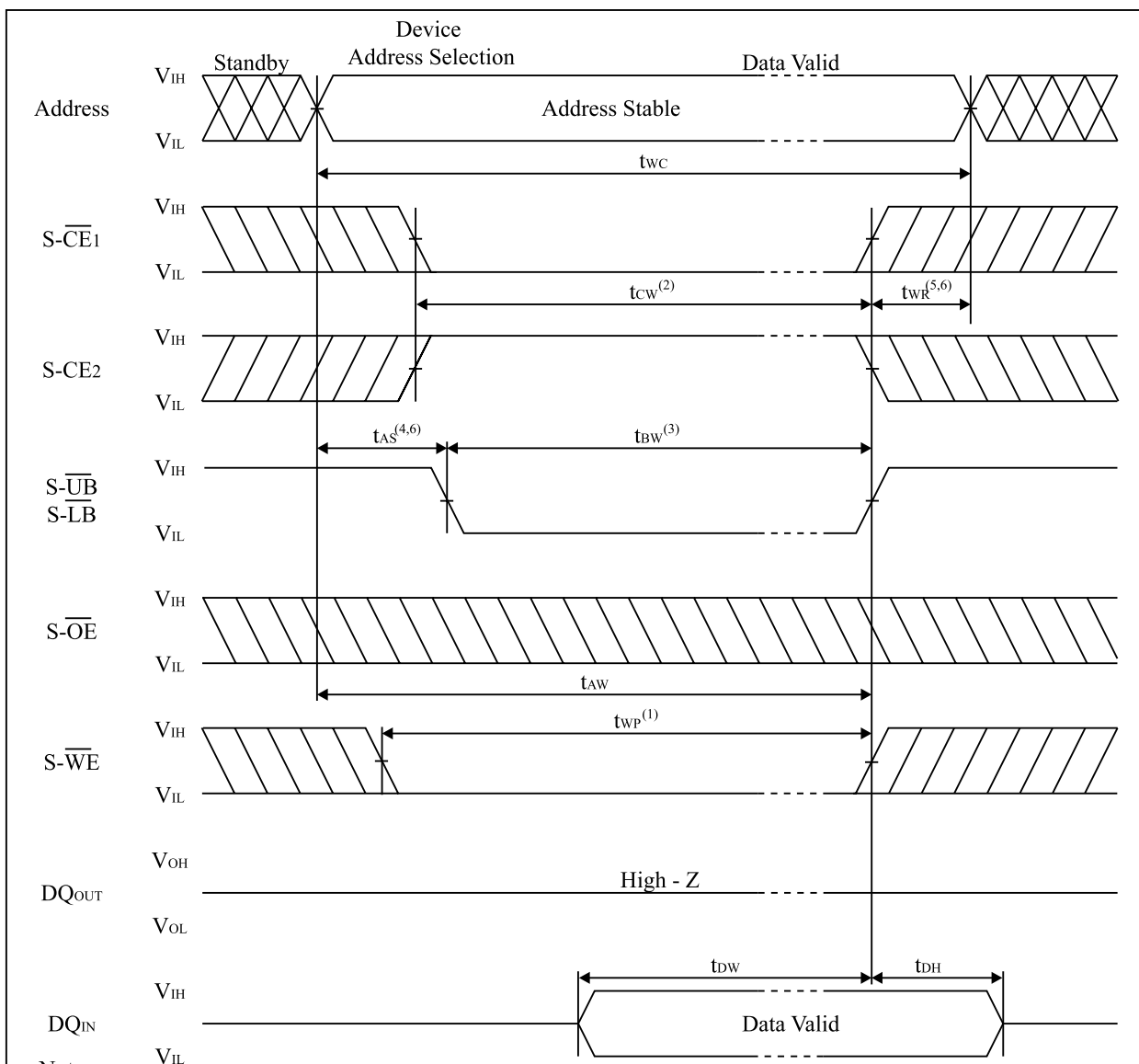
Notes:

1. A write occurs during the overlap of a low S- $\overline{\text{CE1}}$, a high S-CE2 and a low S- $\overline{\text{WE}}$.
A write begins at the latest transition among S- $\overline{\text{CE1}}$ going low, S-CE2 going high and S- $\overline{\text{WE}}$ going low.
A write ends at the earliest transition among S- $\overline{\text{CE1}}$ going high, S-CE2 going low and S- $\overline{\text{WE}}$ going high.
 t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of S- $\overline{\text{CE1}}$ going low or S-CE2 going high to the end of write.
3. t_{BW} is measured from the time of going low S- $\overline{\text{UB}}$ or low S- $\overline{\text{LB}}$ to the end of write.
4. t_{AS} is measured from the address valid to beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applies in case a write ends at S- $\overline{\text{CE1}}$ going high, S-CE2 going low or S- $\overline{\text{WE}}$ going high.
6. During this period DQ pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
7. If S- $\overline{\text{CE1}}$ goes low or S-CE2 goes high simultaneously with S- $\overline{\text{WE}}$ going low or after S- $\overline{\text{WE}}$ going low, the outputs remain in high impedance state.
8. If S- $\overline{\text{CE1}}$ goes high or S-CE2 goes low simultaneously with S- $\overline{\text{WE}}$ going high or before S- $\overline{\text{WE}}$ going high, the outputs remain in high impedance state.

Write cycle timing chart (S- $\overline{\text{CE}}$ Controlled)

Notes:

1. A write occurs during the overlap of a low S- $\overline{\text{CE}}$ 1, a high S-CE2 and a low S- $\overline{\text{WE}}$.
A write begins at the latest transition among S- $\overline{\text{CE}}$ 1 going low, S-CE2 going high and S- $\overline{\text{WE}}$ going low.
A write ends at the earliest transition among S- $\overline{\text{CE}}$ 1 going high, S-CE2 going low and S- $\overline{\text{WE}}$ going high.
 t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of S- $\overline{\text{CE}}$ 1 going low or S-CE2 going high to the end of write.
3. t_{BW} is measured from the time of going low S- $\overline{\text{UB}}$ or low S- $\overline{\text{LB}}$ to the end of write.
4. t_{AS} is measured from the address valid to beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applies in case a write ends at S- $\overline{\text{CE}}$ 1 going high, S-CE2 going low or S- $\overline{\text{WE}}$ going high.

Write cycle timing chart (S- $\overline{\text{UB}}$, S- $\overline{\text{LB}}$ Controlled)

Notes:

1. A write occurs during the overlap of a low S- $\overline{\text{CE1}}$, a high S-CE2 and a low S- $\overline{\text{WE}}$.
A write begins at the latest transition among S- $\overline{\text{CE1}}$ going low, S-CE2 going high and S- $\overline{\text{WE}}$ going low.
A write ends at the earliest transition among S- $\overline{\text{CE1}}$ going high, S-CE2 going low and S- $\overline{\text{WE}}$ going high.
 $t_{wp}^{(1)}$ is measured from the beginning of write to the end of write.
2. $t_{cw}^{(2)}$ is measured from the later of S- $\overline{\text{CE1}}$ going low or S-CE2 going high to the end of write.
3. $t_{bw}^{(3)}$ is measured from the time of going low S- $\overline{\text{UB}}$ or low S- $\overline{\text{LB}}$ to the end of write.
4. $t_{as}^{(4,6)}$ is measured from the address valid to beginning of write.
5. $t_{wr}^{(5,6)}$ is measured from the end of write to the address change. t_{wr} applies in case a write ends at S- $\overline{\text{CE1}}$ going high, S-CE2 going low or S- $\overline{\text{WE}}$ going high.
6. S- $\overline{\text{UB}}$ and S- $\overline{\text{LB}}$ need to make the time of start of a cycle, and an end "high" level for reservation of t_{as} and t_{wr} .

14. Data Retention Characteristics for SRAM

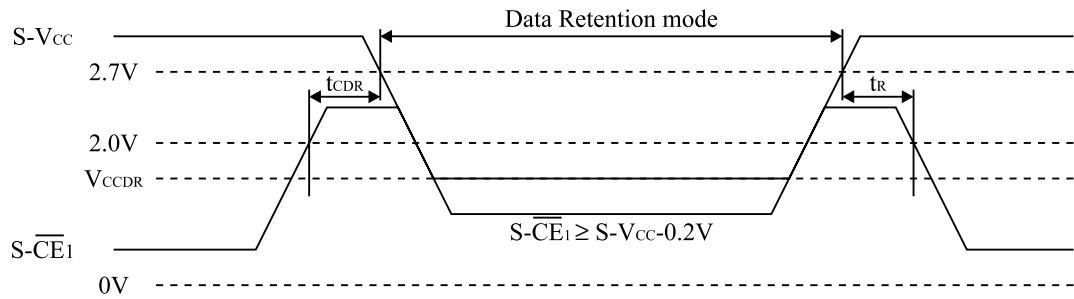
($T_A = -25^{\circ}\text{C}$ to $+85^{\circ}\text{C}$)

Symbol	Parameter	Note	Min.	Typ. ⁽¹⁾	Max.	Unit	Conditions
V_{CCDR}	Data Retention Supply voltage	2	1.5		3.6	V	$S\text{-CE}_2 \leq 0.2\text{V}$ or $S\text{-}\overline{\text{CE}}_1 \geq S\text{-}V_{CC} - 0.2\text{V}$
I_{CCDR}	Data Retention Supply current	2		0.5	10	μA	$S\text{-}V_{CC} = 3.0\text{V}$ $S\text{-CE}_2 \leq 0.2\text{V}$ or $S\text{-}\overline{\text{CE}}_1 \geq S\text{-}V_{CC} - 0.2\text{V}$
t_{CDR}	Chip enable setup time		0			ns	
t_R	Chip enable hold time		t_{RC}			ns	

Notes

1. Reference value at $T_A = 25^{\circ}\text{C}$, $S\text{-}V_{CC} = 3.0\text{V}$.
2. $S\text{-}\overline{\text{CE}}_1 \geq S\text{-}V_{CC} - 0.2\text{V}$, $S\text{-CE}_2 \geq S\text{-}V_{CC} - 0.2\text{V}$ ($S\text{-}\overline{\text{CE}}_1$ controlled) or $S\text{-CE}_2 \leq 0.2\text{V}$ ($S\text{-CE}_2$ controlled).

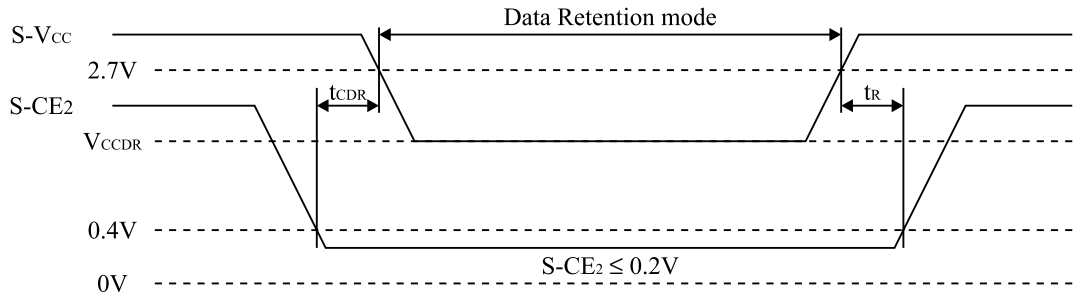
Data Retention timing chart ($S\text{-}\overline{\text{CE}}_1$ Controlled)⁽¹⁾



Note:

1. To control the data retention mode at $S\text{-}\overline{\text{CE}}_1$, fix the input level of $S\text{-CE}_2$ between V_{CCDR} and $V_{CCDR} - 0.2\text{V}$ or 0V or 0.2V and during the data retention mode.

Data Retention timing chart ($S\text{-CE}_2$ Controlled)



15. Notes

This product is a stacked CSP package that a 16M (x16) bit Flash Memory and a 2M (x16) bit SRAM are assembled into.

- Supply Power

Maximum difference (between F- V_{CC} and S- V_{CC}) of the voltage is less than 0.3V.

- Power Supply and Chip Enable of Flash Memory and SRAM

S- \overline{CE}_1 should not be “low” and S- CE_2 should not be “high” when F- \overline{CE} is “low” simultaneously.

If the two memories are active together, possibly they may not operate normally by interference noises or data collision on DQ bus.

Both F- V_{CC} and S- V_{CC} are needed to be applied by the recommended supply voltage at the same time expect SRAM data retention mode.

- Power Up Sequence

When turning on Flash memory power supply, keep F- \overline{RP} “low”. After F- V_{CC} reaches over 2.7V, keep F- \overline{RP} “low” for more than 100nsec.

- Device Decoupling

The power supply is needed to be designed carefully because one of the SRAM and the Flash Memory is in standby mode when the other is active. A careful decoupling of power supplies is necessary between SRAM and Flash Memory. Note peak current caused by transition of control signals (F- \overline{CE} , S- \overline{CE}_1 , S- CE_2).

16. Flash Memory Data Protection

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems. Such noises, when induced onto $F\text{-}\overline{WE}$ signal or power supply, may be interpreted as false commands, causing undesired memory updating. To protect the data stored in the flash memory against unwanted writing, systems operating with the flash memory should have the following write protect designs, as appropriate.

■ The below describes data protection method.

1. Protecting data in specific block

- By setting a $F\text{-}\overline{WP}$ to low, only the boot block can be protected against overwriting. Parameter and main blocks cannot be locked. System program, etc., can be locked by storing them in the boot block. For further information on setting/resetting of lock bit, and controlling of $F\text{-}\overline{WP}$ and $F\text{-}\overline{RP}$ refer to the specification. (See Chapter 5. Command Definitions for Flash Memory)

2. Data Protection through $F\text{-}V_{CCW}$

- When the level of $F\text{-}V_{CCW}$ is lower than V_{CCWLK} (lockout voltage), write operation on the flash memory is disabled. All blocks are locked and the data in the blocks are completely write protected. For the lockout voltage, refer to specification. (See Chapter 11. DC Electrical Characteristics)

■ Data Protection during voltage transition

1. Data protection thorough $F\text{-}\overline{RP}$

- When the $F\text{-}\overline{RP}$ is kept low during power up and power down sequence, write operation on the flash memory is disabled, write protecting all blocks.
- For the details of $F\text{-}\overline{RP}$ control, refer to the specification. (See Chapter 12. AC Electrical Characteristics for Flash Memory)

17. Design Considerations

1. Power Supply Decoupling

To avoid a bad effect to the system by flash memory power switching characteristics, each device should have a 0.1 μ F ceramic capacitor connected between its F-V_{CC} and GND and between its F-V_{CCW} and GND. Low inductance capacitors should be placed as close as possible to package leads.

2. F-V_{CCW} Trace on Printed Circuit Boards

Updating the memory contents of flash memories that reside in the target system requires that the printed circuit board designer pay attention to the F-V_{CCW} Power Supply trace. Use similar trace widths and layout considerations given to the F-V_{CC} power bus.

3. The Inhibition of Overwrite Operation

Please do not execute reprogramming “0” for the bit which has already been programed “0”. Overwrite operation may generate unerasable bit.

In case of reprogramming “0” to the data which has been programed “1”.

- Program “0” for the bit in which you want to change data from “1” to “0”.
- Program “1” for the bit which has already been programmed “0”.

For example, changing data from “1011110110111101” to “1010110110111100” requires “111011111111110” programming.

4. Power Supply

Block erase, full chip erase, word write and lock-bit configuration with an invalid F-V_{CCW} (See 11. DC Electrical Characteristics) produce spurious results and should not be attempted.

Device operations at invalid F-V_{CC} voltage (See Chapter 11. DC Electrical Characteristics) produce spurious results and should not be attempted.

18. Related Document Information⁽¹⁾

Document No.	Document Name
FUM99902	LH28F160BJ, LH28F320BJ Series Appendix

Note:

1. International customers should contact their local SHARP or distribution sales offices.

19 Package and packing specification

1.Storage Conditions.

1-1.Storage conditions required before opening the dry packing.

- Normal temperature : 5~40°C
- Normal humidity : 80% R.H. max.

1-2.Storage conditions required after opening the dry packing.

In order to prevent moisture absorption after opening, ensure the following storage conditions apply:

(1) Storage conditions for one-time soldering. (Convection reflow, IR/Convection reflow)

- Temperature : 5~25°C
- Humidity : 60% R.H. max.
- Period : 36 hours max. after opening.

(2) Storage conditions for two-time soldering. (Convection reflow, IR/Convection reflow.)

a. Storage conditions following opening and prior to performing the 1st reflow.

- Temperature : 5~25°C.
- Humidity : 60% R.H. max.
- Period : 36 hours max. after opening.

b. Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow.

- Temperature : 5~25°C.
- Humidity : 60% R.H. max.
- Period : 36 hours max. after completion of the 1st reflow.

1-3.Temporary storage after opening.

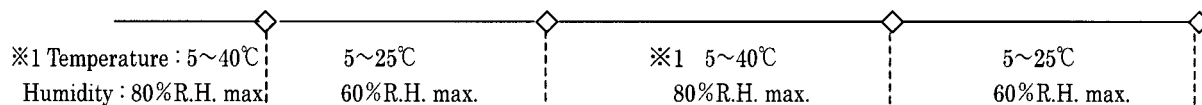
To re-store the devices before soldering, do so only once and use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using heat-sealing.

The storage period, temperature and humidity must be as follows :

(1) Storage temperature and humidity.

※1 : External atmosphere temperature and humidity of the dry packing.

First opening ← X1 → Re-sealing ← Y → Re-opening ← X2 → Mounting



(2) Storage period.

- X1 + X2 : Refer to Section 1-2(1) and (2)a , depending on the mounting method.
- Y : Two weeks max.

2. Baking Condition.

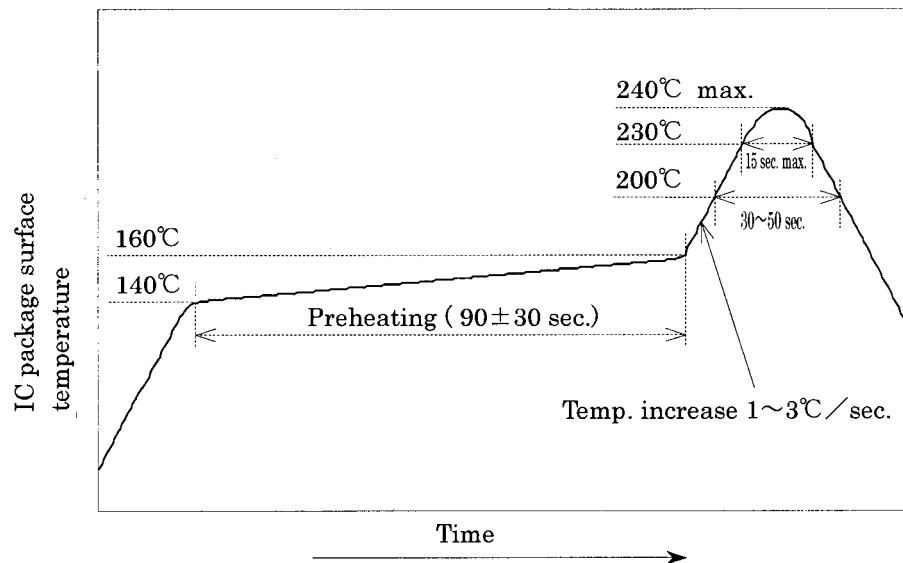
- (1) Situations requiring baking before mounting.
 - Storage conditions exceed the limits specified in Section 1-2 or 1-3.
 - Humidity indicator in the desiccant was already pink when opened.
(Also for re-opening.)
- (2) Recommended baking conditions.
 - Baking temperature and period :
120+10/-0°C for 1~3 hours.
 - The above baking conditions apply since the trays are heat-resistant.
- (3) Storage after baking.
 - After baking, store the devices in the environment specified in Section 1-2 and mount immediately.

3. Surface mount conditions.

The following soldering condition are recommended to ensure device quality.

3-1. Soldering.

- (1) Convection reflow or IR/Convection. (one-time soldering or two-time soldering)
 - Temperature and period :
 - Peak temperature of 240°C max., above 230°C for 15 sec. max.
 - Above 200°C for 30~50 sec.
 - Preheat temperature of 140~160°C for 90±30 sec.
 - Temperature increase rate of 1~3°C/sec.
 - Measuring point : IC package surface.
 - Temperature profile :



4. Condition for removal of residual flux.

- (1) Ultrasonic washing power : 25 watts / liter max.
- (2) Washing time : Total 1 minute max.
- (3) Solvent temperature : 15~40°C

5. Package outline specification.

Due to the different manufacturing process, there are tow types of package outline. (see *1)
No changes are planned on package structure, substrate, and quality or reliability level
remains unchanges. Refer to the attached drawing.

6. Markings.

6-1. Marking details. (The information on the package should be given as follows.)

(1) Product name : LRS1370

(2) Company name : S

(3) Date code

(Example) YY WW XXX

→ Denotes the production ref. code (1~3 digits).

→ Denotes the production week. (01 · 02 · ~ · 52 · 53)

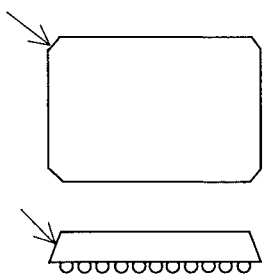
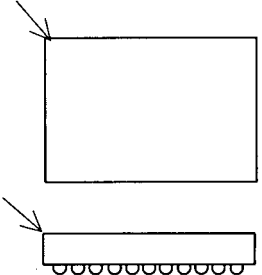
→ Denotes the production year. (Last two digits of the year.)

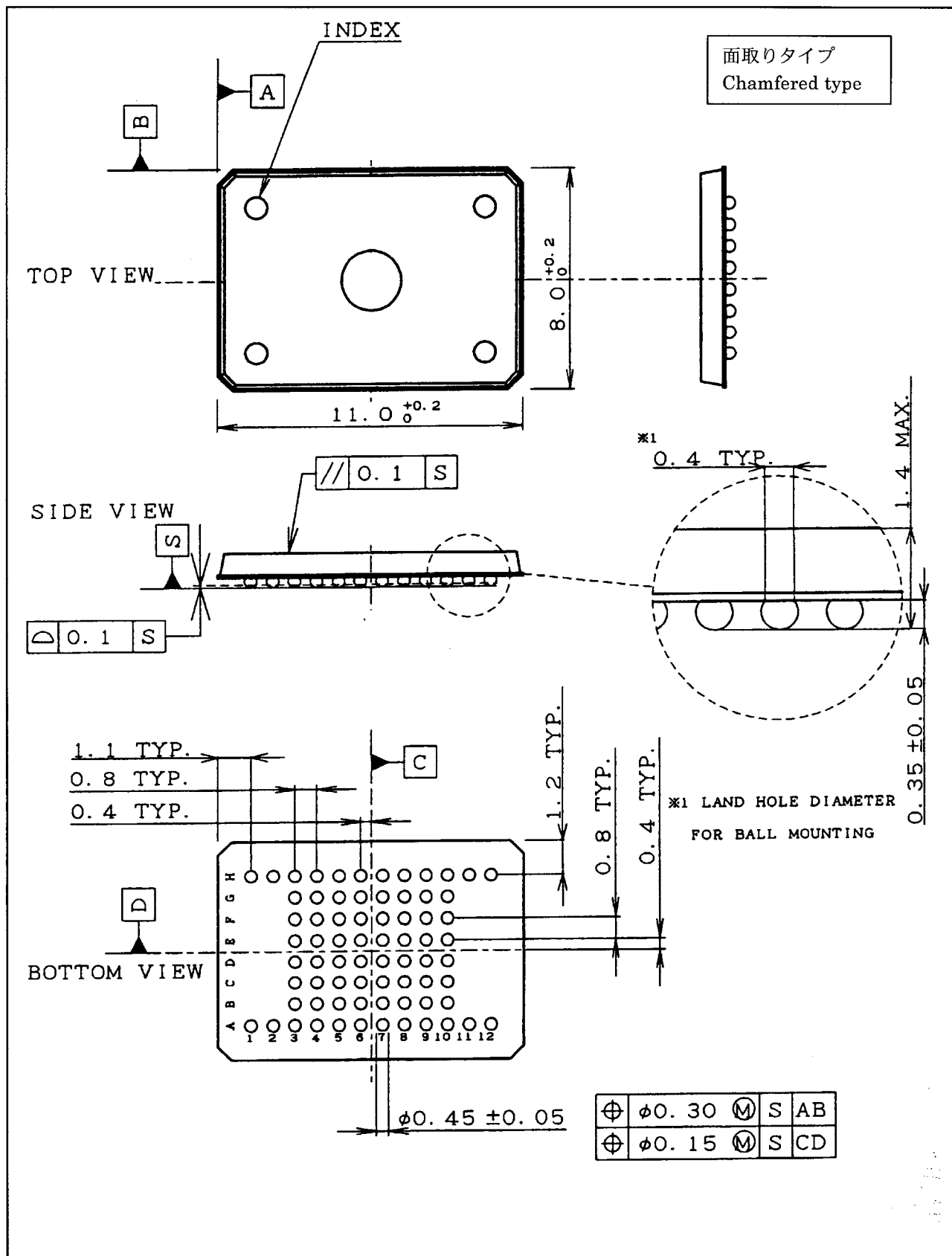
6-2. Marking layout.

The layout is shown in the attached drawing.

(However, this layout does not specify the size of the marking character and marking position.)

*1 Package outline

Item	Chamfered type	Rectangle type
Manufacturing Process	Devices are encapsulated separately, the cut into individual units by tool.	Multiple devices are encapsulated together, then cut into individual units by saw.
Drawing No.	AA2078	AA2149
Package outline		
Package index mark	Ejector pin mark.	Ink mark.
The word of "BATCH" is printed on the packing label	Not printed	Printed



名称

NAME FBGA072/064-P-0811 (LCSP072/064-P-0811)

備考

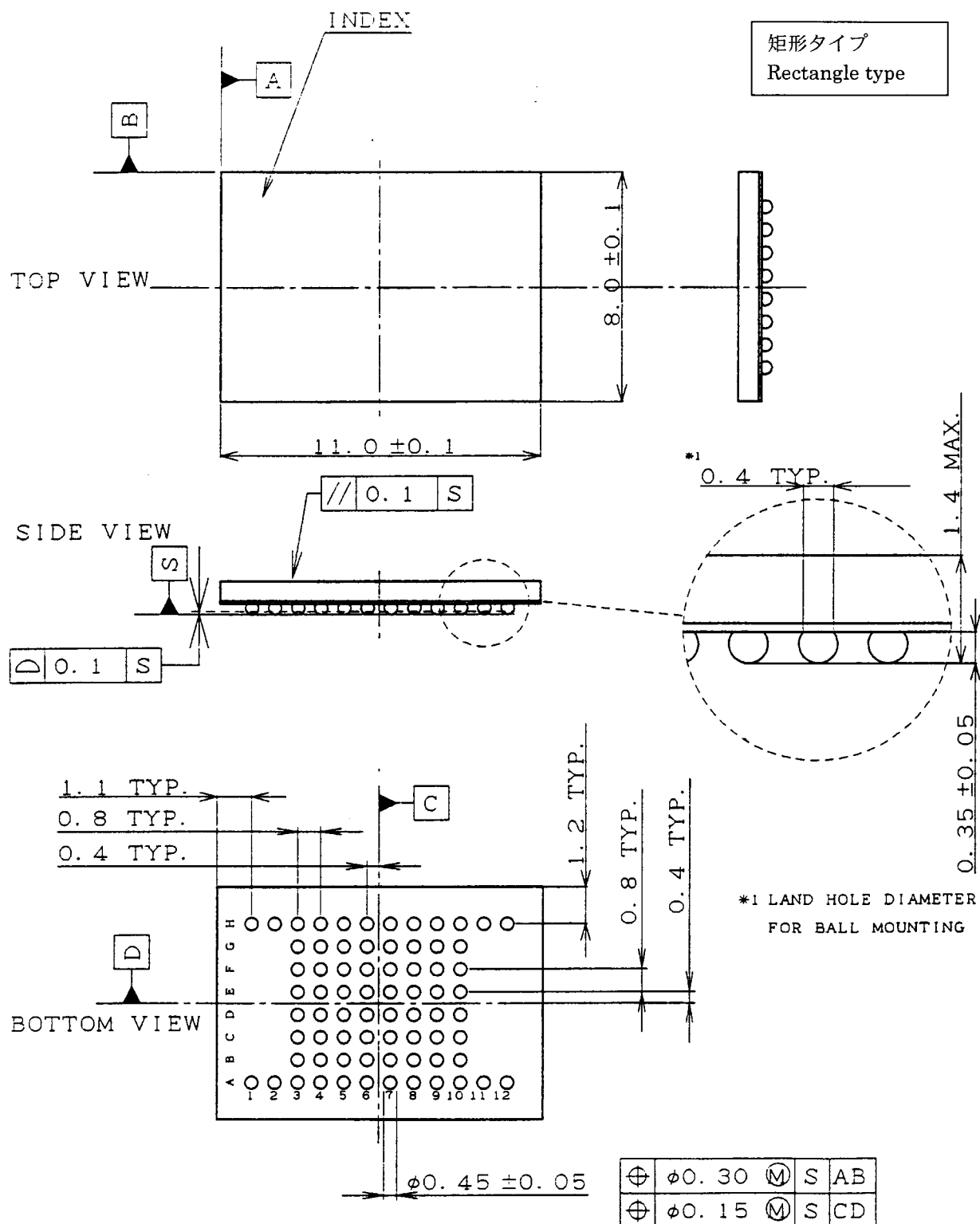
NOTE

DRAWING NO.

AA2078

単位
UNIT

mm



名称
NAME FBGA072/064-P-0811 (LCSP072/064-P-0811)

備考

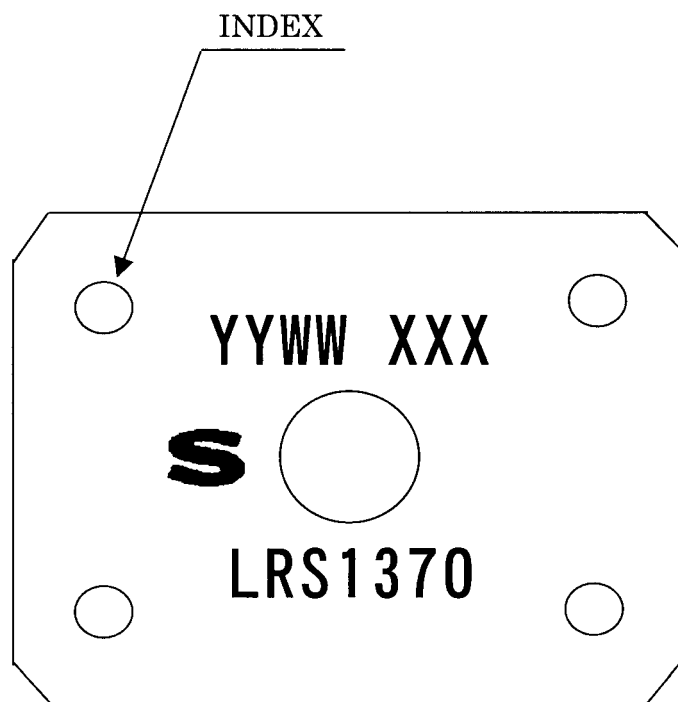
DRAWING NO. AA2149

単位
UNIT mm

NOTE

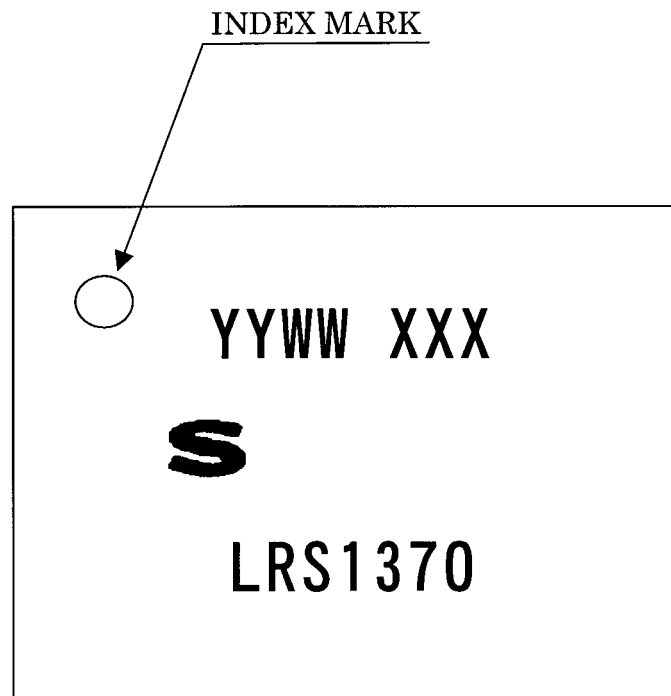
マーケレイアウト図
Marking layout

面取りタイプ
Chamfered type



マークレイアウト図
Marking layout

矩形タイプ
Rectangle type



7. Packing Specifications (Dry packing for surface mount packages.)

7-1. Packing materials.

Material name	Material specifications	Purpose
Inner carton	Cardboard (800 devices / inner carton max.)	Packing the devices. (10 trays / inner carton)
Tray	Conductive plastic (80 devices / tray)	Securing the devices.
Upper cover tray	Conductive plastic (1 tray / inner carton)	Securing the devices.
Laminated aluminum bag	Aluminum polyethylene	Keeping the devices dry.
Desiccant	Silica gel	Keeping the devices dry.
Label	Paper	Indicates part number, quantity, and packed date.
PP band	Polypropylene (3 pcs. / inner carton)	Securing the devices.
Outer carton	Cardboard (3200 devices / outer carton max.)	Outer packing.

(Devices must be placed on the tray in the same direction.)

7-2. Outline dimension of tray.

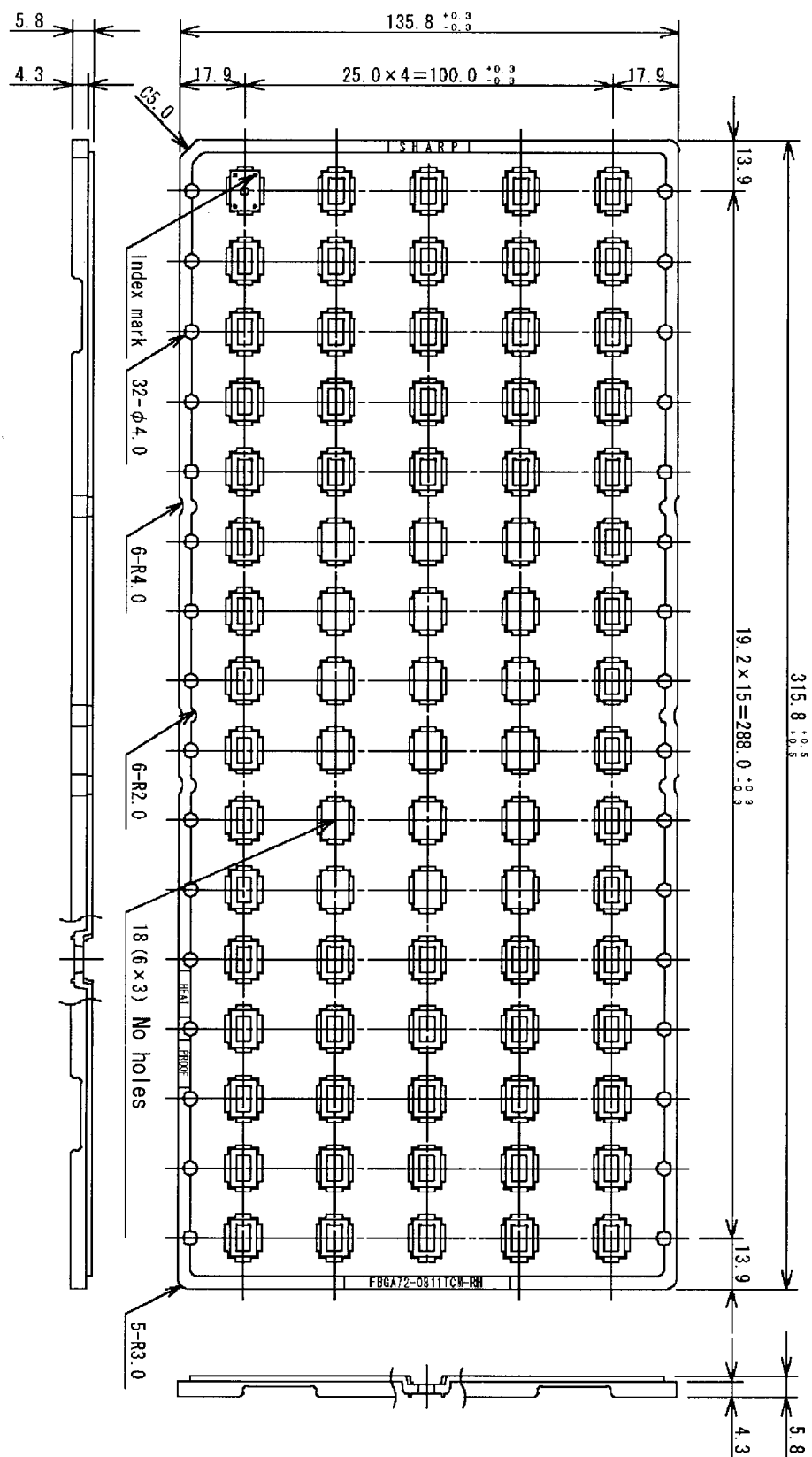
Refer to the attached drawing.

7-3. Outline dimension of carton.

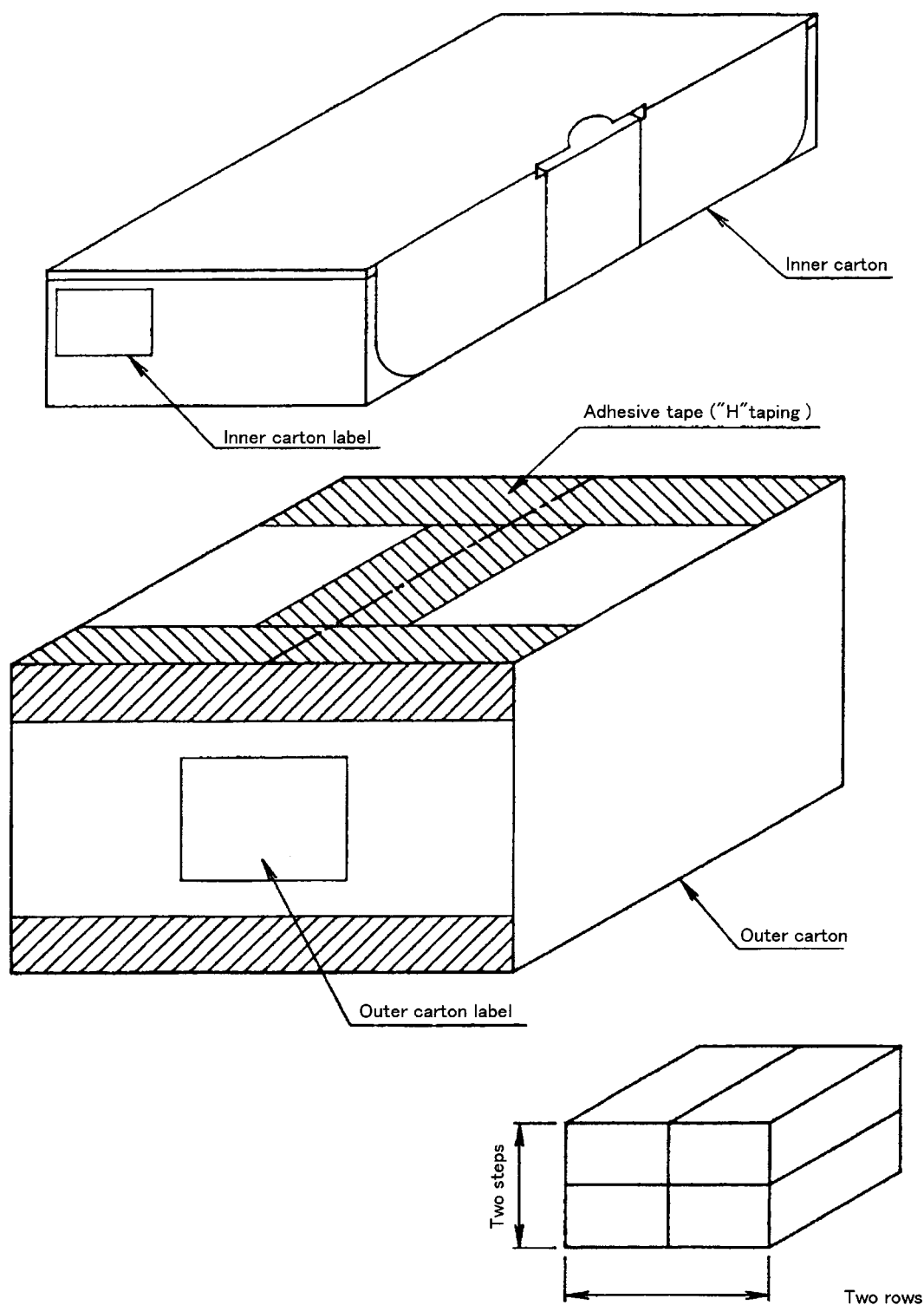
Refer to the attached drawing.

8. Precautions for use.

- (1) Opening must be done on an anti-ESD treated workbench.
All workers must also have undergone anti-ESD treatment.
- (2) The trays have undergone either conductive or anti-ESD treatment.
If another tray is used, make sure it has also undergone conductive or anti-ESD treatment.
- (3) The devices should be mounted the devices within one year of the date of delivery.



名称 NAME	FBGA72-0811TCM-RH			備考 NOTE
DRAWING NO.	CV839	単位 UNIT	mm	



$$L \times W \times H$$

Inner carton - Outer dimensions : 335×150×80

Outer carton - Outer dimensions : 340×310×175

備考 出荷数量が端数の場合、本仕様と異なることがあります。
 NOTE There is a possibility different from this specification when the number of shipments is fractions.

名称 NAME	トレイ品 包装仕様 Packing specifications		
DRAWING NO.	BJ433	単位 UNIT	mm

A-1 RECOMMENDED OPERATING CONDITIONS

A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

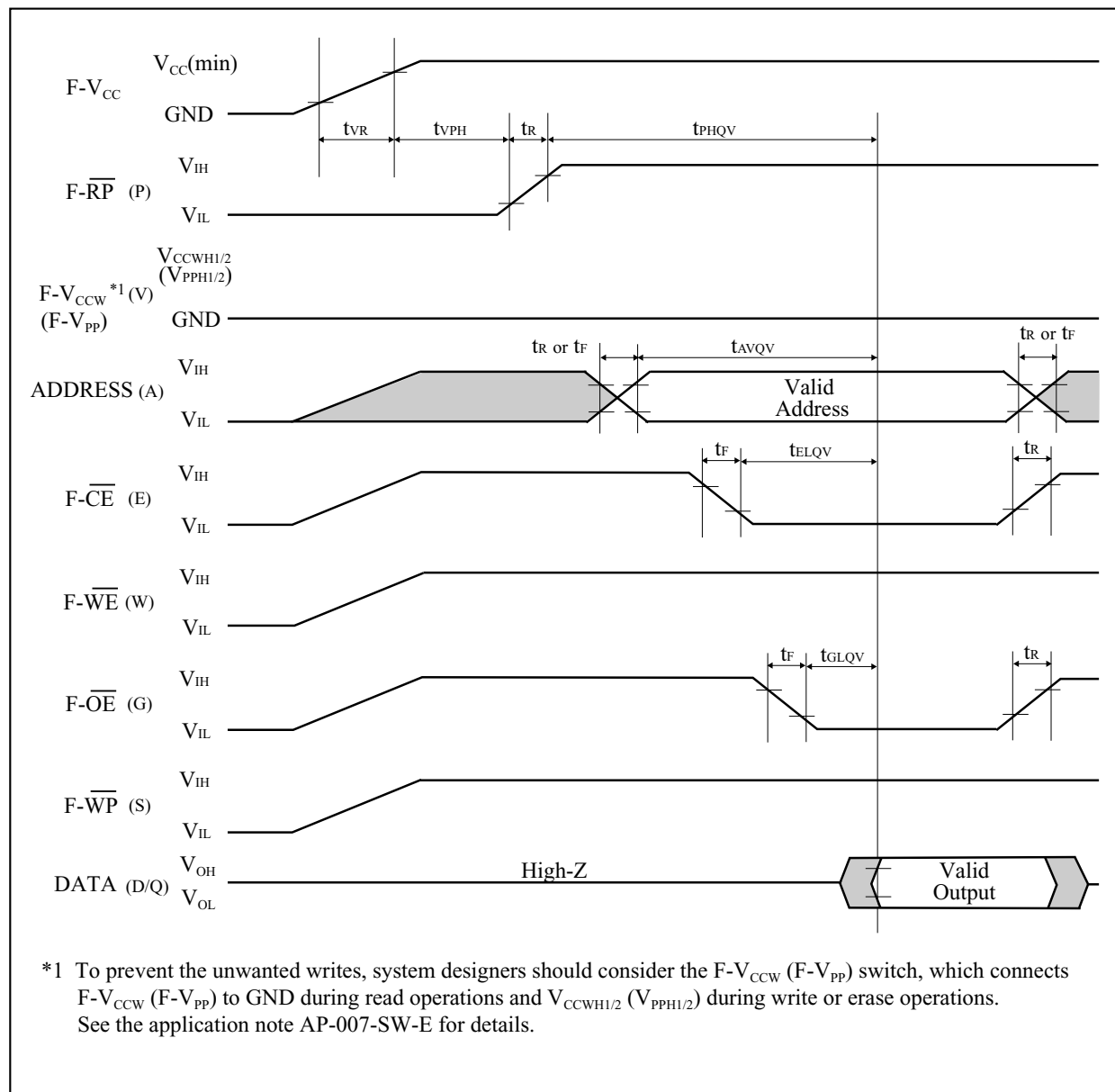


Figure A-1. AC Timing at Device Power-Up

For the AC specifications t_{VR} , t_R , t_F in the figure, refer to the next page. See the “AC Electrical Characteristics for Flash Memory” described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

A-1.1.1 Rise and Fall Time

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{VR}	F- V_{CC} Rise Time	1	0.5	30000	$\mu s/V$
t_R	Input Signal Rise Time	1, 2		1	$\mu s/V$
t_F	Input Signal Fall Time	1, 2		1	$\mu s/V$

NOTES:

1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.
 t_R (Max.) and t_F (Max.) for F-RP are 50 $\mu s/V$.

A-1.2 Glitch Noises

Do not input the glitch noises which are below V_{IH} (Min.) or above V_{IL} (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).

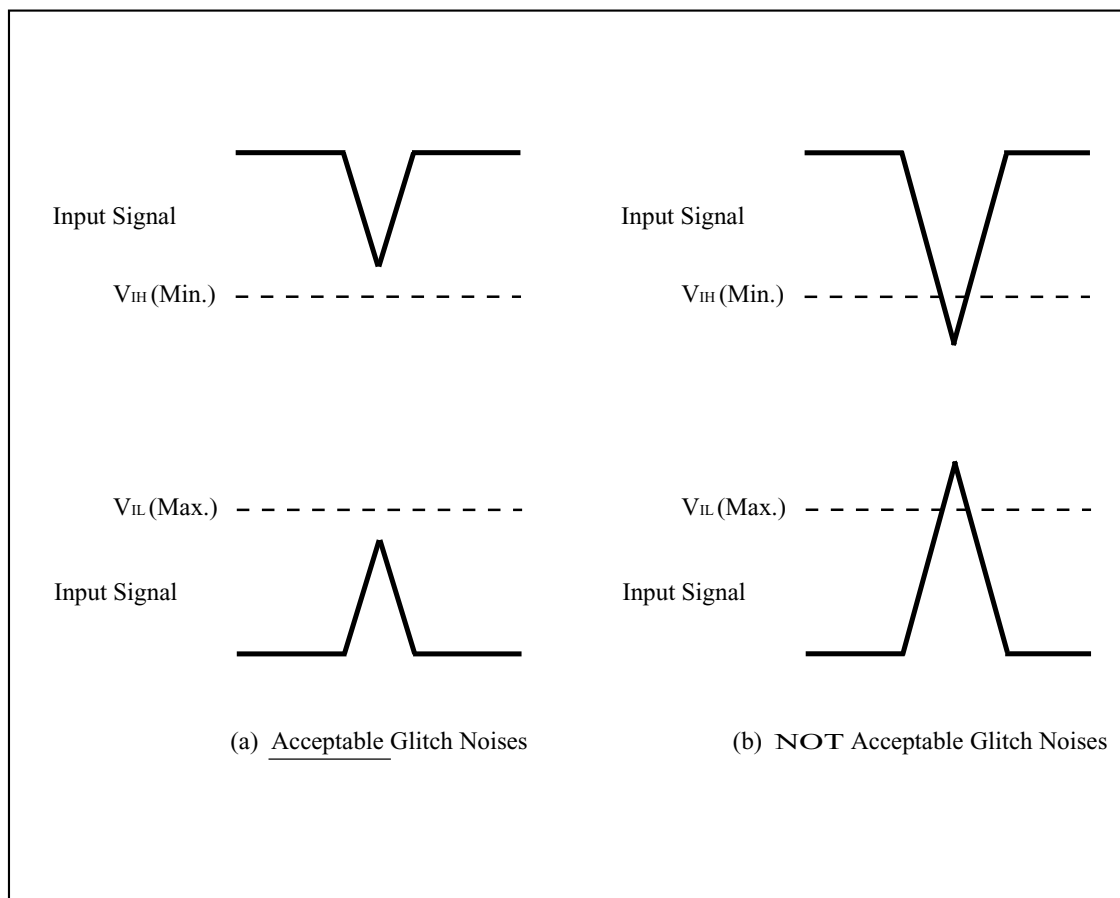


Figure A-2. Waveform for Glitch Noises

See the “DC Electrical Characteristics” described in specifications for V_{IH} (Min.) and V_{IL} (Max.).

A-2 RELATED DOCUMENT INFORMATION⁽¹⁾

Document No.	Document Name
AP-001-SD-E	Flash Memory Family Software Drivers
AP-006-PT-E	Data Protection Method of SHARP Flash Memory
AP-007-SW-E	RP#, V _{pp} Electric Potential Switching Circuit

NOTE:

1. International customers should contact their local SHARP or distribution sales office.

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