PRELIMINARY PRODUCT SPECIFICATIONS

SHARP®

Integrated Circuits Group

LRS1331C

Stacked Chip

16M (x16) Flash and 4M (x16) SRAM

(Model No.: LRS1331C)

Spec No.: MFM2-J13603
Issue Date: June 14, 2001

- When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

  (1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).

  - Office electronics
  - Instrumentation and measuring equipment
  - Machine tools
  - Audiovisual equipment
  - Home appliance
  - Communication equipment other than for trunk lines

  (2) Those contemplating using the products covered herein for the following equipment <u>which demands high reliability</u>, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

  - Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
  - Mainframe computers
  - Traffic control systems
  - Gas leak detectors and automatic cutoff devices
  - Rescue and security equipment
  - Other safety devices and safety equipment, etc.

  (3) Do not use the products covered herein for the following equipment <u>which demands extremely high performance</u> in terms of functionality, reliability, or accuracy.

  - Aerospace equipment
  - Communications equipment for trunk lines
  - Control equipment for the nuclear power industry
  - Medical equipment related to life support, etc.

  (4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

- Please direct all queries regarding the products covered herein to a sales representative of the company.

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1. Description

The LRS1331C is a combination memory organized as 1,048,576 × 16 bit flash memory and 262,144 × 16 bit static RAM in one package.

Features

- Power supply •••• 2.7V to 3.3V
- Operating temperature •••• -25°C to +85°C
- Not designed or rated as radiation hardened
- 72 pin CSP (LCSP072-P-0811) plastic package
- Flash memory has P-type bulk silicon, and SRAM has P-type bulk silicon

Flash Memory

- Access Time •••• 90 ns (Max.)
- Power Supply current (The current for F-V_{CC} pin and F-V_{CCW} pin)
  - Read •••• 25 mA (Max. t_{CYCLE} = 200ns, CMOS Input)
  - Word write •••• 57 mA (Max.)
  - Block erase •••• 42 mA (Max.)
  - Reset Power-Down •••• 20 µA (Max. F-$\overline{RP}$ = GND ± 0.2V, I_{OUT} (F-RY/$\overline{BY}$) = 0mA)
  - Standby •••• 30 µA (Max. F-$\overline{CE}$ = F-$\overline{RP}$ = F-V_{CC} ± 0.2V)
- Optimized Array Blocking Architecture
  - Two 4k-word Boot Blocks
  - Six 4k-word Parameter Blocks
  - Thirty-one 32k-word Main Blocks
  - Bottom Boot Location
- Extended Cycling Capability
  - 100,000 Block Erase Cycles (F-V_{CCW} = 2.7 to 3.3V)
- Enhanced Automated Suspend Options
  - Word Write Suspend to Read
  - Block Erase Suspend to Word Write
  - Block Erase Suspend to Read

SRAM

- Access Time •••• 85 ns (Max.)
- Power Supply current
  - Operating current •••• 45 mA (Max. t_{RC},t_{WC} = Min.)
  - •••• 8 mA (Max. t_{RC},t_{WC} = 1µs, CMOS Input)
  - Standby current •••• 15 µA (Max.)
  - Data retention current •••• 15 µA (Max. S-V_{CC} = 3.0V)

2. Pin Configuration

INDEX (TOP View)

	1	2	3	4	5	6	7	8	9	10	11	12
A	NC	NC	NC	A_{11}	A_{15}	A_{14}	A_{13}	A_{12}	GND	NC	NC	NC
B			A_{16}	A_8	A_{10}	A_9	DQ_{15}	S-$\overline{WE}$	DQ_{14}	DQ_7		
C			F-$\overline{WE}$	F-RY/$\overline{BY}$	T_1	S-A_{17}	DQ_{13}	DQ_6	DQ_4	DQ_5		
D			GND	F-$\overline{RP}$	T_2	T_4	DQ_{12}	S-CE_2	S-V_{CC}	F-V_{CC}		
E			F-$\overline{WP}$	F-V_{CCW}	F-A_{19}	DQ_{11}	T_3	DQ_{10}	DQ_2	DQ_3		
F			S-$\overline{LB}$	S-$\overline{UB}$	S-$\overline{OE}$	NC	DQ_9	DQ_8	DQ_0	DQ_1		
G			F-A_{18}	F-A_{17}	A_7	A_6	A_3	A_2	A_1	S-$\overline{CE_1}$		
H	NC	NC	NC	A_5	A_4	A_0	F-$\overline{CE}$	GND	F-$\overline{OE}$	NC	NC	NC

Note) From T_1 to T_4 pins are needed to be open.
Two NC pins at the corner are connected.
Do not float any GND pins.

Pin	Description	Type
A_0 to A_{16}	Address Inputs (Common)	Input
F-A_{17} to F-A_{19}	Address Inputs (Flash)	Input
S-A_{17}	Address Inputs (SRAM)	Input
F-$\overline{CE}$	Chip Enable Inputs (Flash)	Input
S-$\overline{CE}_1$, S-CE_2	Chip Enable Inputs (SRAM)	Input
F-$\overline{WE}$	Write Enable Input (Flash)	Input
S-$\overline{WE}$	Write Enable Input (SRAM)	Input
F-$\overline{OE}$	Output Enable Input (Flash)	Input
S-$\overline{OE}$	Output Enable Input (SRAM)	Input
S-$\overline{LB}$	SRAM Byte Enable Input (DQ_0 to DQ_7)	Input
S-$\overline{UB}$	SRAM Byte Enable Input (DQ_8 to DQ_{15})	Input
F-$\overline{RP}$	Reset Power Down Input (Flash) Block erase and Write : V_{IH} Read : V_{IH} Reset Power Down : V_{IL}	Input
F-$\overline{WP}$	Write Protect Input (Flash) Two Boot Blocks Locked : V_{IL}	Input
F-RY/$\overline{BY}$	Ready/Busy Output (Flash) During an Erase or Write operation : V_{OL} Block Erase and Write Suspend : High-Z (High impedance)	Open Drain Output
DQ_0 to DQ_{15}	Data Inputs and Outputs (Common)	Input / Output
F-V_{CC}	Power Supply (Flash)	Power
S-V_{CC}	Power Supply (SRAM)	Power
F-V_{CCW}	Write, Erase Power Supply (Flash) Block Erase and Write : F-$V_{CCW} = V_{CCWH}$ All Blocks Locked : F-$V_{CCW} < V_{CCWLK}$	Power
GND	GND (Common)	Power
NC	Non Connection	-
T_1 to T_4	Test pins (Should be all open)	-

3. Truth Table(1)

<table>
<tr><th>Flash</th><th>SRAM</th><th>Notes</th><th>F-$\overline{CE}$</th><th>F-$\overline{RP}$</th><th>F-$\overline{OE}$</th><th>F-$\overline{WE}$</th><th>S-$\overline{CE}_1$</th><th>S-CE_2</th><th>S-$\overline{OE}$</th><th>S-$\overline{WE}$</th><th>S-$\overline{LB}$</th><th>S-$\overline{UB}$</th><th>DQ_0 to DQ_{15}</th></tr>
<tr><td>Read</td><td rowspan="3">Standby</td><td>3,5</td><td rowspan="3">L</td><td rowspan="3">H</td><td>L</td><td rowspan="2">H</td><td colspan="2" rowspan="3">(6)</td><td rowspan="3">X</td><td rowspan="3">X</td><td colspan="2" rowspan="3">(6)</td><td>D_{OUT}</td></tr>
<tr><td>Output Disable</td><td>5</td><td rowspan="2">H</td><td>High-Z</td></tr>
<tr><td>Write</td><td>2,3,4,5</td><td>L</td><td>D_{IN}</td></tr>
<tr><td rowspan="4">Standby</td><td>Read</td><td>5</td><td rowspan="4">H</td><td rowspan="4">H</td><td rowspan="4">X</td><td rowspan="4">X</td><td rowspan="4">L</td><td rowspan="4">H</td><td>L</td><td>H</td><td colspan="3">(7)</td></tr>
<tr><td rowspan="2">Output Disable</td><td rowspan="2">5</td><td>H</td><td>H</td><td>X</td><td>X</td><td rowspan="2">High-Z</td></tr>
<tr><td>X</td><td>X</td><td>H</td><td>H</td></tr>
<tr><td>Write</td><td>5</td><td>X</td><td>L</td><td colspan="3">(7)</td></tr>
<tr><td rowspan="4">Reset Power Down</td><td>Read</td><td>5</td><td rowspan="4">X</td><td rowspan="4">L</td><td rowspan="4">X</td><td rowspan="4">X</td><td rowspan="4">L</td><td rowspan="4">H</td><td>L</td><td>H</td><td colspan="3">(7)</td></tr>
<tr><td rowspan="2">Output Disable</td><td rowspan="2">5</td><td>H</td><td>H</td><td>X</td><td>X</td><td rowspan="2">High-Z</td></tr>
<tr><td>X</td><td>X</td><td>H</td><td>H</td></tr>
<tr><td>Write</td><td>5</td><td>X</td><td>L</td><td colspan="3">(7)</td></tr>
<tr><td>Standby</td><td rowspan="2">Standby</td><td>5</td><td>H</td><td>H</td><td rowspan="2">X</td><td rowspan="2">X</td><td colspan="2" rowspan="2">(6)</td><td rowspan="2">X</td><td rowspan="2">X</td><td colspan="2" rowspan="2">(6)</td><td rowspan="2">High-Z</td></tr>
<tr><td>Reset Power Down</td><td>5</td><td>X</td><td>L</td></tr>
</table>

Notes:

1. L = V_{IL}, H = V_{IH}, X = H or L. Refer to DC Characteristics. High-Z = High impedance.
2. Command Writes involving block erase, full chip erase, word write, or lock-bit configuration are reliably executed when F-V_{CCW} = V_{CCWH} and F-V_{CC} = 2.7V to 3.3V.
   Block erase, full chip erase, word write, or lock-bit configuration with F-V_{CCW} < V_{CCWH} (Min.) produce spurious results and should not be attempted.
3. Never hold F-$\overline{OE}$ low and F-$\overline{WE}$ low at the same timing.
4. Refer Section 5. Command Definitions for Flash Memory valid D_{IN} during a write operation.
5. F-$\overline{WP}$ set to V_{IL} or V_{IH}.

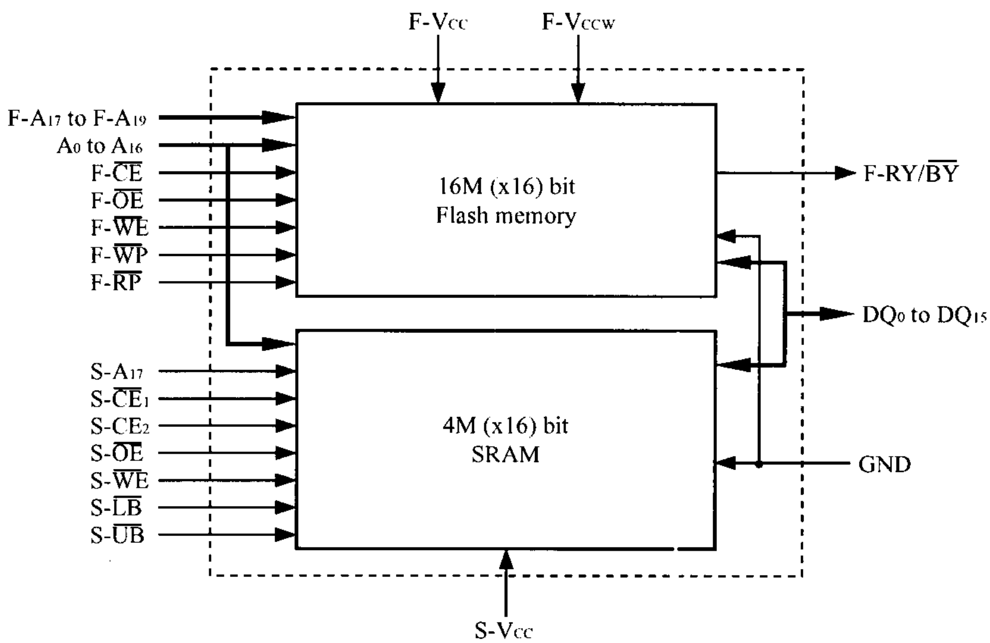
6. SRAM Standby Mode

S-$\overline{CE}_1$	S-CE_2	S-$\overline{LB}$	S-$\overline{UB}$
H	X	X	X
X	L	X	X
X	X	H	H

7. S-$\overline{UB}$, S-$\overline{LB}$ Control Mode

S-$\overline{LB}$	S-$\overline{UB}$	DQ_0 to DQ_7	DQ_8 to DQ_{15}
L	L	D_{OUT}/D_{IN}	D_{OUT}/D_{IN}
L	H	D_{OUT}/D_{IN}	High-Z
H	L	High-Z	D_{OUT}/D_{IN}

4. Block Diagram



5. Command Definitions for Flash Memory[1]

5.1 Command Definitions

Command	Bus Cycles Required	Note	First Bus Cycle			Second Bus Cycle		
			Oper[2]	Address[3]	Data	Oper[2]	Address[3]	Data[3]
Read Array / Reset	1		Write	XA	FFH			
Read Identifier Codes	≥ 2	4	Write	XA	90H	Read	IA	ID
Read Status Register	2		Write	XA	70H	Read	XA	SRD
Clear Status Register	1		Write	XA	50H			
Block Erase	2	5	Write	XA	20H	Write	BA	D0H
Full Chip Erase	2	5	Write	XA	30H	Write	XA	D0H
Word Write	2	5	Write	XA	40H or 10H	Write	WA	WD
Block Erase and Word Write Suspend	1	5,9	Write	XA	B0H			
Block Erase and Word Write Resume	1	5,9	Write	XA	D0H			
Set Block Lock Bit	2	7	Write	XA	60H	Write	BA	01H
Clear Block Lock Bits	2	6,7	Write	XA	60H	Write	XA	D0H
Set Permanent Lock Bit	2	8	Write	XA	60H	Write	XA	F1H

Notes:

1. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.
2. Bus operations are defined in 3. Truth Table.
3. XA = Any valid address within the device.
   IA = Identifier code address.
   BA = Address within the block being erased.
   WA = Address of memory location to be written.
   SRD = Data read from status register (See 6. Status Register Definition).
   WD = Data to be written at location WA. Data is latched on the rising edge of F-$\overline{WE}$ or F-$\overline{CE}$ (whichever goes high first).
   ID = Data read from identifier codes (See 5.2 Identifier Codes).
4. See Identifier Codes at next page.
5. See Write Protection Alternatives in section 5.3.
6. The clear block lock-bits operation simultaneously clears all block lock-bits.
7. If the permanent lock-bit is set, Set Block Lock-Bit and Clear Block Lock-Bits commands can not be done.
8. Once the permanent lock-bit is set, it cannot be cleared.
9. If the time between writing the Block Erase Resume command and writing the Block Erase Suspend command is shorter than t_{ERES} and both commands are written repeatedly, a longer time is required than standard block erase until the completion of the operation.

5.2 Identifier Codes(3)

Codes	Address $[A_{19} - A_0]$	Data $[DQ_{15} - DQ_0]$
Manufacture Code	00000H	00B0H
Device Code	00001H	00E9H
Block Lock Configuration(2)	BA(1) + 2	$DQ_0 = 0$: Unlocked $DQ_0 = 1$: Locked
Permanent Lock Configuration(2)	00003H	$DQ_0 = 0$: Unlocked $DQ_0 = 1$: Locked

Notes:

1. BA selects the specific block lock configuration code to be read.
2. $DQ_{15} - DQ_1$ are reserved for future use.
3. Read Identifier Codes command is defined in 5.1 Command Definitions.

5.3 Write Protection Alternatives

Operation	$F\text{-}V_{CCW}$	$F\text{-}\overline{RP}$	$F\text{-}\overline{WP}$	Permanent Lock-Bit	Block Lock-Bit	Effect
Block Erase or Word Write	$\leq V_{CCWLK}$	X	X	X	X	All Blocks Locked.
	$>V_{CCWLK}$(1)	V_{IL}	X	X	X	All Blocks Locked.
		V_{IH}	V_{IL}	X	0	2 Boot Blocks Locked.
			V_{IH}			Block Erase and Word Write Enabled.
			V_{IL}		1	Block Erase and Word Write Disabled.
			V_{IH}			Block Erase and Word Write Disabled.
Full Chip Erase	$\leq V_{CCWLK}$	X	X	X	X	All Blocks Locked.
	$>V_{CCWLK}$(1)	V_{IL}	X	X	X	All Blocks Locked.
		V_{IH}	V_{IL}	X	X	All Unlocked Blocks are Erased. 2 Boot Blocks and Locked Blocks are Not Erased.
			V_{IH}			All Unlocked Blocks are Erased. Locked Blocks are Not Erased.
Set Block Lock-Bit	$\leq V_{CCWLK}$	X	X	X	X	Set Block Lock-Bit Disabled.
	$>V_{CCWLK}$(1)	V_{IL}	X	X	X	Set Block Lock-Bit Disabled.
		V_{IH}	X	0	X	Set Block Lock-Bit Enabled.
			X	1	X	Set Block Lock-Bit Disabled.
Clear Block Lock-Bits	$\leq V_{CCWLK}$	X	X	X	X	Clear Block Lock-Bits Disabled.
	$>V_{CCWLK}$(1)	V_{IL}	X	X	X	Clear Block Lock-Bits Disabled.
		V_{IH}	X	0	X	Clear Block Lock-Bits Enabled.
			X	1	X	Clear Block Lock-Bits Disabled.
Set Permanent Lock-Bit	$\leq V_{CCWLK}$	X	X	X	X	Set Permanent Lock-Bit Disabled.
	$>V_{CCWLK}$(1)	V_{IL}	X	X	X	Set Permanent Lock-Bit Disabled.
		V_{IH}	X	X	X	Set Permanent Lock- Bit Enabled.

Note:

1. $F\text{-}V_{CCW}$ is guaranteed only with the nominal voltages.

6. Status Register Definition

WSMS	BESS	ECBLBS	WWSLBS	VCCWS	WWSS	DPS	R
7	6	5	4	3	2	1	0

SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Notes: Check SR.7 or F-RY/$\overline{BY}$ to determine Block Erase, Full Chip Erase, Word Write or Lock-Bit configuration completion. SR.6 - SR.1 are invalid while SR.7 = "0".
SR.6 = BLOCK ERASE SUSPEND STATUS (BESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	
SR.5 = ERASE AND CLEAR BLOCK LOCK-BITS STATUS (ECBLBS) 1 = Error in Block Erase, Full Chip Erase or Clear Block Lock-Bits 0 = Successful Block Erase, Full Chip Erase or Clear Block Lock-Bits	If both SR.5 and SR.4 are "1"s after a Block Erase, Full Chip Erase or Lock-Bit configuration attempt, an improper command sequence was entered.
SR.4 = WORD WRITE AND SET LOCK-BIT STATUS (WWSLBS) 1 = Error in Word Write or Set Block/Permanent Lock-Bit 0 = Successful Word Write or Set Block/Permanent Lock-Bit	SR.3 does not provide a continuous indication of F-V_{CCW} level. The WSM (Write State Machine) interrogates and indicates the F-V_{CCW} level only after Block Erase, Full Chip Erase, Word Write, or Lock-Bit Configuration command sequences. SR.3 is not guaranteed to reports accurate feedback only when F-$V_{CCW} \neq V_{CCWH}$.
SR.3 = F-V_{CCW} STATUS (VCCWS) 1 = F-V_{CCW} Low Detect, Operation Abort 0 = F-V_{CCW} OK	
SR.2 = WORD WRITE SUSPEND STATUS (WWSS) 1 = Word Write Suspended 0 = Word Write in Progress/Completed	SR.1 does not provide a continuous indication of permanent and block lock-bit and F-$\overline{WP}$ values. The WSM interrogates the permanent lock-bit, block lock-bit and F-$\overline{WP}$ only after Block Erase, Full Chip Erase, Word Write, or Lock-Bit Configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set, permanent lock-bit is set and/or F-$\overline{WP}$ is V_{IL}. Reading the block lock and permanent lock configuration codes after writing the Read Identifier Codes command indicates permanent and block lock-bit status.
SR.1 = DEVICE PROTECT STATUS (DPS) 1 = Block Lock-Bit, Permanent Lock-Bit and/or F-$\overline{WP}$ Lock Detected, Operation Abort 0 = Unlocked	
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	SR.0 is reserved for future use and should be masked out when polling the status register.

7. Memory Map for Flash Memory

Bottom Boot

[A19 ~ A0]	
FFFFF – F8000	32K-word Main Block 30
F7FFF – F0000	32K-word Main Block 29
EFFFF – E8000	32K-word Main Block 28
E7FFF – E0000	32K-word Main Block 27
DFFFF – D8000	32K-word Main Block 26
D7FFF – D0000	32K-word Main Block 25
CFFFF – C8000	32K-word Main Block 24
C7FFF – C0000	32K-word Main Block 23
BFFFF – B8000	32K-word Main Block 22
B7FFF – B0000	32K-word Main Block 21
AFFFF – A8000	32K-word Main Block 20
A7FFF – A0000	32K-word Main Block 19
9FFFF – 98000	32K-word Main Block 18
97FFF – 90000	32K-word Main Block 17
8FFFF – 88000	32K-word Main Block 16
87FFF – 80000	32K-word Main Block 15
7FFFF – 78000	32K-word Main Block 14
77FFF – 70000	32K-word Main Block 13
6FFFF – 68000	32K-word Main Block 12
67FFF – 60000	32K-word Main Block 11
5FFFF – 58000	32K-word Main Block 10
57FFF – 50000	32K-word Main Block 9
4FFFF – 48000	32K-word Main Block 8
47FFF – 40000	32K-word Main Block 7
3FFFF – 38000	32K-word Main Block 6
37FFF – 30000	32K-word Main Block 5
2FFFF – 28000	32K-word Main Block 4
27FFF – 20000	32K-word Main Block 3
1FFFF – 18000	32K-word Main Block 2
17FFF – 10000	32K-word Main Block 1
0FFFF – 08000	32K-word Main Block 0
07FFF – 07000	4K-word Parameter Block 5
06FFF – 06000	4K-word Parameter Block 4
05FFF – 05000	4K-word Parameter Block 3
04FFF – 04000	4K-word Parameter Block 2
03FFF – 03000	4K-word Parameter Block 1
02FFF – 02000	4K-word Parameter Block 0
01FFF – 01000	4K-word Boot Block 1
00FFF – 00000	4K-word Boot Block 0

8. Absolute Maximum Ratings

Symbol	Parameter	Notes	Ratings	Unit
V_{CC}	Supply voltage	1,2	-0.2 to +4.0	V
V_{IN}	Input voltage	1,2,3,4	-0.2 to V_{CC} + 0.3	V
T_A	Operating temperature		-25 to +85	°C
T_{STG}	Storage temperature		-55 to +125	°C
F-V_{CCW}	F-V_{CCW} voltage	1,3	-0.3 to +4.0	V

Notes:
1. The maximum applicable voltage on any pins with respect to GND.
2. Except F-V_{CCW}.
3. -1.0V undershoot and V_{CC} + 1.0V overshoot are allowed when the pulse width is less than 20 nsec.
4. V_{IN} should not be over + 4.0V.

9. Recommended DC Operating Conditions

(T_A = -25°C to +85°C)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	2	2.7	3.0	3.3	V
V_{IH}	Input Voltage	1	2.2		V_{CC}+0.2	V
V_{IL}	Input Voltage		-0.2		0.4	V

Notes:
1. V_{CC} is the lower one of F-V_{CC} and S-V_{CC}.
2. V_{CC} includes both F-V_{CC} and S-V_{CC}.

10. Pin Capacitance(1)

(T_A = 25°C, f = 1MHz)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Condition
C_{IN}	Input capacitance				15	pF	V_{IN} = 0V
$C_{I/O}$	I/O capacitance				25	pF	$V_{I/O}$ = 0V

Note:
1. Sampled but not 100% tested.

11. DC Electrical Characteristics[6]

DC Electrical Characteristics

(T_A = -25°C to +85°, V_{CC} = 2.7V to 3.3V)

Symbol	Parameter	Notes	Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI}	Input Leakage Current				±1.5	μA	V_{IN} = V_{CC} or GND
I_{LO}	Output Leakage Current				±1.5	μA	V_{OUT} = V_{CC} or GND
I_{CCS}	F-V_{CC} Standby Current	2,4		2	15	μA	CMOS Input F-$\overline{CE}$ = F-$\overline{RP}$ = F-V_{CC} ± 0.2V
				0.2	2	mA	TTL Input F-$\overline{CE}$ = F-$\overline{RP}$ = V_{IH}
I_{CCAS}	F-V_{CC} Auto Power-Save Current	3,4		2	15	μA	CMOS Input F-$\overline{CE}$ = GND ± 0.2V
I_{CCD}	F-V_{CC} Reset Power-Down Current			2	15	μA	F-$\overline{RP}$ = GND ± 0.2V I_{OUT}(F-RY/$\overline{BY}$) = 0mA
I_{CCR}	F-V_{CC} Read Current	4		15	25	mA	CMOS Input F-$\overline{CE}$ = GND, f = 5MHz, I_{OUT} = 0mA
					30	mA	TTL Input F-$\overline{CE}$ = V_{IL}, f = 5MHz, I_{OUT} = 0mA
I_{CCW}	F-V_{CC} Word Write or Set Lock-Bit Current	7		5	17	mA	F-V_{CCW} = V_{CCWH}
I_{CCE}	F-V_{CC} Block Erase, Full Chip Erase or Clear Block Lock-Bits Current	7		4	17	mA	F-V_{CCW} = V_{CCWH}
I_{CCWS} I_{CCES}	F-V_{CC} Word Write or Block Erase Suspend Current			1	6	mA	F-$\overline{CE}$ = V_{IH}
I_{CCWS} I_{CCWR}	F-V_{CCW} Standby or Read Current			±2	±15	μA	F-V_{CCW} ≤ F-V_{CC}
				10	200	μA	F-V_{CCW} > F-V_{CC}
I_{CCWAS}	F-V_{CCW} Auto Power-Save Current	3,4		0.1	5	μA	CMOS Input F-$\overline{CE}$ = GND ± 0.2V
I_{CCWD}	F-V_{CCW} Reset Power-Down Current			0.1	5	μA	F-$\overline{RP}$ = GND ± 0.2V
I_{CCWW}	F-V_{CCW} Word Write or Set Lock-Bit Current	7		12	40	mA	F-V_{CCW} = V_{CCWH}
I_{CCWE}	F-V_{CCW} Block Erase, Full Chip Erase or Clear Block Lock-Bits Current	7		8	25	mA	F-V_{CCW} = V_{CCWH}
I_{CCWWS} I_{CCWES}	F-V_{CCW} Word Write or Block Erase Suspend Current			10	200	μA	F-V_{CCW} = V_{CCWH}
I_{SB}	S-V_{CC} Standby Current			1	15	μA	S-$\overline{CE}_1$, S-CE_2 ≥ S-V_{CC} - 0.2V or S-CE_2 ≤ 0.2V
I_{SB1}	S-V_{CC} Standby Current				3	mA	S-$\overline{CE}_1$ = V_{IH} or S-CE_2 = V_{IL}

DC Electrical Characteristics (Continue)

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.3V)

Symbol	Parameter	Notes	Min.	Typ.(1)	Max.	Unit	Conditions	
I_{CC1}	S-V_{CC} Operation Current				45	mA	S-$\overline{CE}_1$ = V_{IL}, S-CE_2 = V_{IH}, V_{IN} = V_{IL} or V_{IH}	t_{CYCLE} =Min. $I_{I/O}$ = 0mA
I_{CC2}	S-V_{CC} Operation Current				8	mA	S-$\overline{CE}_1$ = 0.2V, S-CE_2=S-V_{CC}-0.2V, V_{IN} = S-V_{CC} -0.2V or 0.2V	t_{CYCLE} =1 μ s $I_{I/O}$ = 0mA
V_{IL}	Input Low Voltage	7	-0.2		0.4	V		
V_{IH}	Input High Voltage	7	2.2		V_{CC} +0.2	V		
V_{OL}	Output Low Voltage	2,7			0.4	V	I_{OL} = 0.5mA	
V_{OH}	Output High Voltage	7	2			V	I_{OH} = -0.5mA	
V_{CCWLK}	F-V_{CCW} Lockout during Normal Operations	5,7			1.5	V		
V_{CCWH}	F-V_{CCW} during Block Erase, Full Chip Erase, Word Write, or Lock-Bit configuration Operations		2.7		3.3	V		
V_{LKO}	F-V_{CC} Lockout Voltage		2			V		

Notes:

1. All currents are in RMS unless otherwise noted. Reference values at V_{CC} = 3.0V and T_A = +25°C.
2. Includes F-RY/$\overline{BY}$.
3. The Automatic Power Savings (APS) feature is placed automatically power save mode that addresses not switching more than 300ns while read mode.
4. CMOS inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL inputs are either V_{IL} or V_{IH}.
5. Block erases, full chip erase, word writes and lock-bits configurations are inhibited when F-V_{CCW} ≤ V_{CCWLK} and not guaranteed in the range between V_{CCWLK} (Max.) and V_{CCWH} (Min.), and above V_{CCWH} (Max.).
6. V_{CC} includes both F-V_{CC} and S-V_{CC}.
7. Sampled, not 100% tested.

12. AC Electrical Characteristics for Flash Memory

12.1 AC Test Conditions

Input pulse level	0V to 2.7V
Input rise and fall time	10ns
Input and Output timing Ref. level	1.35V
Output load	1TTL + C_L (50pF)

12.2 Read Cycle

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.3V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Read Cycle Time		90		ns
t_{AVQV}	Address to Output Delay			90	ns
t_{ELQV}	F-$\overline{CE}$ to Output Delay	1		90	ns
t_{PHQV}	F-$\overline{RP}$ High to Output Delay			600	ns
t_{GLQV}	F-$\overline{OE}$ to Output Delay	1		40	ns
t_{ELQX}	F-$\overline{CE}$ to Output in Low-Z		0		ns
t_{EHQZ}	F-$\overline{CE}$ High to Output in High-Z			40	ns
t_{GLQX}	F-$\overline{OE}$ to Output in Low-Z		0		ns
t_{GHQZ}	F-$\overline{OE}$ High to Output in High-Z			15	ns
t_{OH}	Output Hold form Address, F-$\overline{CE}$ or F-$\overline{OE}$ Change, Whichever Occurs First		0		ns

Note:

1. F-$\overline{OE}$ may be delayed up to t_{ELQV} - t_{GLQV} after the falling edge of F-$\overline{CE}$ without impact on t_{ELQV}.

12.3 Write Cycle (F-$\overline{WE}$ Controlled)[1,5]

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.3V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		90		ns
t_{PHWL}	F-$\overline{RP}$ High Recovery to F-$\overline{WE}$ Going Low	2	1		µs
t_{ELWL}	F-$\overline{CE}$ Setup to F-$\overline{WE}$ Going Low		10		ns
t_{WLWH}	F-$\overline{WE}$ Pulse Width		50		ns
t_{SHWH}	F-$\overline{WP}$ V_{IH} Setup to F-$\overline{WE}$ Going High	2	100		ns
t_{VPWH}	F-V_{CCW} Setup to F-$\overline{WE}$ Going High	2	100		ns
t_{AVWH}	Address Setup to F-$\overline{WE}$ Going High	3	50		ns
t_{DVWH}	Data Setup to F-$\overline{WE}$ Going High	3	50		ns
t_{WHDX}	Data Hold from F-$\overline{WE}$ High		0		ns
t_{WHAX}	Address Hold from F-$\overline{WE}$ High		0		ns
t_{WHEH}	F-$\overline{CE}$ Hold from F-$\overline{WE}$ High		10		ns
t_{WHWL}	F-$\overline{WE}$ Pulse Width High		30		ns
t_{WHRL}	F-$\overline{WE}$ going High to F-RY/$\overline{BY}$ Going Low			100	ns
t_{WHGL}	Write Recovery before Read		0		ns
t_{QVVL}	F-V_{CCW} Hold from Valid SRD, F-RY/$\overline{BY}$ High-Z	2,4	0		ns
t_{QVSL}	F-$\overline{WP}$ V_{IH} Hold from Valid SRD, F-RY/$\overline{BY}$ High-Z	2,4	0		ns

Notes:

1. Read timing characteristics during block erase, full chip erase, word write and lock-bit configurations are the same as during read-only operations. Refer to AC Characteristics for read cycle.
2. Sampled, not 100% tested.
3. Refer to Section 5. Command Definitions for Flash Memory for valid A_{IN} and D_{IN} for block erase, full chip erase, word write or lock-bit configuration.
4. F-V_{CC} should be held at V_{CCWH} until determination of block erase, full chip erase, word write or lock-bit configuration success (SR.1/3/4/5 = 0).
5. It is written when F-$\overline{CE}$ and F-$\overline{WE}$ are active. The address and data needed to execute a command are latched on the rising edge of F-$\overline{WE}$ or F-$\overline{CE}$ (Whichever goes high first).

12.4 Write Cycle (F-$\overline{CE}$ Controlled)[1,5]

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.3V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		90		ns
t_{PHEL}	F-$\overline{RP}$ High Recovery to F-$\overline{CE}$ Going Low	2	1		µs
t_{WLEL}	F-$\overline{WE}$ Setup to F-$\overline{CE}$ Going Low		0		ns
t_{ELEH}	F-$\overline{CE}$ Pulse Width		65		ns
t_{SHEH}	F-$\overline{WP}$ V_{IH} Setup to F-$\overline{CE}$ Going High	2	100		ns
t_{VPEH}	F-V_{CCW} Setup to F-$\overline{CE}$ Going High	2	100		ns
t_{AVEH}	Address Setup to F-$\overline{CE}$ Going High	3	50		ns
t_{DVEH}	Data Setup to F-$\overline{CE}$ Going High	3	50		ns
t_{EHDX}	Data Hold from F-$\overline{CE}$ High		0		ns
t_{EHAX}	Address Hold from F-$\overline{CE}$ High		0		ns
t_{EHWH}	F-$\overline{WE}$ Hold from F-$\overline{CE}$ High		0		ns
t_{EHEL}	F-$\overline{CE}$ Pulse Width High		25		ns
t_{EHRL}	F-$\overline{CE}$ going High to F-RY/$\overline{BY}$ Going Low or SR.7 Going "0"			100	ns
t_{EHGL}	Write Recovery before Read		0		ns
t_{QVVL}	F-V_{CC} Hold from Valid SRD, F-RY/$\overline{BY}$ High-Z	2,4	0		ns
t_{QVSL}	F-$\overline{WP}$ V_{IH} Hold from Valid SRD, F-RY/$\overline{BY}$ High-Z	2,4	0		ns

Notes:

1. In systems where F-$\overline{CE}$ defines the write pulse width (within a longer F-$\overline{WE}$ timing waveform), all setup, hold and inactive F-$\overline{WE}$ times should be measured relative to the F-$\overline{CE}$ waveform.
2. Sampled, not 100% tested.
3. Refer to Section 5. Command Definitions for Flash Memory for valid A_{IN} and D_{IN} for block erase, full chip erase, word write or lock-bit configuration.
4. F-V_{CCW} should be held at V_{CCWH} until determination of block erase, full chip erase, word write or lock-bit configuration success (SR.1/3/4/5=0).
5. It is written when F-$\overline{CE}$ and F-$\overline{WE}$ are active. The address and data needed to execute a command are latched on the rising edge of F-$\overline{WE}$ or F-$\overline{CE}$ (Whichever goes high first).

12.5 Block Erase, Full Chip Erase, Word Write and Lock-Bits Configuration Performance(3)

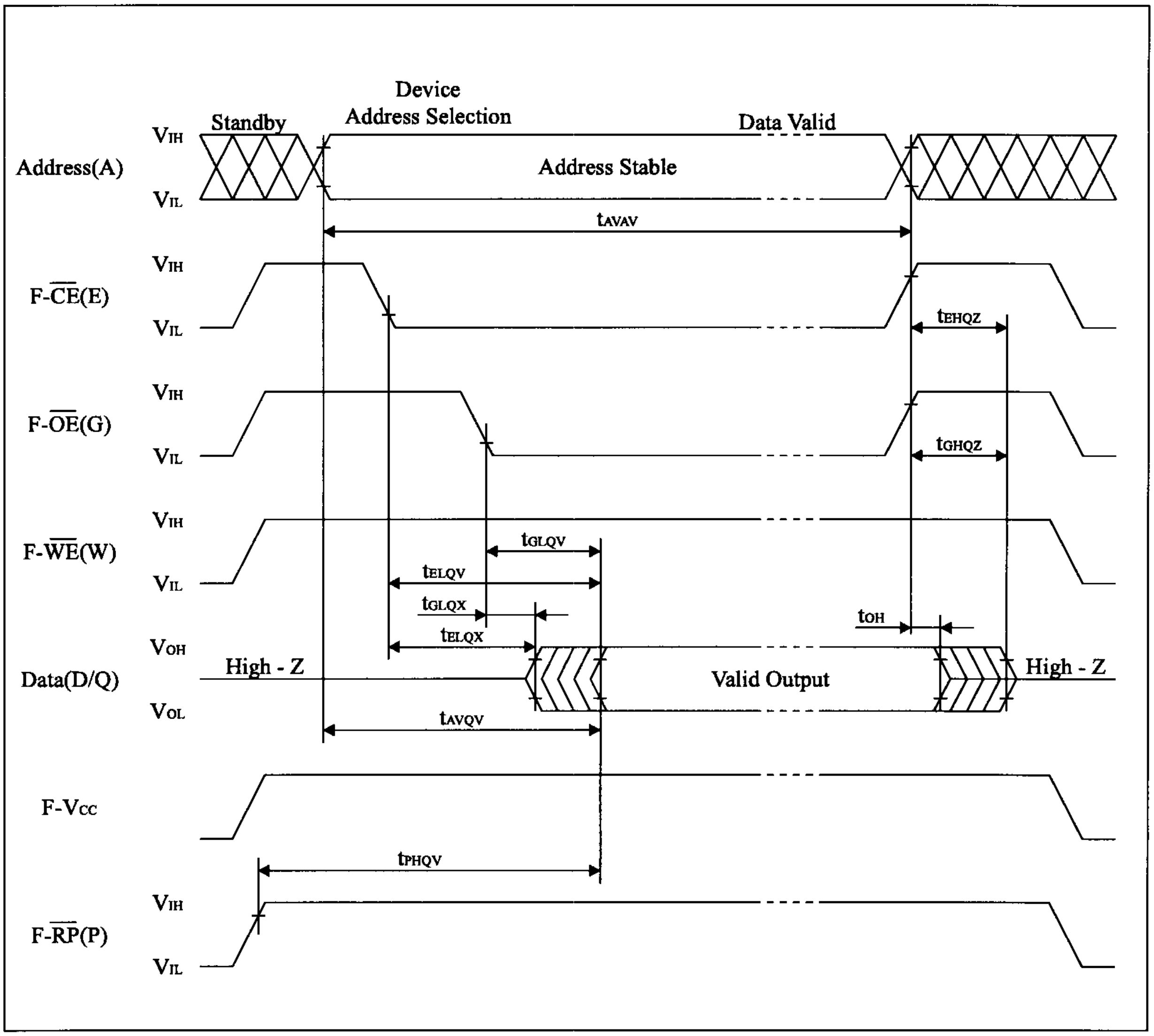
(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.3V)

Symbol	Parameter		Notes	F-V_{CCW} = 2.7V to 3.3V			Unit
				Min.	Typ.(1)	Max.	
t_{WHQV1} t_{EHQV1}	Word Write Time	32K-Word Block	2		33	200	µs
		4K-Word Block	2		36	200	µs
	Block Write Time	32K-Word Block	2		1.1	4	s
		4K-Word Block	2		0.15	0.5	s
t_{WHQV2} t_{EHQV2}	Block Erase Time	32K-Word Block	2		1.2	6	s
		4K-Word Block	2		0.6	5	s
	Full Chip Erase Time		2		42	210	s
t_{WHQV3} t_{EHQV3}	Set Lock-Bit Time		2		56	200	µs
t_{WHQV4} t_{EHQV4}	Clear Block Lock-Bits Time		2		1	5	s
t_{WHRZ1} t_{EHRZ1}	Word Write Suspend Latency Time to Read		4		6	15	µs
t_{WHRZ2} t_{EHRZ2}	Erase Suspend Latency Time to Read		4		16	30	µs
t_{ERES}	Latency Time from Block Erase Resume Command to Block Erase Suspend Command		5	600			µs

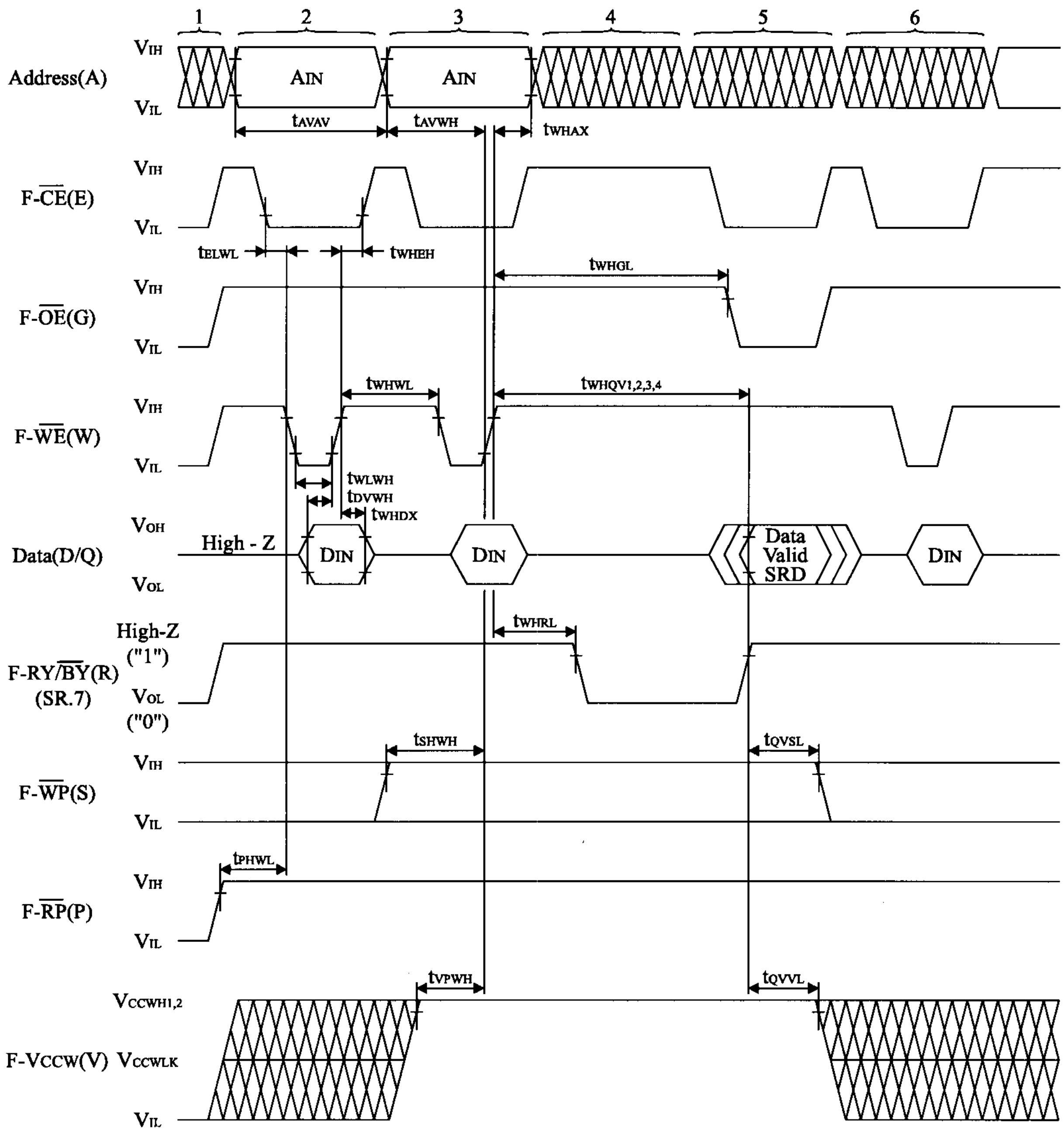
Notes:
1. Reference values at T_A = +25°C and F-V_{CC} = 3.0V, F-V_{CCW} = 3.0V. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. Sampled, not 100% tested.
4. A Latency time is required from issuing suspend command (F-$\overline{WE}$ or F-$\overline{CE}$ going high) until F-RY/$\overline{BY}$ going High-Z or SR.7 going "1".
5. If the time between writing the Block Erase Resume command and writing the Block Erase Suspend command is shorter than t_{ERES} and both commands are written repeatedly, a longer time is required than standard block erase until the completion of the operation.

12.6 Flash Memory AC Characteristics Timing Chart

Read Cycle Timing Chart

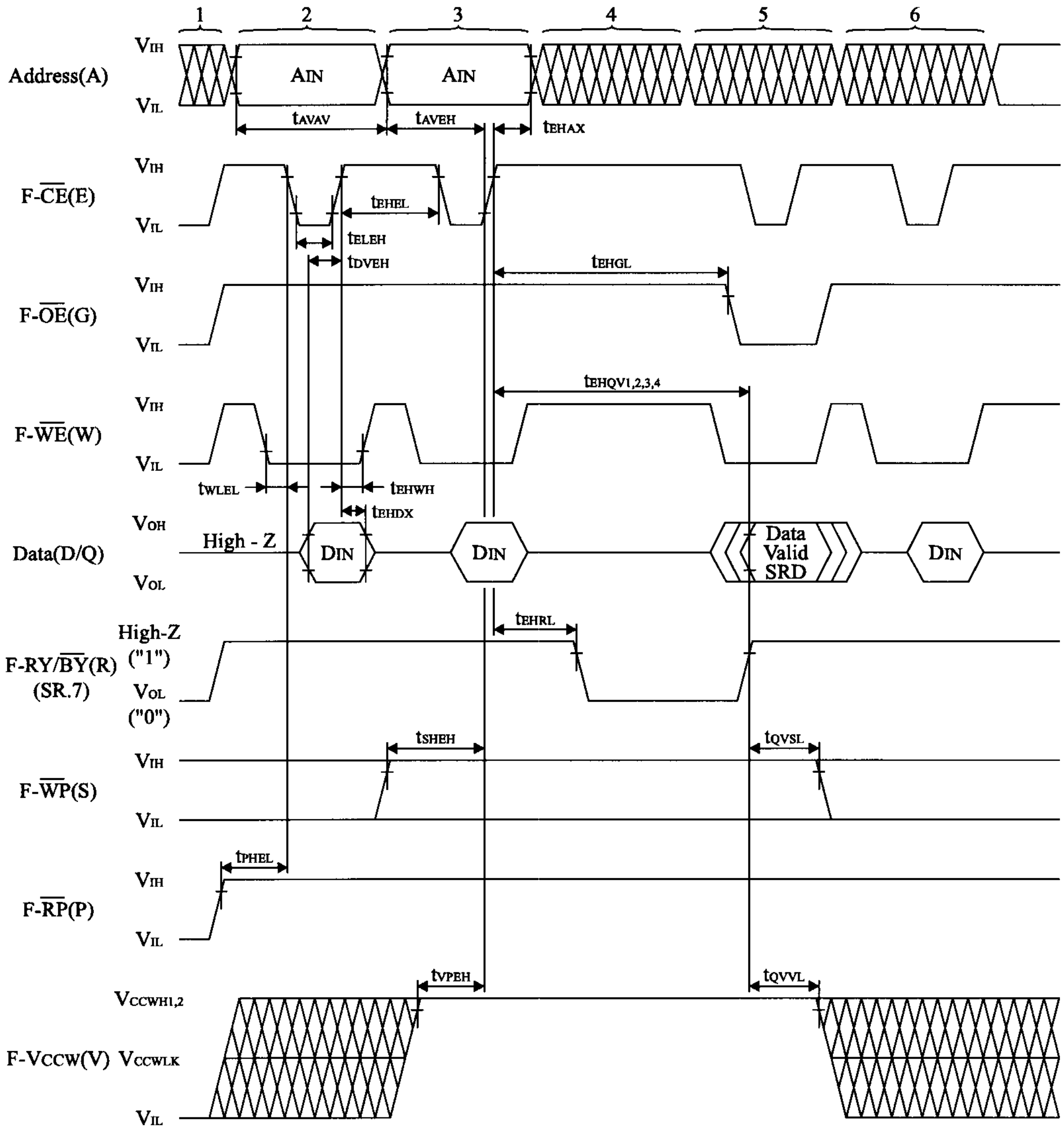


Write Cycle Timing Chart (F-WE Controlled)



Notes:
1. F-VCC power-up and standby.
2. Write each setup command.
3. Write each comfirm command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

Write Cycle Timing Chart (F-$\overline{CE}$ Controlled)



Notes:
1. F-VCC power-up and standby.
2. Write each setup command.
3. Write each comfirm command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

12.7 Reset Operations[1,2]

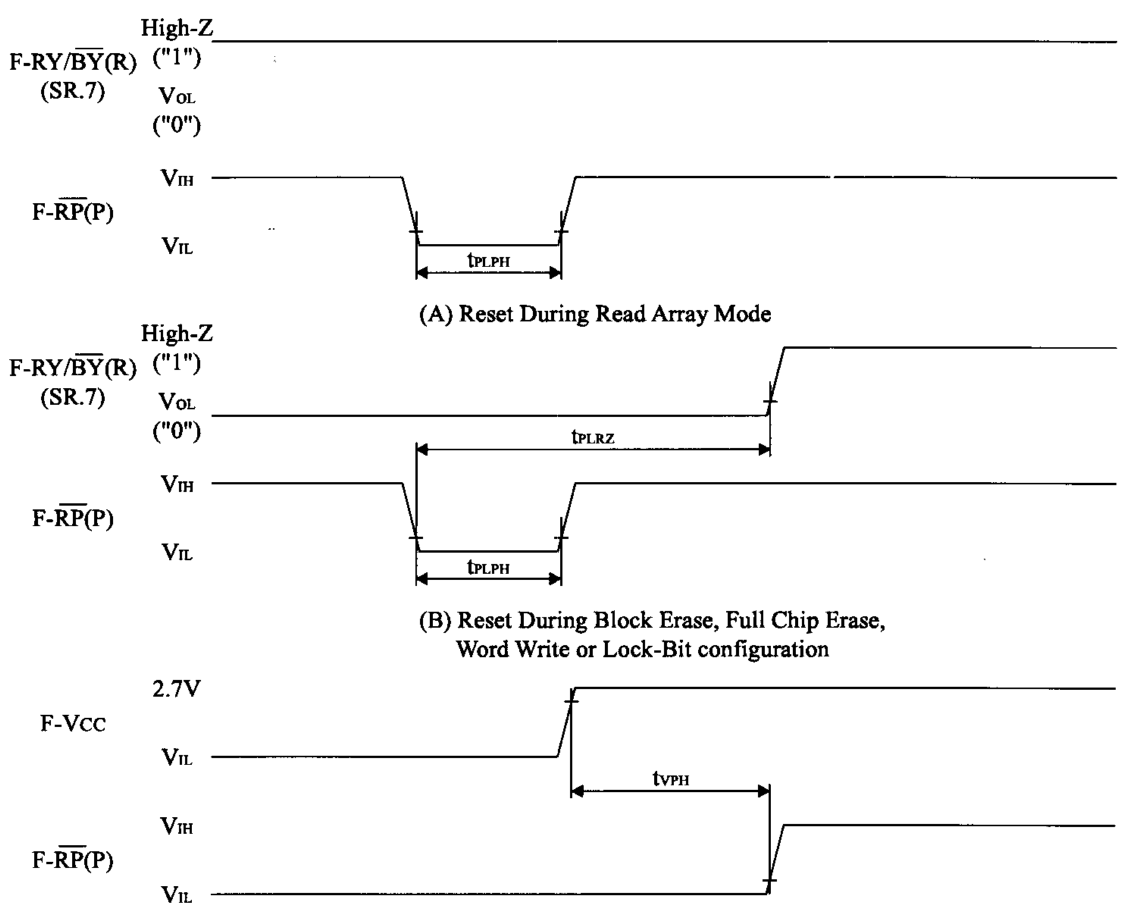
(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.3V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{PLPH}	F-$\overline{RP}$ Pulse Low Time (If F-$\overline{RP}$ is tied to V_{CC}, this specification is not applicable.)		100		ns
t_{PLRZ}	F-$\overline{RP}$ Low to Reset during Block Erase, Full Chip Erase, Word Write or lock-bit configuration			30	µs
t_{VPH}	F-V_{CC} = 2.7V to F-$\overline{RP}$ High	3	100		ns

Notes:

1. If F-$\overline{RP}$ is asserted while a block erase, full chip erase, word write or lock-bit configuration operation is not executing, the reset will complete within 100ns.
2. A reset time, t_{PHQV}, is required from the later of F-RY/$\overline{BY}$(SR.7) going High-Z ("1"), or F-$\overline{RP}$ going high until outputs are valid. Refer to AC Characteristics-Read Cycle for t_{PHQV}.
3. When the device power-up, holding F-$\overline{RP}$ low minimum 100ns is required after F-V_{CC} has been in predefined range and also has been in stable there.

AC Waveform for Reset Operation



(A) Reset During Read Array Mode

(B) Reset During Block Erase, Full Chip Erase, Word Write or Lock-Bit configuration

(C) F-$\overline{RP}$ Rising Timing

13. AC Electrical Characteristics for SRAM

13.1 AC Test Conditions

Input pulse level	0.4V to 2.2V
Input rise and fall time	5ns
Input and Output timing Ref. level	1.5V
Output load	1TTL + C_L (30pF)$^{(1)}$

Note:
1. Including scope and socket capacitance.

13.2 Read Cycle

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.3V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{RC}	Read Cycle Time		85		ns
t_{AA}	Address access time			85	ns
t_{ACE1}	Chip enable access time (S-$\overline{CE}_1$)			85	ns
t_{ACE2}	Chip enable access time (S-CE_2)			85	ns
t_{BE}	Byte enable access time			85	ns
t_{OE}	Output enable to output valid			45	ns
t_{OH}	Output hold from address change		10		ns
t_{LZ1}	S-$\overline{CE}_1$ Low to output active	1	10		ns
t_{LZ2}	S-CE_2 High to output active	1	10		ns
t_{OLZ}	S-$\overline{OE}$ Low to output active	1	5		ns
t_{BLZ}	S-$\overline{UB}$ or S-$\overline{LB}$ Low to output active	1	10		ns
t_{HZ1}	S-$\overline{CE}_1$ High to output in High-Z	1	0	30	ns
t_{HZ2}	S-CE_2 Low to output in High-Z	1	0	30	ns
t_{OHZ}	S-$\overline{OE}$ High to output in High-Z	1	0	30	ns
t_{BHZ}	S-$\overline{UB}$ or S-$\overline{LB}$ High to output in High-Z	1	0	30	ns

Note:
1. Active output to High-Z and High-Z to output active tests specified for a ±200mV transition from steady state levels into the test load.

13.3 Write Cycle

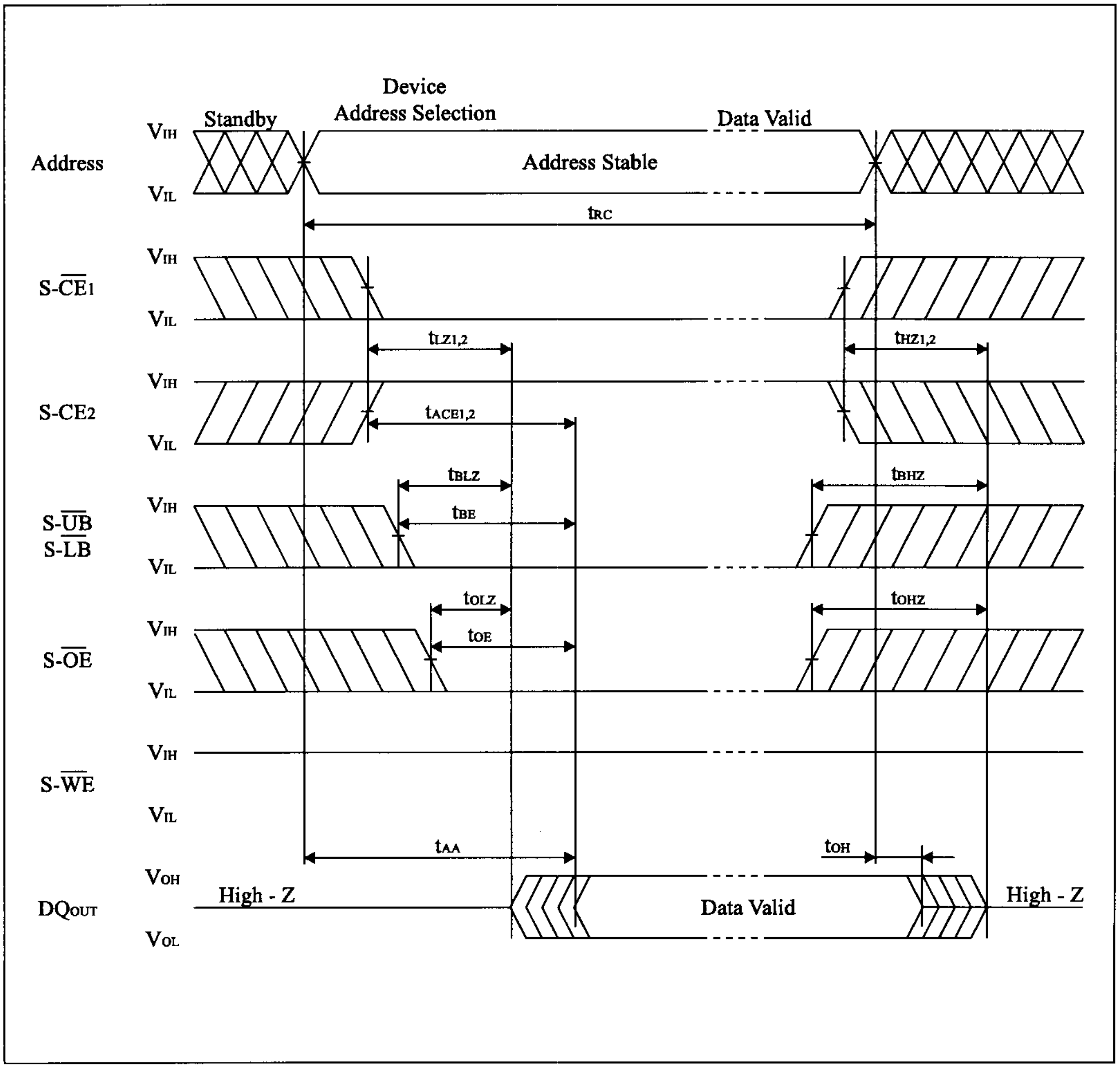
(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.3V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{WC}	Write cycle time		85		ns
t_{CW}	Chip enable to end of write		70		ns
t_{AW}	Address valid to end of write		70		ns
t_{BW}	Byte select time		70		ns
t_{AS}	Address setup time		0		ns
t_{WP}	Write pulse width		60		ns
t_{WR}	Write recovery time		0		ns
t_{DW}	Input data setup time		35		ns
t_{DH}	Input data hold time		0		ns
t_{OW}	S-$\overline{WE}$ High to output active	1	5		ns
t_{WZ}	S-$\overline{WE}$ Low to output in High-Z	1	0	30	ns

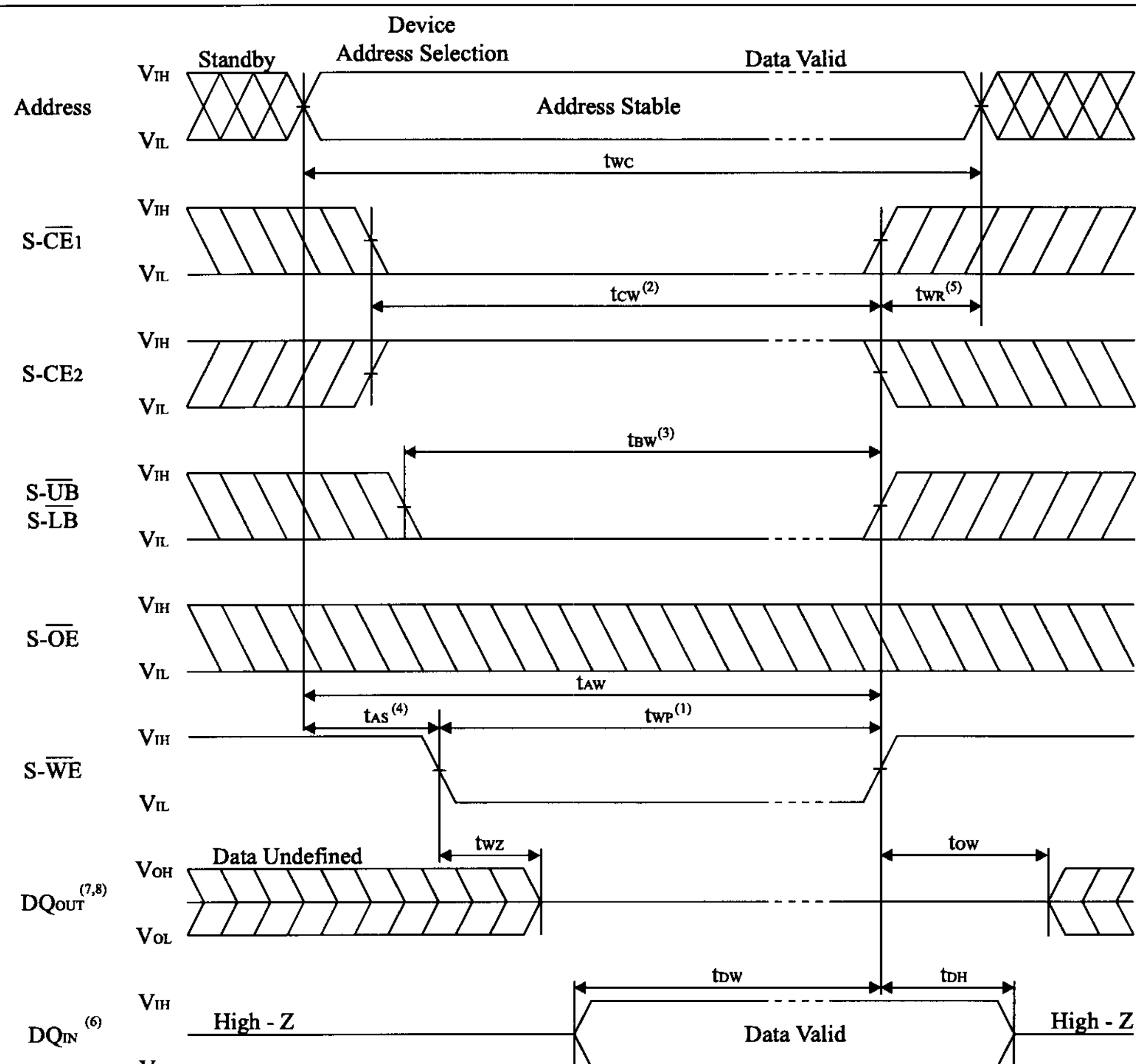
Note:
1. Active output to High-Z and High-Z to output active tests specified for a ±200mV transition from steady state levels into the test load.

13.4 SRAM AC Characteristics Timing Chart

Read cycle timing chart



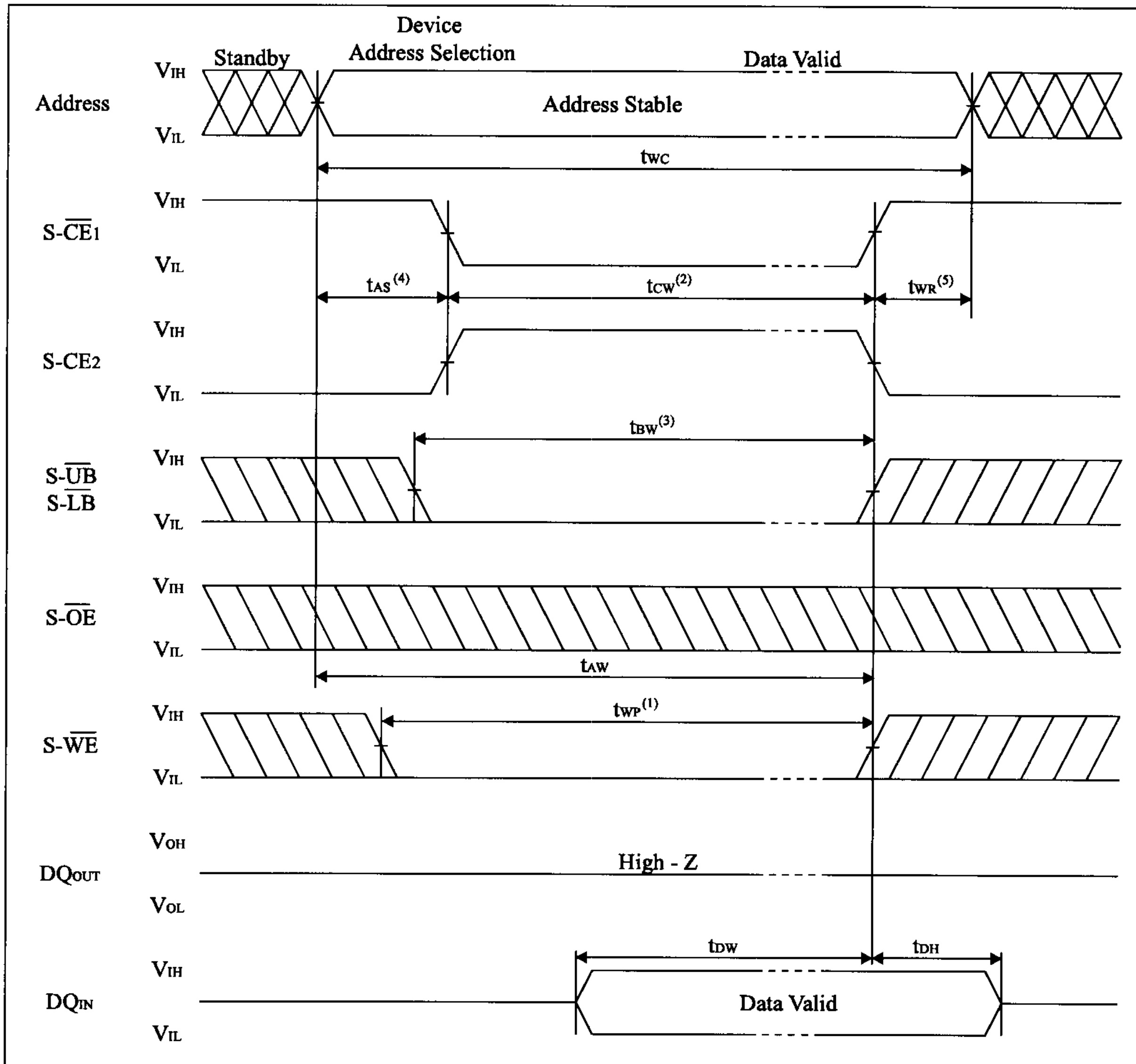
Write cycle timing chart (S-$\overline{WE}$ Controlled)



Notes:

1. A write occurs during the overlap of a low S-$\overline{CE}_1$, a high S-CE_2 and a low S-$\overline{WE}$.
   A write begins at the latest transition among S-$\overline{CE}_1$ going low, S-CE_2 going high and S-$\overline{WE}$ going low.
   A write ends at the earliest transition among S-$\overline{CE}_1$ going high, S-CE_2 going low and S-$\overline{WE}$ going high.
   t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of S-$\overline{CE}_1$ going low or S-CE_2 going high to the end of write.
3. t_{BW} is measured from the time of going low S-$\overline{UB}$ or low S-$\overline{LB}$ to the end of write.
4. t_{AS} is measured from the address valid to beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applies in case a write ends at S-$\overline{CE}_1$ going high, S-CE_2 going low or S-$\overline{WE}$ going high.
6. During this period DQ pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
7. If S-$\overline{CE}_1$ goes low or S-CE_2 goes high simultaneously with S-$\overline{WE}$ going low or after S-$\overline{WE}$ going low, the outputs remain in high impedance state.
8. If S-$\overline{CE}_1$ goes high or S-CE_2 goes low simultaneously with S-$\overline{WE}$ going high or before S-$\overline{WE}$ going high, the outputs remain in high impedance state.

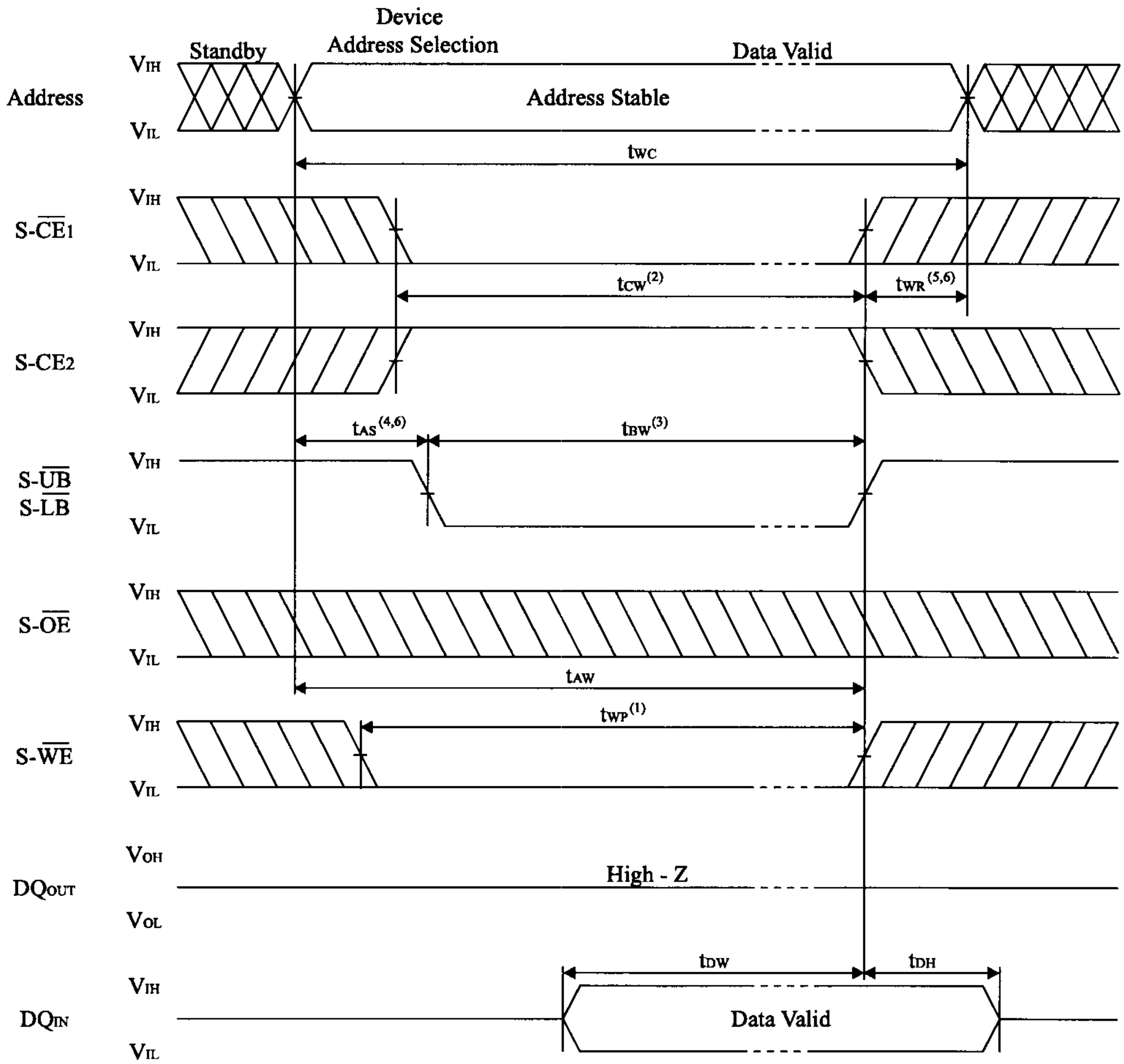
Write cycle timing chart (S-$\overline{CE}$ Controlled)



Notes:

1. A write occurs during the overlap of a low S-$\overline{CE}_1$, a high S-CE_2 and a low S-$\overline{WE}$.
   A write begins at the latest transition among S-$\overline{CE}_1$ going low, S-CE_2 going high and S-$\overline{WE}$ going low.
   A write ends at the earliest transition among S-$\overline{CE}_1$ going high, S-CE_2 going low and S-$\overline{WE}$ going high.
   t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of S-$\overline{CE}_1$ going low or S-CE_2 going high to the end of write.
3. t_{BW} is measured from the time of going low S-$\overline{UB}$ or low S-$\overline{LB}$ to the end of write.
4. t_{AS} is measured from the address valid to beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applies in case a write ends at S-$\overline{CE}_1$ going high, S-CE_2 going low or S-$\overline{WE}$ going high.

Wrire cycle timing chart (S-$\overline{UB}$, S-$\overline{LB}$ Controlled)



Notes:

1. A write occurs during the overlap of a low S-$\overline{CE}_1$, a high S-CE_2 and a low S-$\overline{WE}$.
   A write begins at the latest transition among S-$\overline{CE}_1$ going low, S-CE_2 going high and S-$\overline{WE}$ going low.
   A write ends at the earliest transition among S-$\overline{CE}_1$ going high, S-CE_2 going low and S-$\overline{WE}$ going high.
   t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of S-$\overline{CE}_1$ going low or S-CE_2 going high to the end of write.
3. t_{BW} is measured from the time of going low S-$\overline{UB}$ or low S-$\overline{LB}$ to the end of write.
4. t_{AS} is measured from the address valid to beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applies in case a write ends at S-$\overline{CE}_1$ going high, S-CE_2 going low or S-$\overline{WE}$ going high.
6. S-$\overline{UB}$ and S-$\overline{LB}$ need to make the time of start of a cycle, and an end "high" level for reservation of t_{AS} and t_{WR}.

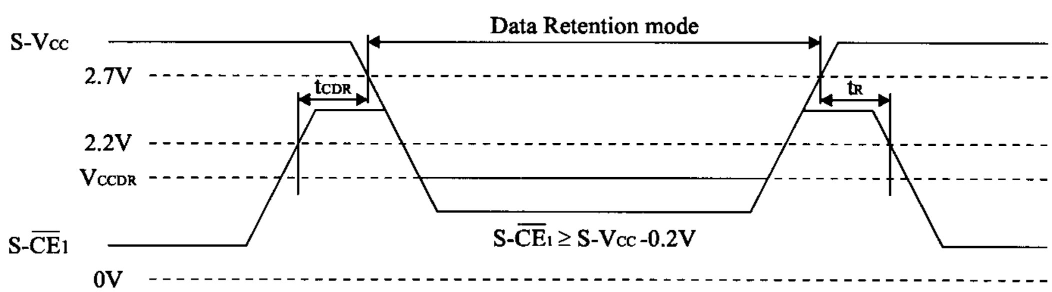
14. Data Retention Characteristics for SRAM

(T_A = -25°C to +85°C)

Symbol	Parameter	Note	Min.	Typ.[1]	Max.	Unit	Conditions
V_{CCDR}	Data Retention Supply voltage	2	1.5		3.3	V	S-CE_2 ≤ 0.2V or S-$\overline{CE}_1$ ≥ S-V_{CC} - 0.2V
I_{CCDR}	Data Retention Supply current	2		1	15	µA	S-V_{CC} = 3.0V S-CE_2 ≤ 0.2V or S-$\overline{CE}_1$ ≥ S-V_{CC} - 0.2V
t_{CDR}	Chip enable setup time		0			ns	
t_R	Chip enable hold time		t_{RC}			ns	

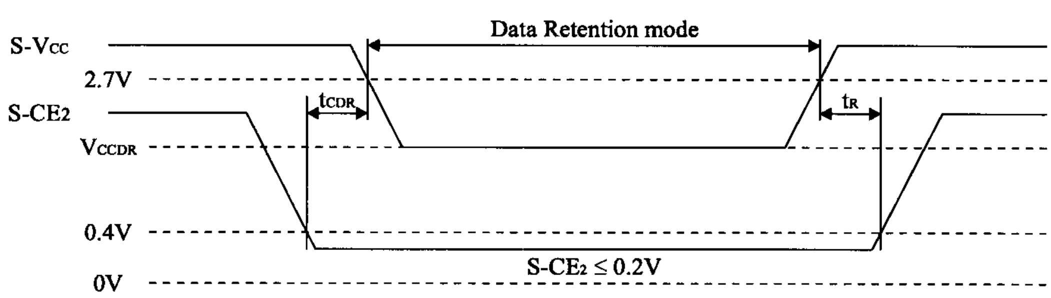
Notes
1. Reference value at T_A = 25°C, S-V_{CC} = 3.0V.
2. S-$\overline{CE}_1$ ≥ S-V_{CC} - 0.2V, S-CE_2 ≥ S-V_{CC} - 0.2V (S-$\overline{CE}_1$ controlled) or S-CE_2 ≤ 0.2V (S-CE_2 controlled).

Data Retention timing chart (S-$\overline{CE}_1$ Controlled)[1]



Note:
1. To control the data retention mode at S-$\overline{CE}_1$, fix the input level of S-CE_2 between "V_{CCDR} and V_{CCDR}-0.2V" or "0V and 0.2V" during the data retention mode.

Data Retention timing chart (S-CE_2 Controlled)



15. Notes

This product is a stacked CSP package that a 16M (x16) bit Flash Memory and a 4M (x16) bit SRAM are assembled into.

- Supply Power
  Maximum difference (between F-V_{CC} and S-V_{CC}) of the voltage is less than 0.3V.

- Power Supply and Chip Enable of Flash Memory and SRAM
  S-$\overline{CE}_1$ should not be "low" and S-CE_2 should not be "high" when F-$\overline{CE}$ is "low" simultaneously.
  If the two memories are active together, possibly they may not operate normally by interference noises or data collision on DQ bus.
  Both F-V_{CC} and S-V_{CC} are needed to be applied by the recommended supply voltage at the same time expect SRAM data retention mode.

- Power Up Sequence
  When turning on Flash memory power supply, keep F-$\overline{RP}$ "low". After F-V_{CC} reaches over 2.7V, keep F-$\overline{RP}$ "low" for more than 100nsec.

- Device Decoupling
  The power supply is needed to be designed carefully because one of the SRAM and the Flash Memory is in standby mode when the other is active. A careful decoupling of power supplies is necessary between SRAM and Flash Memory. Note peak current caused by transition of control signals (F-$\overline{CE}$, S-$\overline{CE}_1$, S-CE_2).

16. Flash Memory Data Protection

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems. Such noises, when induced onto F-$\overline{WE}$ signal or power supply, may be interpreted as false commands, causing undesired memory updating. To protect the data stored in the flash memory against unwanted writing, systems operating with the flash memory should have the following write protect designs, as appropriate.

■ The below describes data protection method.

1. Protecting data in specific block
   - By setting a F-$\overline{WP}$ to low, only the boot block can be protected against overwriting. Parameter and main blocks cannot be locked. System program, etc., can be locked by storing them in the boot block. For further information on setting/resetting of lock bit, and controlling of F-$\overline{WP}$ and F-$\overline{RP}$ refer to the specification. (See Chapter 5. Command Definitions for Flash Memory)

2. Data Protection through F-V_{CCW}
   - When the level of F-V_{CCW} is lower than V_{CCWLK} (lockout voltage), write operation on the flash memory is disabled. All blocks are locked and the data in the blocks are completely write protected. For the lockout voltage, refer to specification. (See Chapter 11. DC Electrical Characteristics)

■ Data Protection during voltage transition

3. Data protection thorough F-$\overline{RP}$
   - When the F-$\overline{RP}$ is kept low during power up and power down sequence, write operation on the flash memory is disabled, write protecting all blocks.
   - For the details of F-$\overline{RP}$ control, refer to the specification. (See Chapter 12. AC Electrical Characteristics for Flash Memory)

17. Design Considerations

1. Power Supply Decoupling

To avoid a bad effect to the system by flash memory power switching characteristics, each device should have a 0.1μF ceramic capacitor connected between its F-V_{CC} and GND and between its F-V_{CCW} and GND. Low inductance capacitors should be placed as close as possible to package leads.

2. F-V_{CCW} Trace on Printed Circuit Boards

Updating the memory contents of flash memories that reside in the target system requires that the printed circuit board designer pay attention to the F-V_{CCW} Power Supply trace. Use similar trace widths and layout considerations given to the F-V_{CC} power bus.

3. The Inhibition of Overwrite Operation

Please do not execute reprogramming "0" for the bit which has already been programed "0". Overwrite operation may generate unerasable bit.

In case of reprogramming "0" to the data which has been programed "1".
• Program "0" for the bit in which you want to change data from "1" to "0".
• Program "1" for the bit which has already been programmed "0".

For example, changing data from "1011110110111101" to "1010110110111100" requires "1110111111111110" programming.

4. Power Supply

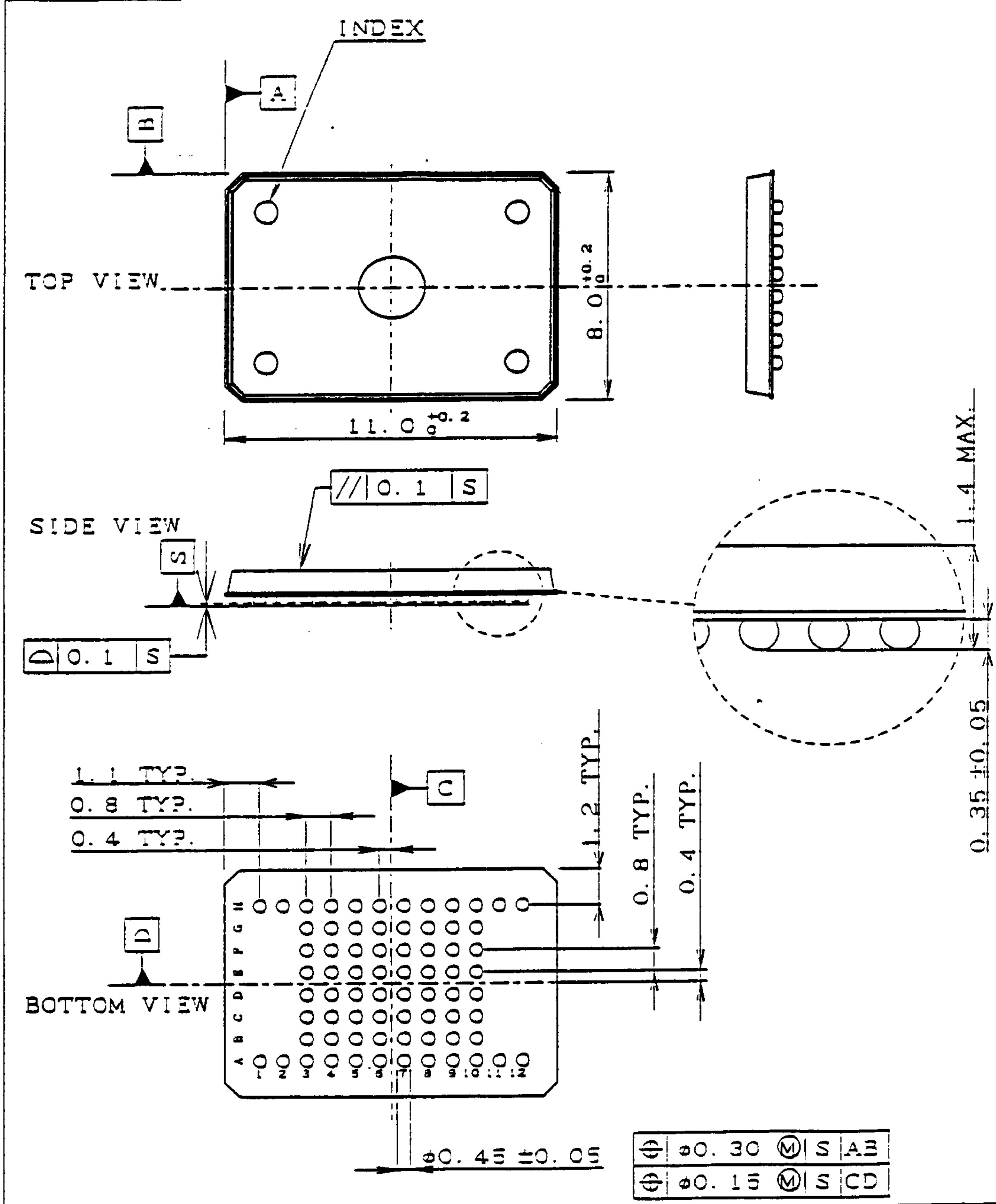
Block erase, full chip erase, word write and lock-bit configuration with an invalid F-V_{CCW} (See 11. DC Electrical Characteristics) produce spurious results and should not be attempted.
Device operations at invalid F-V_{CC} voltage (See Chapter 11.DC Electrical Characteristics) produce spurious results and should not be attempted.

18. Related Document Information[1]

Document No.	Document Name
FUM99902	LH28F800BJ, LH28F160BJ, LH28F320BJ Series Appendix

Note:
1.International customers should contact their local SHARP or distribution sales offices.

SHARP



尺度 SCALE 5/1

単位 UNIT 1=1/1mm

適用機種 APPLICABLE MODEL

端子マトリクス MATRIX 12 X 8

端子数 COUNTS 72

端子ピッチ PITCH 0.8

名称 NAME LCSP072-P-0811 (LFBGA072-P-0811)

コード CODE LCSP-GR-072-1-0811

図番 DRAWING No. AA2078

改訂日 DATE | 改訂記事 REVISE | 担当 CHARGE

日付 DATE 1998. 2. 10

設計 DESIGN | 製図 DRAW | 写図 TRACE | 検図 CHECK | 承認 APPROVE

SOTA | SOTA

シャープ株式会社 SHARP CORPORATION

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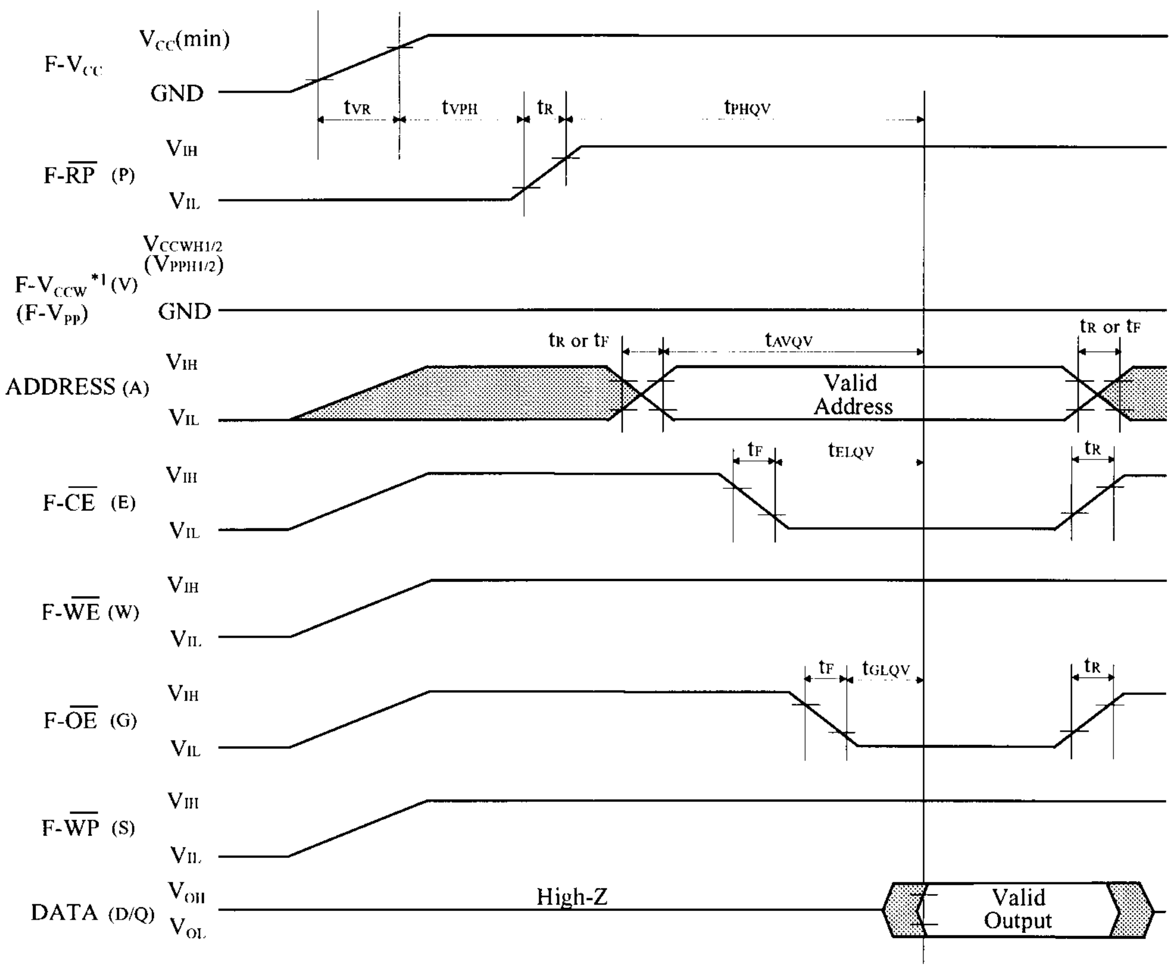
超LSI開発研究所 VLSI DEVELOPMENT LABORATORIES

生産技術開発部 PRODUCTION ENGINEERING DEPT.

A-1 RECOMMENDED OPERATING CONDITIONS

A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.



*1 To prevent the unwanted writes, system designers should consider the F-V_{CCW} (F-V_{PP}) switch, which connects F-V_{CCW} (F-V_{PP}) to GND during read operations and $V_{CCWH1/2}$ ($V_{PPH1/2}$) during write or erase operations. See the application note AP-007-SW-E for details.

Figure A-1. AC Timing at Device Power-Up

For the AC specifications t_{VR}, t_R, t_F in the figure, refer to the next page. See the "AC Electrical Characteristics for Flash Memory" described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

A-1.1.1 Rise and Fall Time

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{VR}	F-V_{CC} Rise Time	1	0.5	30000	µs/V
t_R	Input Signal Rise Time	1, 2		1	µs/V
t_F	Input Signal Fall Time	1, 2		1	µs/V

NOTES:

1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.
   t_R (Max.) and t_F (Max.) for F-RP are 50µs/V.

A-1.2 Glitch Noises

Do not input the glitch noises which are below V_{IH} (Min.) or above V_{IL} (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).

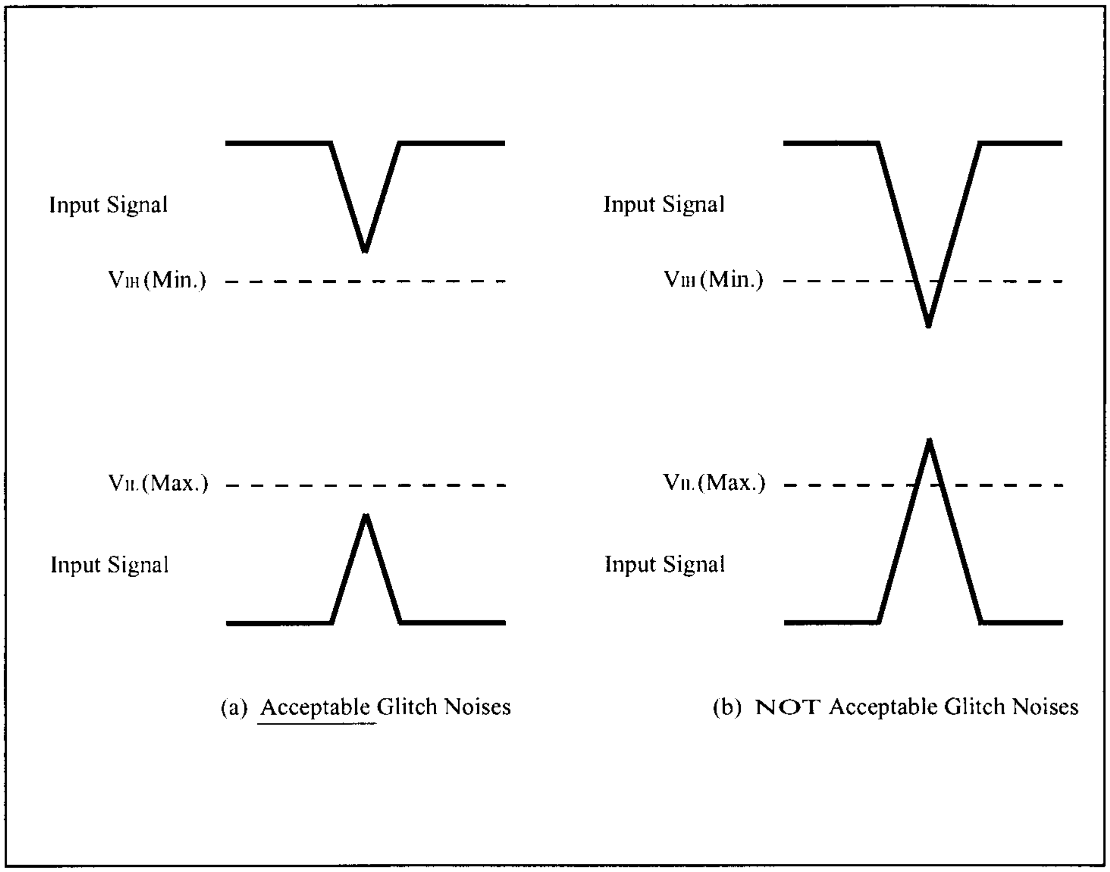


Figure A-2. Waveform for Glitch Noises

See the "DC Electrical Characteristics" described in specifications for V_{IH} (Min.) and V_{IL} (Max.).

A-2 RELATED DOCUMENT INFORMATION[1]

Document No.	Document Name
AP-001-SD-E	Flash Memory Family Software Drivers
AP-006-PT-E	Data Protection Method of SHARP Flash Memory
AP-007-SW-E	RP#, V_{PP} Electric Potential Switching Circuit

NOTE:
1. International customers should contact their local SHARP or distribution sales office.

SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE.

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