Dual/Quad 100MHz, Rail-to-Rail Input and Output, Ultralow Noise, Low Power Op Amps

April 2002

FEATURES

- **Low Noise Voltage: 1.9nV/√Hz (100kHz)**
- **Low Supply Current: 3mA/Amp Max**
- **Gain Bandwidth Product: 100MHz**
- **Low Distortion: –80dB at 1MHz**
- Low Offset Voltage: 500µV Max
- Wide Supply Range: 2.5V to 12.6V
- Input Common Mode Range Includes Both Rails
- Output Swings Rail-to-Rail
- Common Mode Rejection Ratio 90dB Typ
- Unity Gain Stable
- Low Noise Current: 0.75pA/√Hz
- Output Current: 30mA Min
- Dual in MSOP and SO-8 Packages
- Quad in SO-14 Package
- Operating Temperature Range –40°C to 85°C

APPLICATIONS

- Low Noise, Low Power Signal Processing
- Active Filters
- Rail-to-Rail Buffer Amplifiers
- Driving A/D Converters
- DSL Receivers
- Battery Powered/Battery Backed Equipment

DESCRIPTION

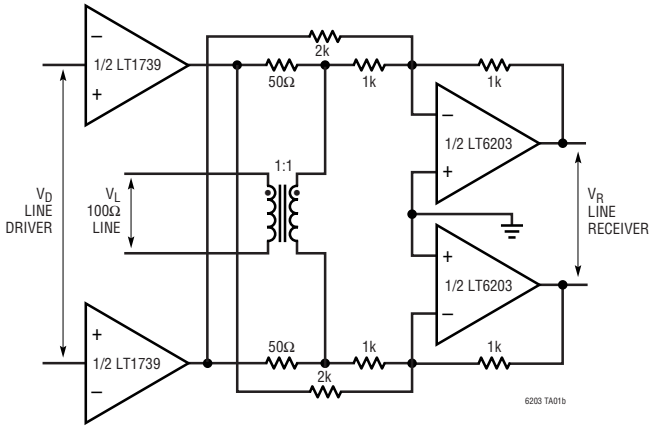
The LT®6203/LT6204 are dual/quad low noise, rail-to-rail input and output unity gain stable op amps that feature 1.9nV/√Hz noise voltage and draw only 2.5mA of supply current per amplifier. These amplifiers combine very low noise and supply current with a 100MHz gain bandwidth product, a 25V/µs slew rate, and are optimized for low supply signal conditioning systems.

The LT6203/LT6204 have an input range that includes both supply rails and an output that swings within 30mV of either supply rail to maximize the signal dynamic range in low supply applications. These amplifiers maintain their performance for supplies from 2.5V to 12.6V and are specified at 3V, 5V and ±5V supplies. Harmonic distortion is less than –80dBc at 1MHz making these amplifiers suitable in low power data acquisition systems.

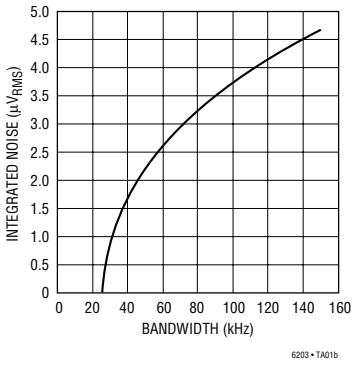
The LT6203 is available in 8-pin SO and MSOP packages with standard op amp pinouts. For compact layouts the quad LT6204 is available in the 14-pin SO package. These devices can be used as plug-in replacements for many op amps to improve input/output range and noise performance.

TYPICAL APPLICATION

Low Noise 4- to 2-Wire Local Echo Cancellation Differential Receiver



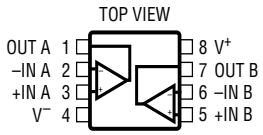
Line Receiver Integrated Noise 25kHz to 150kHz



ABSOLUTE MAXIMUM RATINGS (Note 1)

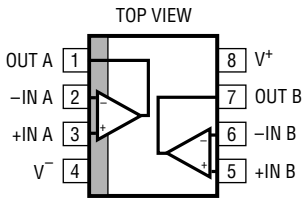
Total Supply Voltage (V^+ to V^-) 12.6V
Input Current (Note 2) ..... ±40mA
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4) ...–40°C to 85°C
Specified Temperature Range (Note 5) ....–40°C to 85°C
Junction Temperature ..... 150°C
Storage Temperature Range .....–65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



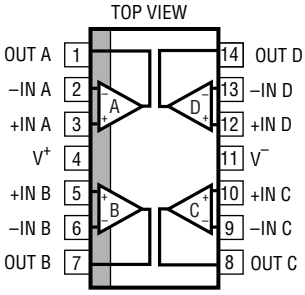
MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 250°C/W

ORDER PART NUMBER
LT6203CMS8 LT6203IMS8
MS8 PART MARKING
LTB2 LTB3



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 190°C/W

ORDER PART NUMBER
LT6203CS8 LT6203IS8
S8 PART MARKING
6203 6203I



S PACKAGE
14-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT6204CS LT6204IS

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_S = 5V, 0, V_{CM} =Half Supply		0.1	0.5	mV
		V_S = 3V, 0, V_{CM} = Half Supply		0.6	1.5	mV
		V_S = 5V, 0, V_{CM} = V^+ to V^-		0.8	2.5	mV
		V_S = 3V, 0, V_{CM} = V^+ to V^-		1.0	3.5	mV

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Input Offset Voltage Match (Channel-to-Channel)(Note 6)	V_{CM} = Half Supply V_{CM} = V^- to V^+		0.15 0.3	0.8 1.8	mV mV
I_B	Input Bias Current	V_{CM} = Half Supply V_{CM} = V^+ V_{CM} = V^-		–1.3 1.3 –3.3	–7.0 2.5 –8.8	µA µA µA
ΔI_B	I_B Shift	V_{CM} = V^- to V^+		4.7	11.3	µA
	I_B Match (Channel-to-Channel) (Note 6)			0.1	0.6	µA
I_{OS}	Input Offset Current	V_{CM} = Half Supply V_{CM} = V^+ V_{CM} = V^-		0.12 0.07 0.12	1 1 1.1	µA µA µA
	Input Noise Voltage	0.1Hz to 10Hz		600		nV_{P-P}
e_n	Input Noise Voltage Density	f = 100kHz, V_S = 5V f = 10kHz, V_S = 5V		2 2.9	 4.5	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 10kHz, V_S = 5V		0.75		$pA/\sqrt{Hz}$
	Input Resistance	Common Mode Differential Mode		4 12		MΩ kΩ
C_{IN}	Input Capacitance			2.8		pF
A_{VOL}	Large Signal Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k to V_S/2 V_S = 5V, V_O = 1V to 4V, R_L = 100 to V_S/2 V_S = 3V, V_O = 0.5V to 2.5V, R_L = 1k to V_S/2	40 8.0 17	70 14 40		V/mV V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = V^- to V^+ V_S = 5V, V_{CM} = 1.5V to 3.5V V_S = 3V, V_{CM} = V^- to V^+	60 80 56	83 100 80		dB dB dB
	CMRR Match (Channel-to-Channel)(Note 6)	V_S = 5V, V_{CM} = 1.5V to 3.5V	85	120		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 10V, V_{CM} = 0V	60	74		dB
	PSRR Match (Channel-to-Channel) (Note 6)	V_S = 2.5V to 10V, V_{CM} = 0V	70	100		dB
	Minimum Supply Voltage (Note 7)		2.5			V
V_{OL}	Output Voltage Swing LOW Saturation (Note 8)	No Load I_{SINK} = 5mA V_S = 5V, I_{SINK} = 20mA V_S = 3V, I_{SINK} = 15mA		5 85 240 185	30 190 460 350	mV mV mV mV
V_{OH}	Output Voltage Swing HIGH Saturation (Note 8)	No Load I_{SOURCE} = 5mA V_S = 5V, I_{SOURCE} = 20mA V_S = 3V, I_{SOURCE} = 15mA		25 90 325 225	75 210 600 410	mV mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3V	±30 ±25	±45 ±40		mA mA
I_S	Supply Current per Amp	V_S = 5V V_S = 3V		2.5 2.3	3.0 2.85	mA mA
GBW	Gain Bandwidth Product	Frequency = 1MHz		90		MHz
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k, V_O = 4V	17	24		V/µs
FPBW	Full Power Bandwidth (Note 10)	V_S = 5V, V_{OUT} = $3V_{P-P}$	1.8	2.5		MHz
t_S	Settling Time	0.1%, V_S = 5V, V_{STEP} = 2V, A_V = –1, R_L = 1k		175		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over 0°C < T_A < 70°C temperature range. V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_S = 5V, 0, V_{CM} = Half Supply	●		0.2	0.7	mV
		V_S = 3V, 0, V_{CM} = Half Supply	●		0.6	1.7	mV
		V_S = 5V, 0, V_{CM} = V^+ to V^-	●		0.7	3.0	mV
		V_S = 3V, 0, V_{CM} = V^+ to V^-	●		1.2	4.0	mV
V_{OS} TC	Input Offset Voltage Drift (Note 9)	V_{CM} = Half Supply	●		3.0	9.0	µV/°C
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)	V_{CM} = Half Supply	●		0.15	0.9	mV
		V_{CM} = V^- to V^+	●		0.5	2.3	mV
I_B	Input Bias Current	V_{CM} = Half Supply	●		–1.3	–7.0	µA
		V_{CM} = V^+	●		1.3	2.5	µA
		V_{CM} = V^-	●		–3.3	–8.8	µA
ΔI_B	I_B Shift	V_{CM} = V^- to V^+	●		4.7	11.3	µA
	I_B Match (Channel-to-Channel) (Note 6)		●		0.1	0.6	µA
I_{OS}	Input Offset Current	V_{CM} = Half Supply	●		0.15	1	µA
		V_{CM} = V^+	●		0.10	1	µA
		V_{CM} = V^-	●		0.15	1.1	µA
A_{VOL}	Large Signal Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k to V_S/2	●	35	60		V/mV
		V_S = 5V, V_O = 1.5V to 3.5V, R_L = 100 to V_S/2	●	6.0	12		V/mV
		V_S = 3V, V_O = 0.5V to 2.5V, R_L = 1k to V_S/2	●	15	36		V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = V^- to V^+	●	60	83		dB
		V_S = 5V, V_{CM} = 1.5V to 3.5V	●	78	97		dB
		V_S = 3V, V_{CM} = V^- to V^+	●	56	75		dB
	CMRR Match(Channel-to-Channel) (Note 6)	V_S = 5V, V_{CM} = 1.5V to 3.5V	●	83	100		dB
PSRR	Power Supply Rejection Ratio	V_S = 3V to 10V, V_{CM} = 0V	●	60	70		dB
	PSRR Match (Channel-to-Channel)(Note 6)	V_S = 3V to 10V, V_{CM} = 0V	●	70	100		dB
	Minimum Supply Voltage (Note 7)		●	3.0			V
V_{OL}	Output Voltage Swing LOW Saturation (Note 8)	No Load	●		5.0	35	mV
		I_{SINK} = 5mA	●		95	200	mV
		I_{SINK} = 15mA	●		260	365	mV
V_{OH}	Output Voltage Swing HIGH Saturation (Note 8)	No Load	●		50	100	mV
		I_{SOURCE} = 5mA	●		115	230	mV
		V_S = 5V, I_{SOURCE} = 20mA	●		360	635	mV
		V_S = 3V, I_{SOURCE} = 15mA	●		260	430	mV
I_{SC}	Short-Circuit Current	V_S = 5V	●	±20	±33		mA
		V_S = 3V	●	±20	±30		mA
I_S	Supply Current per Amp	V_S = 5V	●		3.1	3.85	mA
		V_S = 3V	●		2.75	3.50	mA
GBW	Gain Bandwidth Product	Frequency = 1MHz	●		87		MHz
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k, V_O = 4V	●	15	21		V/µs
FPBW	Full Power Bandwidth (Note 10)	V_S = 5V, V_{OUT} = $3V_{P-P}$	●	1.6	2.2		MHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over –40°C < T_A < 85°C temperature range. V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_S = 5V, 0, V_{CM} = Half Supply	●		0.2	0.8	mV
		V_S = 3V, 0, V_{CM} = Half Supply	●		0.6	2.2	mV
		V_S = 5V, 0, V_{CM} = V^+ to V^-	●		1.0	3.5	mV
		V_S = 3V, 0, V_{CM} = V^+ to V^-	●		1.4	4.5	mV
V_{OS} TC	Input Offset Voltage Drift (Note 9)	V_{CM} = Half Supply	●		3.0	9.0	µV/°C
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)	V_{CM} = Half Supply	●		0.3	1.0	mV
		V_{CM} = V^- to V^+	●		0.7	2.5	mV
I_B	Input Bias Current	V_{CM} = Half Supply	●		–1.3	–7.0	µA
		V_{CM} = V^+	●		1.3	2.5	µA
		V_{CM} = V^-	●		–3.3	–8.8	µA
ΔI_B	I_B Shift	V_{CM} = V^- to V^+	●		4.7	11.3	µA
	I_B Match (Channel-to-Channel) (Note 6)		●		0.1	0.6	µA
I_{OS}	Input Offset Current	V_{CM} = Half Supply	●		0.2	1	µA
		V_{CM} = V^+	●		0.2	1.1	µA
		V_{CM} = V^-	●		0.2	1.2	µA
A_{VOL}	Large Signal Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k to V_S/2	●	32	60		V/mV
		V_S = 5V, V_O = 1.5V to 3.5V, R_L = 100 to V_S/2	●	4.0	10		V/mV
		V_S = 3V, V_O = 0.5V to 2.5V,R_L = 1k to V_S/2	●	13	32		V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = V^- to V^+	●	60	80		dB
		V_S = 5V, V_{CM} = 1.5V to 3.5V	●	75	95		dB
		V_S = 3V, V_{CM} = V^- to V^+	●	56	75		dB
	CMRR Match (Channel-to-Channel) (Note 6)	V_S = 5V, V_{CM} = 1.5V to 3.5V	●	80	100		dB
PSRR	Power Supply Rejection Ratio	V_S = 3V to 10V, V_{CM} = 0V	●	60	70		dB
	PSRR Match (Channel-to-Channel) (Note 6)	V_S = 3V to 10V, V_{CM} = 0V	●	70	100		dB
	Minimum Supply Voltage (Note 7)		●	3.0			V
V_{OL}	Output Voltage Swing LOW Saturation (Note 8)	No Load	●		6	35	mV
		I_{SINK} = 5mA	●		95	210	mV
		I_{SINK} = 15mA	●		210	400	mV
V_{OH}	Output Voltage Swing HIGH Saturation (Note 8)	No Load	●		55	110	mV
		I_{SOURCE} = 5mA	●		125	240	mV
		V_S = 5V, I_{SOURCE} = 20mA	●		370	650	mV
		V_S = 3V, I_{SOURCE} = 15mA	●		270	450	mV
I_{SC}	Short-Circuit Current	V_S = 5V	●	±15	±25		mA
		V_S = 3V	●	±15	±23		mA
I_S	Supply Current per Amp	V_S = 5V	●		3.3	4.1	mA
		V_S = 3V	●		3.0	3.65	mA
GBW	Gain Bandwidth Product	Frequency = 1MHz	●		83		MHz
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k, V_O = 4V	●	12	17		V/µs
FPBW	Full Power Bandwidth (Note 10)	V_S = 5V, V_{OUT} = $3V_{P-P}$	●	1.3	1.8		MHz

ELECTRICAL CHARACTERISTICS

T_A = 25°C, $\pm V_S$ = ±5V, 0V; V_{CM} = V_{OUT} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = Half Supply V_{CM} = V^+ V_{CM} = V^-		1.0 2.6 2.3	2.2 5.0 5.0	mV mV mV
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)	V_{CM} = 0V V_{CM} = V^- to V^+		0.2 0.4	1.0 2.0	mV mV
I_B	Input Bias Current	V_{CM} = Half Supply V_{CM} = V^+ V_{CM} = V^-		–1.3 1.3 –3.8	–7.0 3.0 –9.5	µA µA µA
ΔI_B	I_B Shift	V_{CM} = V^- to V^+		5.3	12.5	µA
	I_B Match(Channel-to-Channel) (Note 6)			0.1	0.6	µA
I_{OS}	Input Offset Current	V_{CM} = Half Supply V_{CM} = V^+ V_{CM} = V^-		0.15 0.2 0.35	1 1.2 1.3	µA µA µA
	Input Noise Voltage	0.1Hz to 10Hz		600		nV_{P-P}
e_n	Input Noise Voltage Density	f = 100kHz f = 10kHz		1.9 2.8	 4.5	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 10kHz		0.75		$pA/\sqrt{Hz}$
	Input Resistance	Common Mode Differential Mode		4 12		MΩ kΩ
C_{IN}	Input Capacitance			2.8		pF
A_{VOL}	Large Signal Gain	V_O = ±4.5V, R_L = 1k V_O = ±2.5V, R_L = 100	75 11	130 19		V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = V^- to V^+ V_{CM} = –2V to 2V	65 85	85 98		dB dB
	CMRR Match (Channel-to-Channel)(Note 6)	V_{CM} = –2V to 2V	85	120		dB
PSRR	Power Supply Rejection Ratio	V_S = ±1.25V to ±5V	60	74		dB
	PSRR Match (Channel-to-Channel)(Note 6)	V_S = ±1.25V to ±5V	70	100		dB
V_{OL}	Output Voltage Swing LOW Saturation (Note 8)	No Load I_{SINK} = 5mA I_{SINK} = 20mA		5 87 245	30 190 460	mV mV mV
V_{OH}	Output Voltage Swing HIGH Saturation (Note 8)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 20mA		40 95 320	95 210 600	mV mV mV
I_{SC}	Short-Circuit Current		±30	±40		mA
I_S	Supply Current per Amp			2.8	3.5	mA
GBW	Gain Bandwidth Product	Frequency = 1MHz	72	100		MHz
SR	Slew Rate	A_V = –1, R_L = 1k, V_O = 4V	18	25		V/µs
FPBW	Full Power Bandwidth (Note 10)	V_{OUT} = $3V_{P-P}$	1.9	2.6		MHz
t_S	Settling Time	0.1%, V_{STEP} = 2V, A_V = –1, R_L = 1k		160		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over 0°C < T_A < 70°C temperature range. V_S = ±5V, 0V; V_{CM} = V_{OUT} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = Half Supply	●		1.6	2.8	mV
		V_{CM} = V^+	●		3.2	6.0	mV
		V_{CM} = V^-	●		2.8	5.5	mV
V_{OS} TC	Input Offset Voltage Drift (Note 9)	V_{CM} = Half Supply	●		3.0	9.0	µV/°C
	Input Offset Voltage Match (Channel-to-Channel)(Note 6)	V_{CM} = 0V	●		0.2	1.0	mV
		V_{CM} = V^- to V^+	●		0.5	2.2	mV
I_B	Input Bias Current	V_{CM} = Half Supply	●		–1.4	–7.0	µA
		V_{CM} = V^+	●		1.8	3.6	µA
		V_{CM} = V^-	●		–4.3	–10	µA
ΔI_B	I_B Shift	V_{CM} = V^- to V^+	●		5.4	13	µA
	I_B match(Channel-to-Channel)(Note 6)		●		0.15	0.7	µA
I_{OS}	Input Offset Current	V_{CM} = Half Supply	●		0.1	1	µA
		V_{CM} = V^+	●		0.2	1.2	µA
		V_{CM} = V^-	●		0.4	1.4	µA
A_{VOL}	Large Signal Gain	V_O = ±4.5V, R_L = 1k	●	70	120		V/mV
		V_O = ±2.5V, R_L = 100	●	10	18		V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = V^- to V^+	●	65	84		dB
		V_{CM} = –2V to 2V	●	83	95		dB
	CMRR Match (Channel-to-Channel) (Note 6)	V_{CM} = –2V to 2V	●	83	110		dB
PSRR	Power Supply Rejection Ratio	V_S = ±1.5V to ±5V	●	60	70		dB
	PSRR Match (Channel-to-Channel)(Note 6)	V_S = ±1.5V to ±5V	●	70	100		dB
V_{OL}	Output Voltage Swing LOW Saturation (Note 8)	No Load	●		6	30	mV
		I_{SINK} = 5mA	●		95	200	mV
		I_{SINK} = 15mA	●		210	400	mV
V_{OH}	Output Voltage Swing HIGH Saturation (Note 8)	No Load	●		65	120	mV
		I_{SOURCE} = 5mA	●		125	240	mV
		I_{SOURCE} = 20mA	●		350	625	mV
I_{SC}	Short-Circuit Current		●	±25	±34		mA
I_S	Supply Current per Amp		●		3.5	4.3	mA
GBW	Gain Bandwidth Product	Frequency = 1MHz	●		95		MHz
SR	Slew Rate	A_V = –1, R_L = 1k, V_O = 4V	●	16	22		V/µs
FPBW	Full Power Bandwidth (Note 10)	V_{OUT} = $3V_{P-P}$	●	1.7	2.3		MHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over –40°C < T_A < 85°C temperature range. V_S = ±5V, 0V; V_{CM} = V_{OUT} = 0V, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = Half Supply	●		1.7	3.0	mV
		V_{CM} = V^+	●		3.8	6.5	mV
		V_{CM} = V^-	●		3.5	6.0	mV
V_{OS} TC	Input Offset Voltage Drift (Note 9)	V_{CM} = Half Supply	●		3.0	9.0	µV/°C
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)	V_{CM} = 0V	●		0.3	1.0	mV
		V_{CM} = V^- to V^+	●		0.6	2.5	mV
I_B	Input Bias Current	V_{CM} = Half Supply	●		–1.4	–7.0	µA
		V_{CM} = V^+	●		1.8	3.6	µA
		V_{CM} = V^-	●		–4.5	–10	µA
ΔI_B	I_B Shift	V_{CM} = V^- to V^+	●		5.4	13	µA
	I_B Match (Channel-to-Channel) (Note 6)		●		0.15	0.7	µA
I_{OS}	Input Offset Current	V_{CM} = Half Supply	●		0.15	1	µA
		V_{CM} = V^+	●		0.3	1.2	µA
		V_{CM} = V^-	●		0.5	1.6	µA
A_{VOL}	Large Signal Gain	V_O = ±4.5V, R_L = 1k	●	60	110		V/mV
		V_O = ±2.5V R_L = 100	●	6.0	13		V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = V^- to V^+	●	65	84		dB
		V_{CM} = –2V to 2V	●	80	95		dB
	CMRR Match (Channel-to-Channel) (Note 6)	V_{CM} = –2V to 2V	●	80	110		dB
PSRR	Power Supply Rejection Ratio	V_S = ±1.5V to ±5V	●	60	70		dB
	PSRR Match (Channel-to-Channel)(Note 6)	V_S = ±1.5V to ±5V	●	70	100		dB
V_{OL}	Output Voltage Swing LOW Saturation (Note 8)	No Load	●		7	32	mV
		I_{SINK} = 5mA	●		98	205	mV
		I_{SINK} = 15mA	●		260	500	mV
V_{OH}	Output Voltage Swing HIGH Saturation (Note 8)	No Load	●		70	130	mV
		I_{SOURCE} = 5mA	●		130	250	mV
		I_{SOURCE} = 20mA	●		360	640	mV
I_{SC}	Short-Circuit Current		●	±15	±25		mA
I_S	Supply Current per Amp		●		3.8	4.5	mA
GBW	Gain Bandwidth Product	Frequency = 1MHz	●		90		MHz
SR	Slew Rate	A_V = –1, R_L = 1k, V_O = 4V	●	13	18		V/µs
FPBW	Full Power Bandwidth (Note 10)	V_{OUT} = $3V_{P-P}$	●	1.4	1.9		MHz

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: Inputs are protected by back-to-back diodes and diodes to each supply. If the inputs are taken beyond the supplies or the differential input voltage exceeds 0.7V, the input current must be limited to less than 40mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LT6203C/LT6203I and LT6204C/LT6204I are guaranteed functional over the temperature range of –40°C and 85°C.

Note 5: The LT6203C/LT6204C are guaranteed to meet specified performance from 0°C to 70°C. The LT6203C/LT6204C are designed, characterized and expected to meet specified performance from –40°C to 85°C, but are not tested or QA sampled at these temperatures. The LT6203I/LT6204I are guaranteed to meet specified performance from –40°C to 85°C.

Note 6: Matching parameters are the difference between the two amplifiers A and D and between B and C of the LT6204; between the two amplifiers of the LT6203. CMRR and PSRR match are defined as follows: CMRR and PSRR are measured in µV/V on the identical amplifiers. The difference is calculated between the matching sides in µV/V. The result is converted to dB.

Note 7: Minimum supply voltage is guaranteed by power supply rejection ratio test.

Note 8: Output voltage swings are measured between the output and power supply rails.

Note 9: This parameter is not 100% tested.

Note 10: Full-power bandwidth is calculated from the slew rate: FPBW = $SR/2\pi V_P$

APPLICATIONS INFORMATION

Amplifier Characteristics

Figure 1 shows a simplified schematic of the LT6203/LT6204, which has two input differential amplifiers in parallel that are biased on simultaneously when the common mode voltage is at least 1.5V from either rail. This topology allows the input stage to swing from the positive supply voltage to the negative supply voltage. As the common mode voltage swings beyond V_{CC}-1.5V, current source I1 saturates and current in Q1/Q4 is zero. Feedback is maintained through the Q2/Q3 differential amplifier, but with an input g_m reduction of 1/2. A similar effect occurs with I2 when the common mode voltage swings within 1.5V of the negative rail. The effect of the g_m reduction is a shift in the V_{OS} as I1 or I2 saturate.

Input bias current normally flows out of the + and – inputs. The magnitude of this current increases when the input common mode voltage is within 1.5V of the negative rail, and only Q1/Q4 are active. The polarity of this current reverses when the input common mode voltage is within 1.5V of the positive rail and only Q2/Q3 are active.

The second stage is a folded cascode and current mirror that converts the input stage differential signals to a single ended output. Capacitor C1 reduces the unity cross frequency and improves the frequency stability without degrading the gain bandwidth of the amplifier. The differential drive generator supplies current to the output transistors that swing from rail-to-rail.

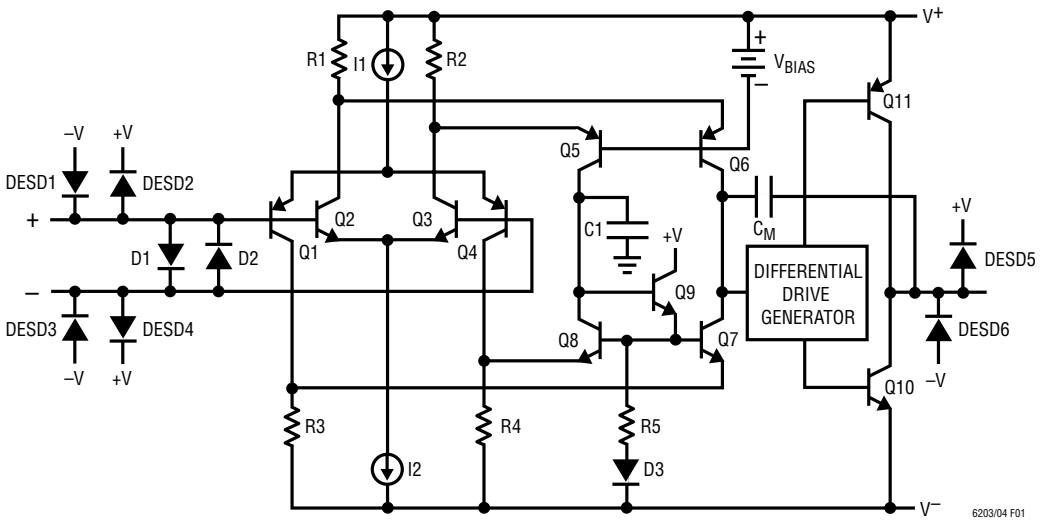


Figure 1. Simplified Schematic

APPLICATIONS INFORMATION

Input Protection

There are back-to-back diodes, D1 and D2, across the + and – inputs of these amplifiers to limit the differential input voltage to ±0.7V. The inputs of the LT6203/LT6304 do not have internal resistors in series with the input transistors. This technique is often used to protect the input devices from over voltage that causes excessive currents to flow. The addition of these resistors would significantly degrade the low noise voltage of these amplifiers. For instance, a 100Ω resistor in series with each input would generate 1.8nV/$\sqrt{Hz}$ of noise, and the total amplifier noise voltage would rise from 1.9nV/$\sqrt{Hz}$ to 2.6nV/$\sqrt{Hz}$. Once the input differential voltage exceeds ±0.7V, steady state current conducted though the protection diodes should be limited to ±40mA. This implies 25Ω of protection resistance per volt of continuous overdrive beyond ±0.7V. The input diodes are rugged enough to handle transient currents due to amplifier slew rate overdrive or momentary clipping without these resistors.

Figure 2 shows the input and output waveforms of the LT6203 driven into clipping while connected in a gain of A_V = 1. In this photo, the input signal generator is clipping at ±35mA, and the output transistors supply this generator current through the protection diodes.

ESD

The LT6203/LT6204 have reverse-biased ESD protection diodes on all inputs and outputs as shown in Figure 1. If these pins are forced beyond either supply, unlimited current will flow through these diodes. If the current is transient and limited to one hundred milliamps or less, no damage to the device will occur.

Noise

The noise voltage of the LT6203/LT6204 is equivalent to that of a 225Ω resistor, and for the lowest possible noise it is desirable to keep the source and feedback resistors at or below this value, i.e. $R_S + R_G||R_{FB} \leq 225\Omega$. With $R_S + R_G||R_{FB} = 225\Omega$ the total noise of the amplifier is: $e_n = \sqrt{(1.9nV)^2 + (1.9nV)^2} = 2.7nV$. Below this resistance value, the amplifier dominates the noise, but in the resistance region between 225Ω and approximately 10kΩ, the noise is dominated by the resistor thermal noise. As the total resistance is further increased, beyond 10k, the noise current multiplied by the total resistance eventually dominates the noise.

The product of $e_n \bullet I_{SUPPLY}$ is an interesting way to gauge low noise amplifiers. Many low noise amplifiers with low e_n have high I_{SUPPLY} current. In applications that require low noise with the lowest possible supply current, this product can prove to be enlightening. The LT6203/LT6204 have an e_n, I_{SUPPLY} product of 4.5 per amplifier, yet it is common to see amplifiers with similar noise specifications have an $e_n \bullet I_{SUPPLY}$ product of 10 to 30.

For a complete discussion of amplifier noise, see the LT1028 data sheet.

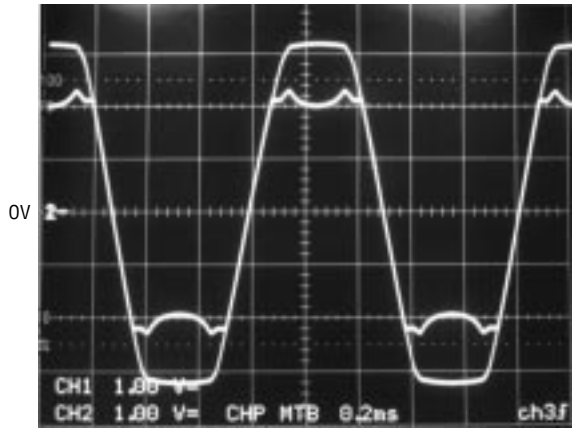
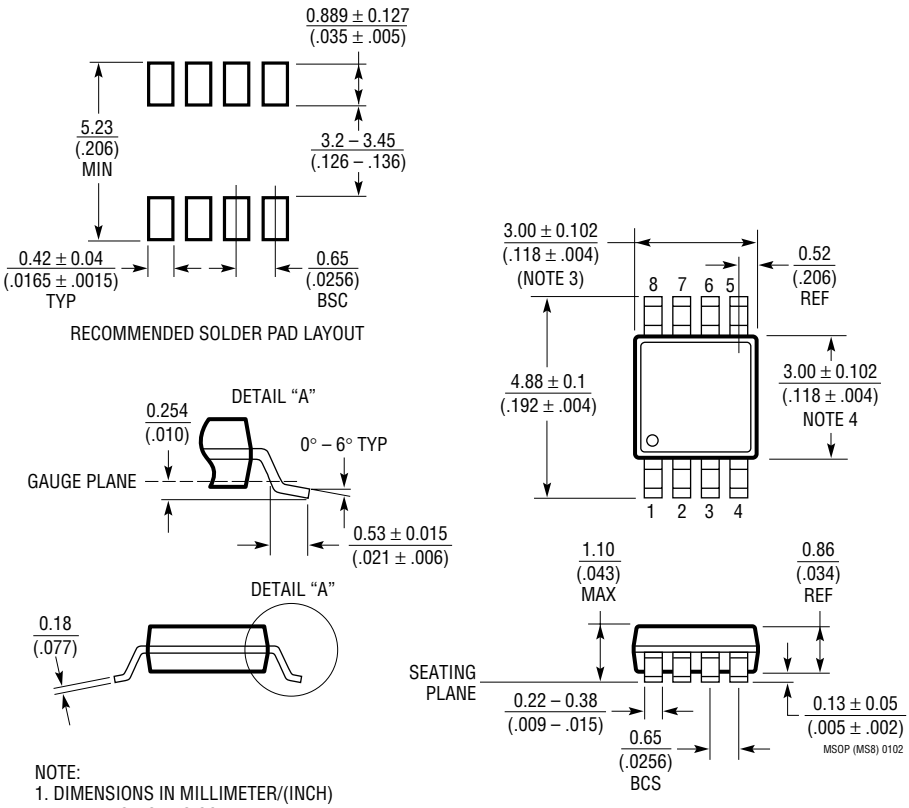


Figure 2. V_S = ±2.5V, A_V = 1 with Large Overdrive

PACKAGE DESCRIPTION

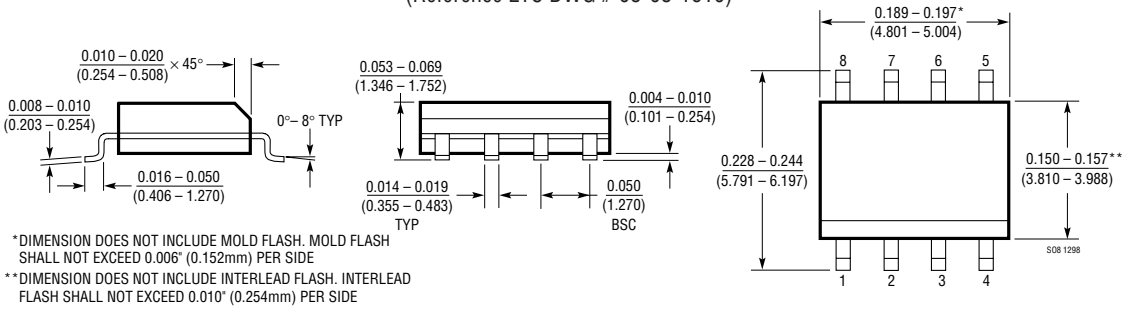
MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

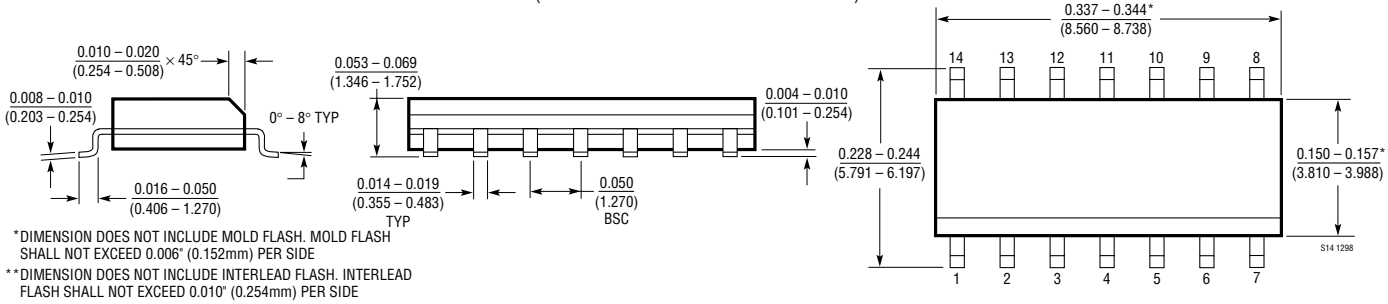
PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S Package
14-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1028	Single, Ultra Low Noise 50MHz Op Amp	1.1nV/$\sqrt{Hz}$
LT1677	Single, Low Noise Rail-to-Rail Amplifier	3V Operation, 2.5mA, 4.5nV/$\sqrt{Hz}$, 60µV Max V_{OS}
LT1722/LT1723/LT1724	Single/Dual/Quad Low Noise Precision Op Amp	70V/µs Slew Rate, 400µV Max V_{OS}, 3.8nV/$\sqrt{Hz}$, 3.7mA
LT1806/LT1807	Single/Dual, Low Noise 325MHz Rail-to-Rail Amplifier	2.5V Operation, 550µV Max V_{OS}, 3.5nV/$\sqrt{Hz}$

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT/TP 0402 1.5K • PRINTED IN USA