LS7060C
LS7061C

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32 BIT BINARY UP COUNTER WITH BYTE MULTIPLEXED THREE-STATE OUTPUTS

ADVANCE INFORMATION

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FEATURES:

- DC to 50MHz Count Frequency
- Byte Multiplexer
- DC to 10MHz Byte Output Scan Frequency
- +4.75V to +5.25V Operation (V_{DD} - V_{SS})
- Three-State Data Outputs; Bus, TTL and CMOS Compatible
- Inputs TTL and CMOS Compatible
- Unique Cascade Feature Allows Multiplexing of Successive Bytes of Data in Sequence in Multiple Counter Systems
- Low Power Dissipation
- LS7060C (DIP), LS7060C-S (SOIC) - See Figure 1
- LS7061C (DIP), LS7061C-S (SOIC) - See Figure 2

DESCRIPTION:

The LS7060C/LS7061C are CMOS Silicon Gate, 32 bit Up Counters. The ICs include latches, multiplexer, byte output sequencer, eight three-state binary data output drivers and output cascading logic.

DESCRIPTION OF OPERATION:

32 BIT BINARY UP COUNTER - LS7060C (LS7061C)

The 32 bit static ripple through counter increments on the negative edge of the input count pulse. Maximum ripple time is 20ns transition count of 32 ones to 32 zeros.
Guaranteed count frequency is DC to 50MHz.
See Figure 9A (9B) for Block Diagram.

$\overline{\text{COUNT}}$, $\overline{\text{ALT COUNT}}$ (LS7060C)

Input count pulses to the 32 bit counter may be applied through either of these two inputs. The $\overline{\text{ALT COUNT}}$ input circuitry contains a Schmitt trigger network which allows proper counting with "infinitely" long clock edges. A high applied to either of these two inputs inhibits counting.

$\overline{\text{COUNT}}$ (LS7061C)

Input count pulses to the 32 bit counter may be applied through this input. This input is the most significant bit of the external data byte.

$\overline{\text{RESET}}$

All 32 counter bits are reset to zero when $\overline{\text{RESET}}$ is brought low for a minimum of 20ns. $\overline{\text{RESET}}$ must be high for a minimum of 10ns before next valid count can be recorded.

$\overline{\text{TEST COUNT}}$

Count pulses may be applied to the last 16 bits of the binary counter through this input, as long as Bit 16 of the counter is a low. The counter advances on the negative transition of these pulses. This input is intended to be used for test purposes.

NOTE: LS7060C and LS7061C can directly replace LS7060 and LS7061 in all existing applications.

PIN ASSIGNMENT - TOP VIEW

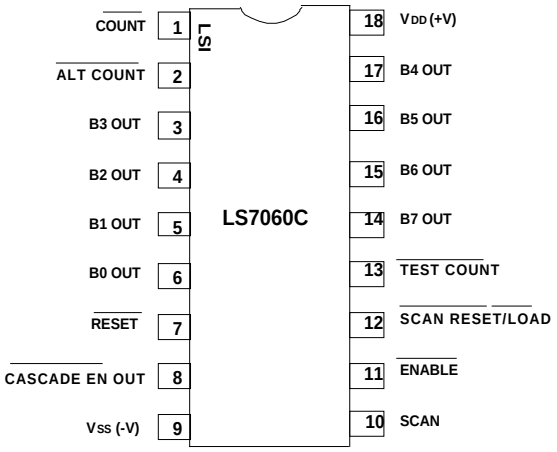


FIGURE 1

PIN ASSIGNMENT - TOP VIEW

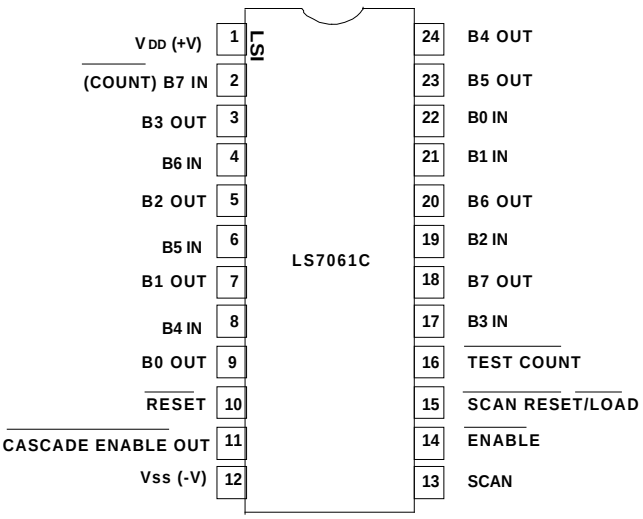


FIGURE 2

LATCHES

32 bits of latch are provided for storage of counter data for the LS7060C. 40 bits of latch are provided for the LS7061C of which eight are for storage of a high speed external prescaling counter and the remaining 32 are for the contents of the chip counter data. All latches are loaded when the $\overline{\text{LOAD}}$ input is brought low for a minimum of 10ns and kept low until a minimum of 20ns has elapsed from previous negative edge of count pulse (ripple time). Storage of valid data occurs when LOAD is brought high for a minimum of 20ns before next negative edge of count pulse or $\overline{\text{RESET}}$.

SCAN COUNTER AND DECODER
The scan counter is reset to the least significant byte position (State 1) when SCAN RESET input is brought low for a minimum of 10ns. The scan counter is enabled for counting as long as the ENABLE input is held low. The counter advances to the next significant byte position on each negative transition of the SCAN pulse. When the scan counter advances to State 5 for the LS7060C or Stage 6 for the LS7061C it disables the Output Drivers and stops in that state until SCAN RESET is again brought low.

SCAN
When the scan counter is enabled, each negative transition of this input advances the scan counter to its next state. When SCAN is low the Data Outputs are disabled. When SCAN is brought high the Data Outputs are enabled and present the latched counter data corresponding to the present state of the scan counter. Therefore, in microprocessor applications, the Data Output Bus may be utilized for other activities while new data is propagating to the outputs. This positive SCAN pulse can be viewed as a "Place the next byte on my bus" instruction from the microprocessor. Minimum positive and negative pulse widths of 10ns for the SCAN signal are required for scan counter operation.

SCAN RESET/LOAD
When this input is brought low for a minimum of 10ns, the scan counter is reset to State 1, the least significant byte position, and the latches are simultaneously loaded with new count information.

ENABLE
When this input is high, the scan counter and the Data Outputs are disabled. When ENABLE is low, the scan counter and Data Outputs are enabled for normal operation. Transition of this input should only be made while the SCAN input is in a low state in order to prevent false clocking of the scan counter.

CASCADE ENABLE
This output is normally high. It transitions low and stays low when the scan counter advances to State 5 for LS7060C and State 6 for LS7061C. In a multiple counter system this output is connected to the ENABLE input of the next counter in the cascade string. The SCAN input and SCAN RESET/LOAD input are carried to all the counters in the "Cascade". Counter 1 then presents its bytes of data to the Output Bus on each positive transition of the SCAN pulse as previously discussed. When State 5 for LS7060C or State 6 for LS7061C of Counter 1 is achieved, Counter 2 presents its data to the Output Bus. This sequence continues until all counters in the cascade have been addressed. See Figure 5 for an illustration of a 3 device cascade design. This output is TTL and CMOS compatible.

THREE-STATE DATA OUTPUT DRIVERS
The eight Data Output Drivers are disabled when either ENABLE input is high, the scan counter is in State 5 for LS7060C and State 6 for LS7061C, or the SCAN input is low. The Output Drivers are TTL and Bus compatible.

ABSOLUTE MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNIT
StorageTemperature	T_{STG}	-55 to +150	°C
Operating Temperature	T_A	0 to +70	°C
Voltage (any pin to V_{SS})	V_{IN}	+10 to -0.3	V

DC ELECTRICAL CHARACTERISTICS:
(V_{DD} = +5V ± 5%, V_{SS} = 0V, T_A = 0°C to +70°C unless otherwise noted.)

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITIONS
Quiescent Power Supply Current	I_{DD}	-	0.5	mA	V_{DD} = Max, Outputs No Load, Ø Frequency
Power Supply Current	I_{DD}	4	-	mA	15 MHz Operating Frequency V_{DD} = Max, Outputs No Load
Power Supply Current	I_{DD}	-	8	mA	At Maximum Operating Frequency V_{DD} = Max, Outputs No Load
Input High Voltage	V_{IH}	+3.5	V_{DD}	V	-
Input Low Voltage	V_{IL}	0	+0.6	V	-
Output High Voltage					
CASCADE ENABLE	V_{OH}	+2.4	-	V	I_O = -6mA, V_{DD} = Min
B0 - B7	V_{OH}	+2.4	-	V	I_O = -33mA, V_{DD} = Min
Output Low Voltage					
CASCADE ENABLE	V_{OL}	-	+0.4	V	I_O = 3mA, V_{DD} = Min
B0 - B7	V_{OL}	-	+0.4	V	I_O = 10mA, V_{DD} = Min
Output Source Current	Isource	-34	-	mA	V_O = +1.2V, V_{DD} = Min
B0 - B7 Outputs		-36	-	mA	V_O = +0.8V, V_{DD} = Min
		-38	-	mA	V_O = +0.4V, V_{DD} = Min
Output Sink Current	Isink	25	-	mA	V_O = +1.2V, V_{DD} = Min
B0 - B7 Outputs		20	-	mA	V_O = +0.8V, V_{DD} = Min
		10	-	mA	V_O = +0.4V, V_{DD} = Min
Output Leakage Current B0 - B7 (Off State)	I_{OL}	-	10	nA	V_O = +.4V to +2.4V, V_{DD} = Min
Input Capacitance	C_{IN}	-	6	pF	T_A = 25°C, f = 1MHz
Output Capacitance	C_{OUT}	-	12	pF	T_A = 25°C, f = 1MHz
Input Leakage Current ENABLE, RESET, SCAN	I_{LI}	-	10	nA	V_{DD} = Max

	SYMBOL	MIN	MAX	UNIT	CONDITIONS
INPUT CURRENT					
*SCAN RESET/LOAD	I_{IH}	-	-3.5	µA	V_{DD} = Max, V_{IH} = +3.5V
	I_{IL}	-	-5	µA	V_{DD} = Max, V_{IL} = 0V
**All Count inputs	I_{IH}	-	5	µA	V_{DD} = Max, V_{IH} = +3.5V
	I_{IL}	-	1	µA	V_{DD} = Max, V_{IL} = 0.35V

*Input has internal pull-up resistor to V_{DD}
** Inputs have internal pull-down resistor to V_{SS}

DYNAMIC ELECTRICAL CHARACTERISTICS:
(V_{DD} = +5V ± 5%, V_{SS} = 0v, T_A = 0˚C to +70˚C unless otherwise noted.)

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITIONS
Count Frequency (All Count inputs)	fc	DC	50	MHz	-
Count Pulse Width (All Count Inputs)	t_{CPW}	10	-	ns	Measured at 50% point, Max tr, t_f = 1ns
Count Ripple Time	t_{CR}	-	20	ns	Transition from 32 ones to 32 zeros from negative edge of count pulse
Reset Pulse Width (All Counter Stages Fully Reset)	t_{RPW}	20	-	ns	Measured at 50% point Max t_r, t_f = 10ns
RESET Removal Time (Reset Removed From All Counter Stages)	t_{RR}	-	10	ns	Measured from RESET signal at V_{IH}
SCAN Frequency	f_{SC}	-	10	MHz	
SCAN Pulse Width	t_{SCPW}	50	-	ns	Measured at 50% point Max t_r, t_f = 10ns
SCAN RESET/LOAD Pulse Width (All latches loaded and Scan Counter Reset to Least Significant Byte)	t_{RSCPW}	10	-	ns	Measured at 50% point Max t_r, t_f = 5ns
SCAN RESET/LOAD Removal Time (Reset Removed from Scan Counter; Load Command Removed From Latches)	t_{RSCR}	-	10	ns	Measured from SCAN RESET/LOAD at V_{IH}
Output Disable Delay Time (B0 - B7)	t_{DOD}	-	5	ns	Transition to Output High Impedance State Measured From Scan at V_{IL} or ENABLE at V_{IH}
Output ENABLE Delay Time (B0 - B7)	t_{DOE}	-	5	ns	Transition to Valid On State Measured from Scan at V_{IH} and ENABLE at V_{IL}; Delay to Valid Data Levels for C_{OL} = 10pF and one TTL Load or Valid Data Currents for High Capacitance Loads
Output Delay Time CASCADE ENABLE	t_{DCE}	-	10	ns	Negative Transition from Scan at V_{IL} and ST5 of Scan Counter or Positive Transition From SCAN RESET/LOAD at V_{IL} to Valid Data Levels for C_{OL} = 12pF and one TTL Load

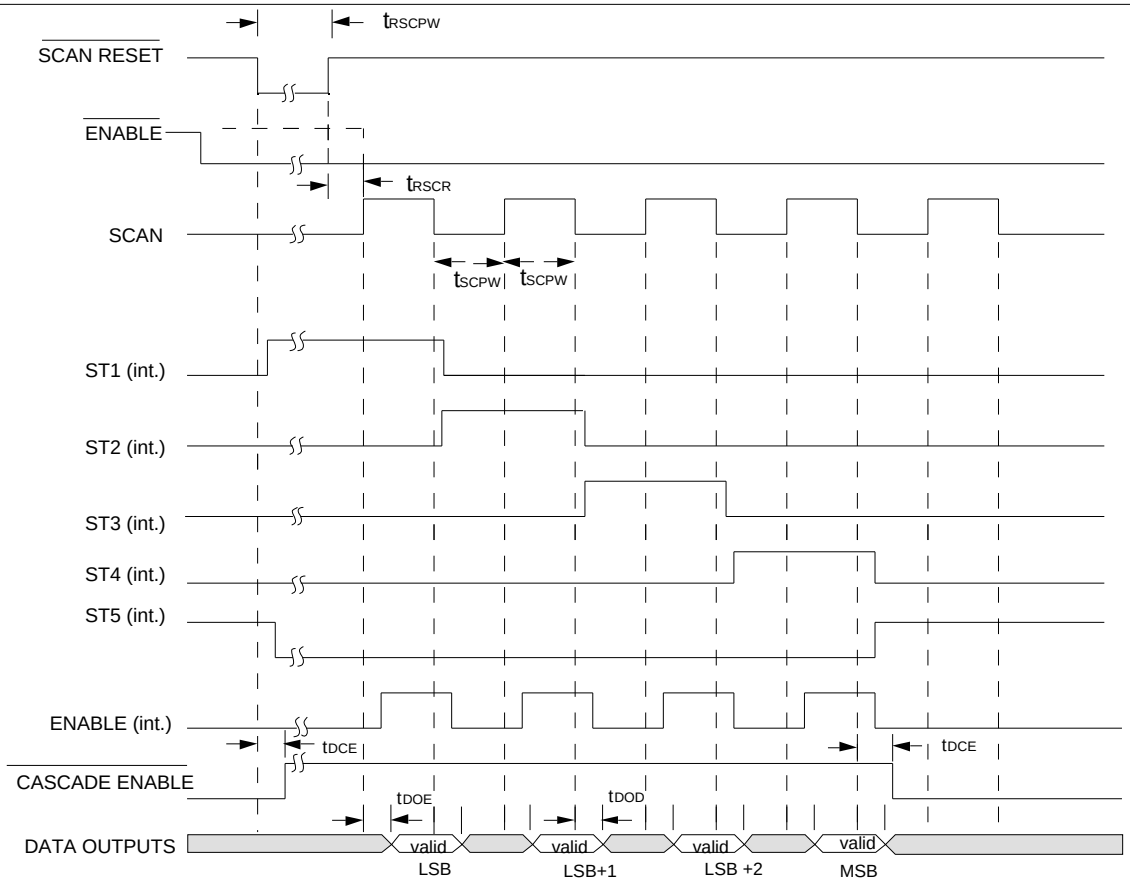


FIGURE 3A. SCAN COUNTER & DECODER OUTPUTS TIMING DIAGRAM FOR LS7060C

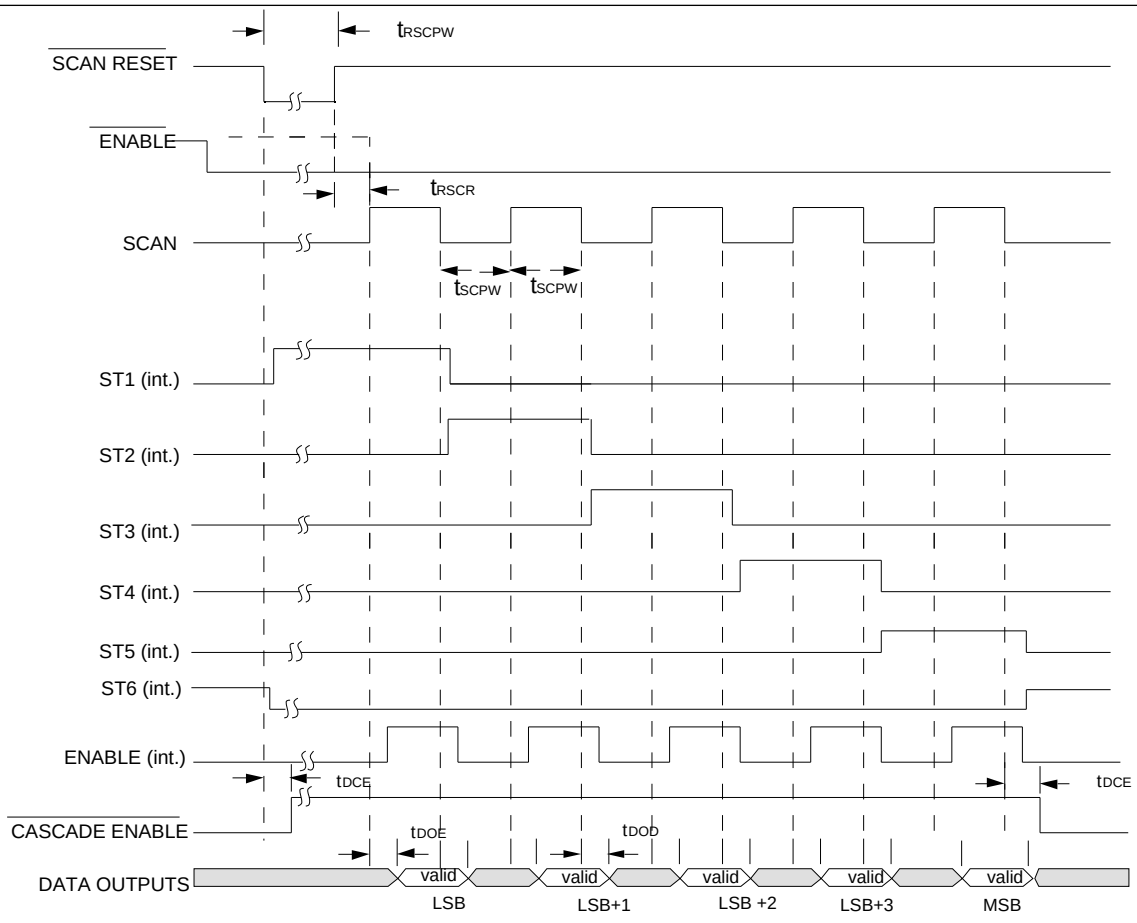


FIGURE 3B. SCAN COUNTER & DECODER OUTPUTS TIMING DIAGRAM FOR LS7061C.

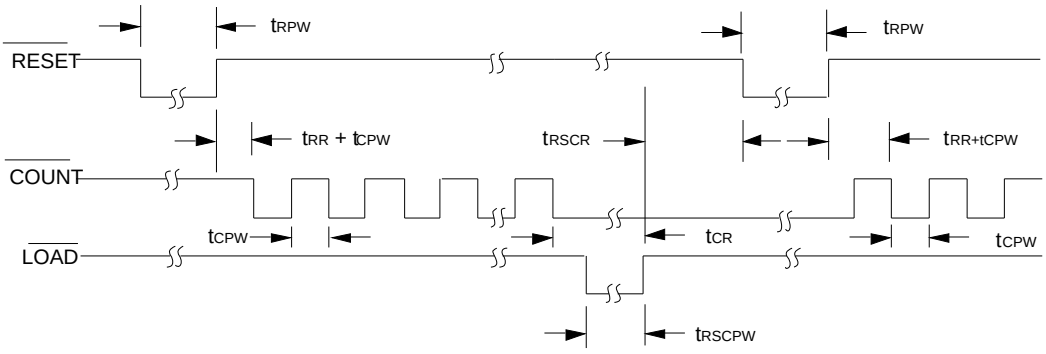


FIGURE 4. COUNTER TIMING DIAGRAM

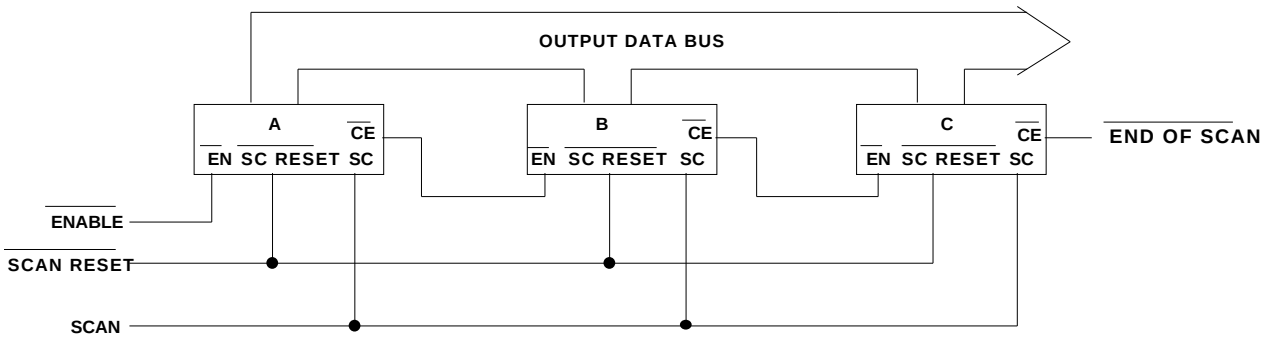


FIGURE 5. ILLUSTRATION OF A 3 DEVICE CASCADE

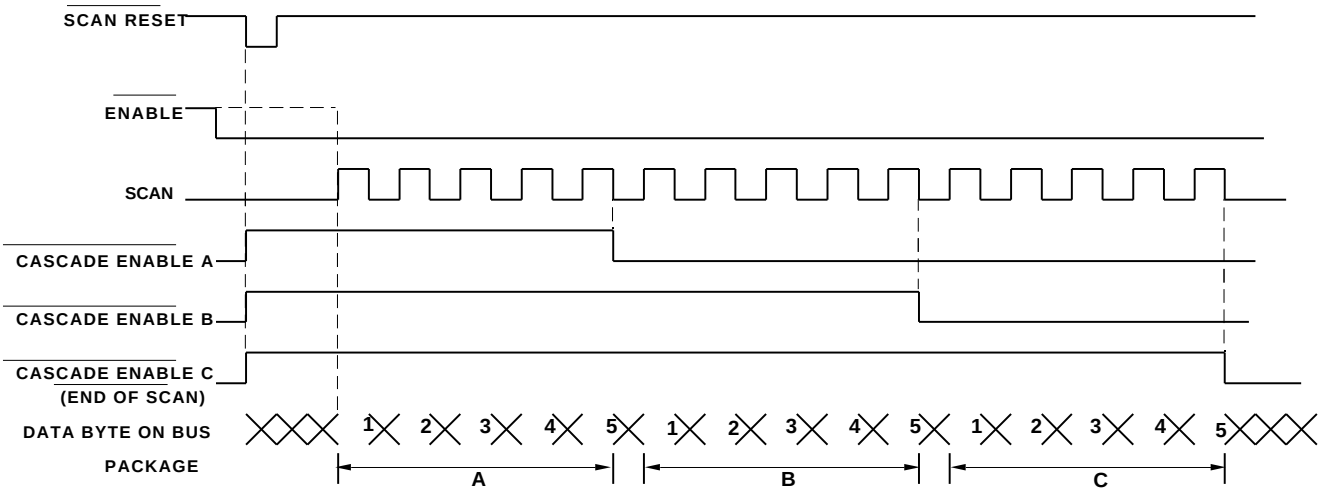


FIGURE 6. TIMING DIAGRAM FOR THE 3 DEVICE CASCADE

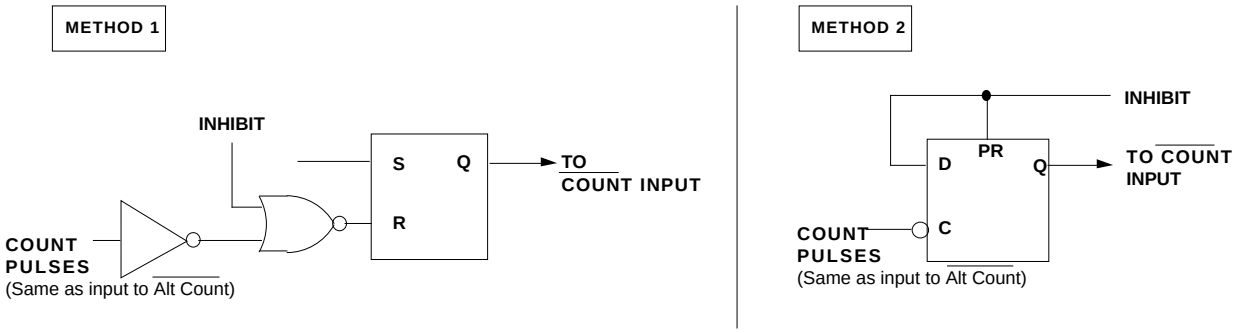
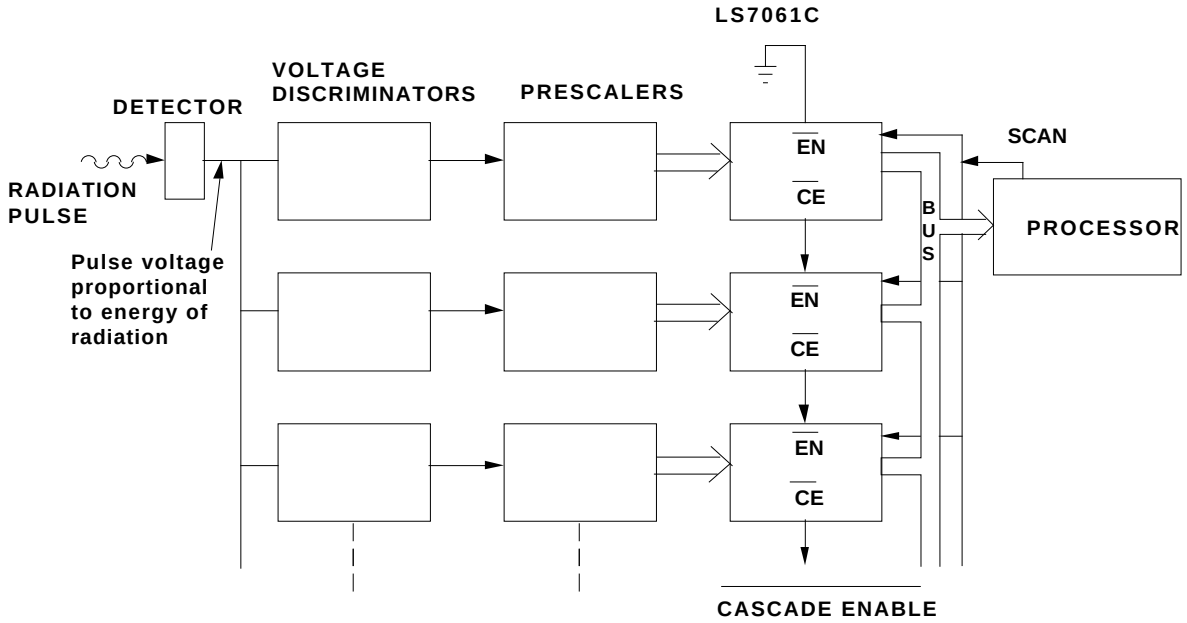


FIGURE 7. SYNCHRONIZING INHIBIT WITH COUNT PULSES

FIGURE 8. APPLICATION EXAMPLE: HIGH SPEED DIFFERENTIAL ENERGY ANALYZER



NOTE : The processor subtracts counts from successive counters to determine the differential energy spectrum

FIGURE 9A. LS7060C BLOCK DIAGRAM

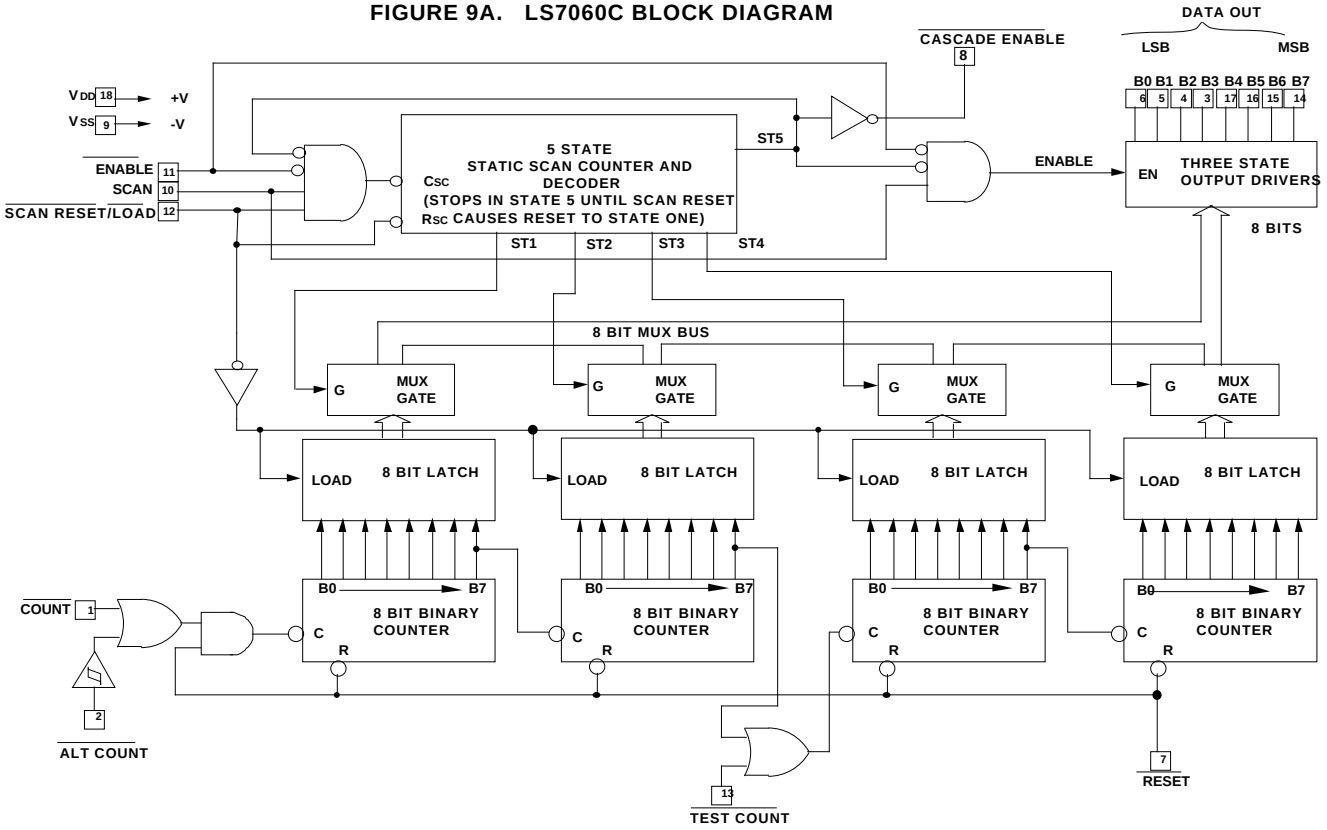


FIGURE 9B. LS7061C BLOCK DIAGRAM