

# Am79R70\*/Le79R70

## Ringing Subscriber Line Interface Circuit

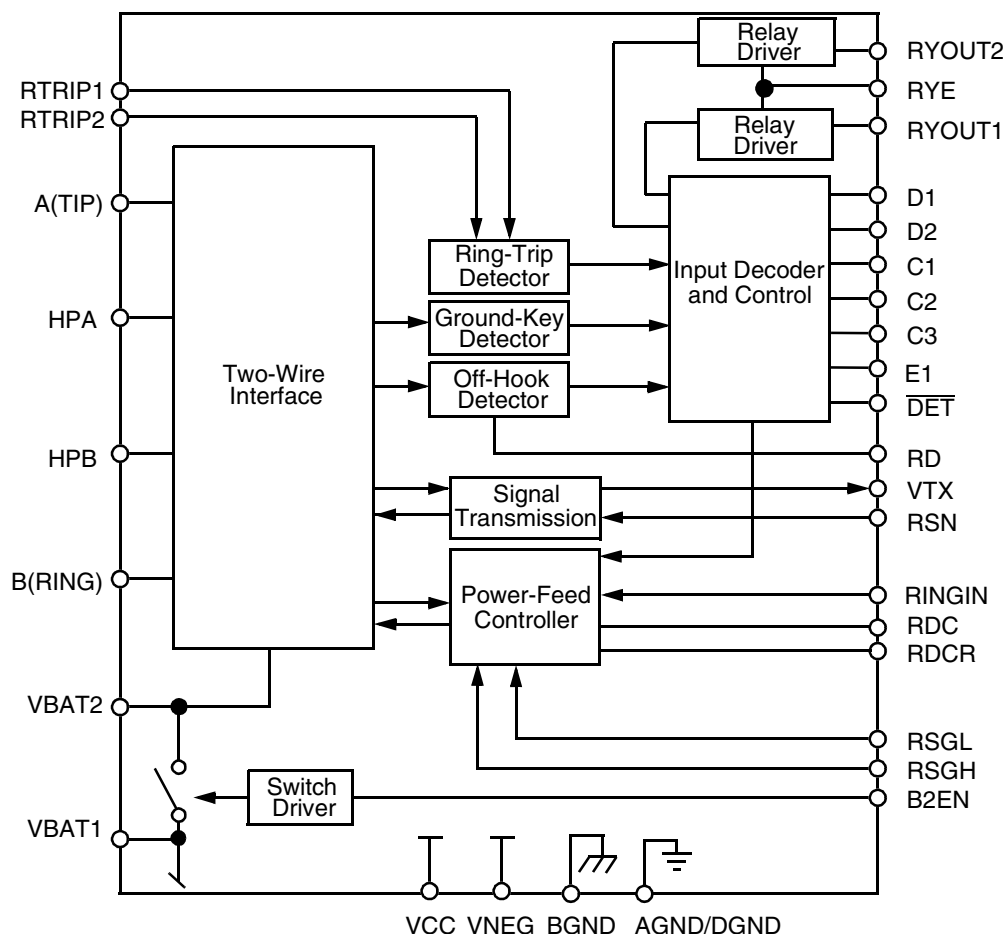


### DISTINCTIVE CHARACTERISTICS

- Ideal for ISDN-TA and set top applications
- On-chip ringing with on-chip ring-trip detector
- Low standby state power
- Battery operation:
  - $V_{BAT1}$ : -40 V to -67 V
  - $V_{BAT2}$ : -19 V to  $V_{BAT1}$
- On-chip battery switching and feed selection
- On-hook transmission
- Polarity reversal option
- Programmable constant-current feed

- Programmable Open Circuit voltage
- Programmable loop-detect threshold
- Current gain = 1000
- Two-wire impedance set by single component
- Ground-key detector
- Tip Open state for ground-start lines
- Internal  $V_{EE}$  regulator (no external -5 V power supply required)
- Two on-chip relay drivers and snubber circuits
- Space Saving Package Options (8x8 QFN)

### BLOCK DIAGRAM



*\*This product can be ordered using ordering part numbers Am79R70 or Le79R70. The Am79R70 ordering part number will be discontinued after 6/30/02, at which time the product will only be available using the Le79R70 ordering part number.*

## GENERAL DESCRIPTION

The Legerity family of subscriber line interface circuit (SLIC) products provide the telephone interface functions required throughout the worldwide market. Legerity SLIC devices address all major telephony markets including central office (CO), private branch exchange (PBX), digital loop carrier (DLC), fiber-in-the-loop (FITL), radio-in-the-loop (RITL), hybrid fiber coax (HFC), and video telephony applications.

The Legerity SLIC devices offer support of BORSHT (battery feed, over voltage protection, ringing, supervision, hybrid, and test) functions with features including current limiting, on-hook transmission, polarity reversal, tip-open, and loop-current detection. These features allow reduction of linecard cost by minimizing component count, conserving board space, and supporting automated manufacturing.

The Legerity SLIC devices provide the two- to four-wire hybrid function, DC loop feed, and two-wire supervision. Two-wire termination is programmed by a scaled impedance network. Transhybrid balance can be achieved with an external balance circuit or simply programmed using a companion Legerity codec device, the Am79C02/03/031 DSLAC™ device, the Am79Q02/021/031 Programmable Quad SLAC (QSLAC™) device, or the Am79Q5457/4457 Non-programmable QSLAC device.

The Le79R70 Ringing SLIC device is a bipolar monolithic SLIC that offers on-chip ringing. Now designers can achieve significant cost reductions at the system level for short-loop applications by integrating the ringing function on chip. Examples of such applications would be ISDN Terminal Adaptors and set top boxes. Using a CMOS-compatible input waveform and wave shaping R-C network, the Le79R70 Ringing SLIC can provide trapezoidal wave ringing to meet various design requirements.

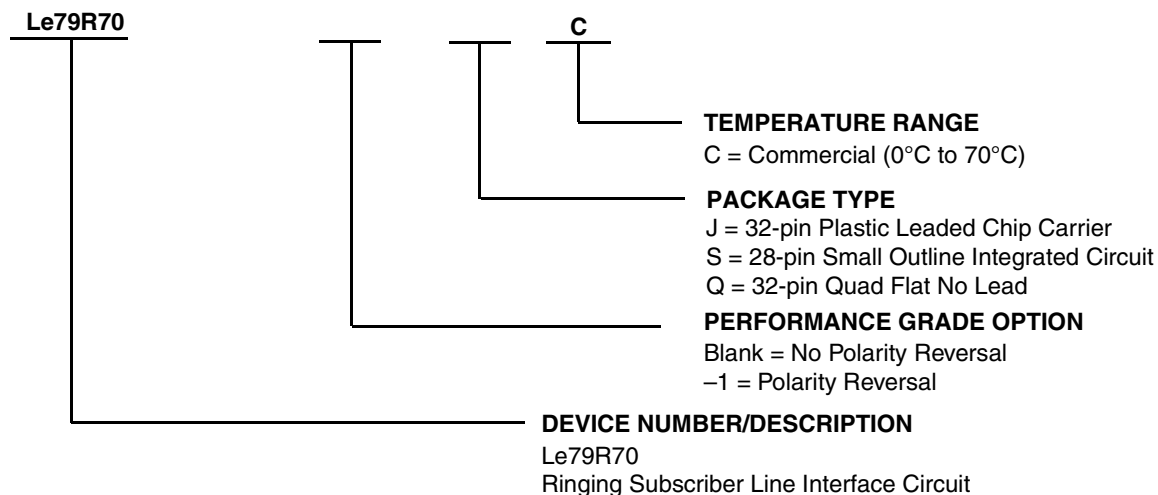
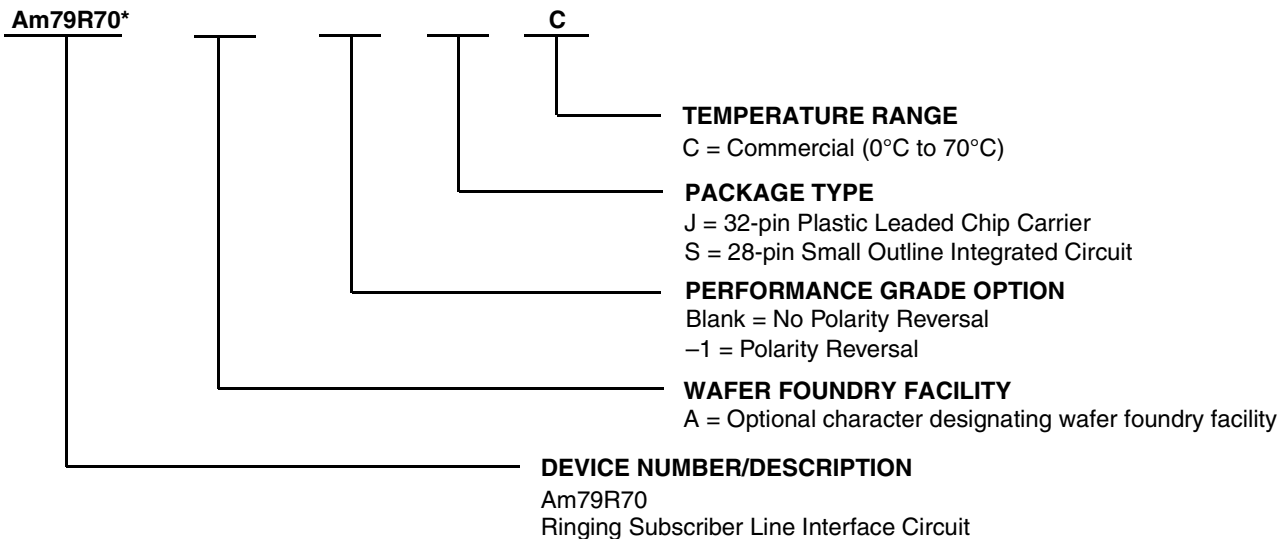
In order to further enhance the suitability of this device in short-loop, distributed switching applications, Legerity has maximized power savings by incorporating battery switching on chip. The Le79R70 Ringing SLIC device switches between two battery supplies such that in the Off-hook (active) state, a low battery is used to save power. In order to meet the Open Circuit voltage requirements of fax machines and maintenance termination units (MTU), the SLIC automatically switches to a higher voltage in the On-hook (standby) state.

Like all of the Legerity SLIC devices, the Le79R70 Ringing SLIC device supports on-hook transmission, ring-trip detection and programmable loop-detect threshold. The Le79R70 Ringing SLIC device is a programmable constant-current feed device with two on-chip relay drivers to operate external relays. This unique device is available in the proven Legerity 75 V bipolar process.

## ORDERING INFORMATION

### Standard Products

Legerity standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below



Valid Combinations		
Am79R70 Am79R70A	-1	JC SC

Valid Combinations		
Le79R70	-1	JC SC QC**

#### Valid Combinations

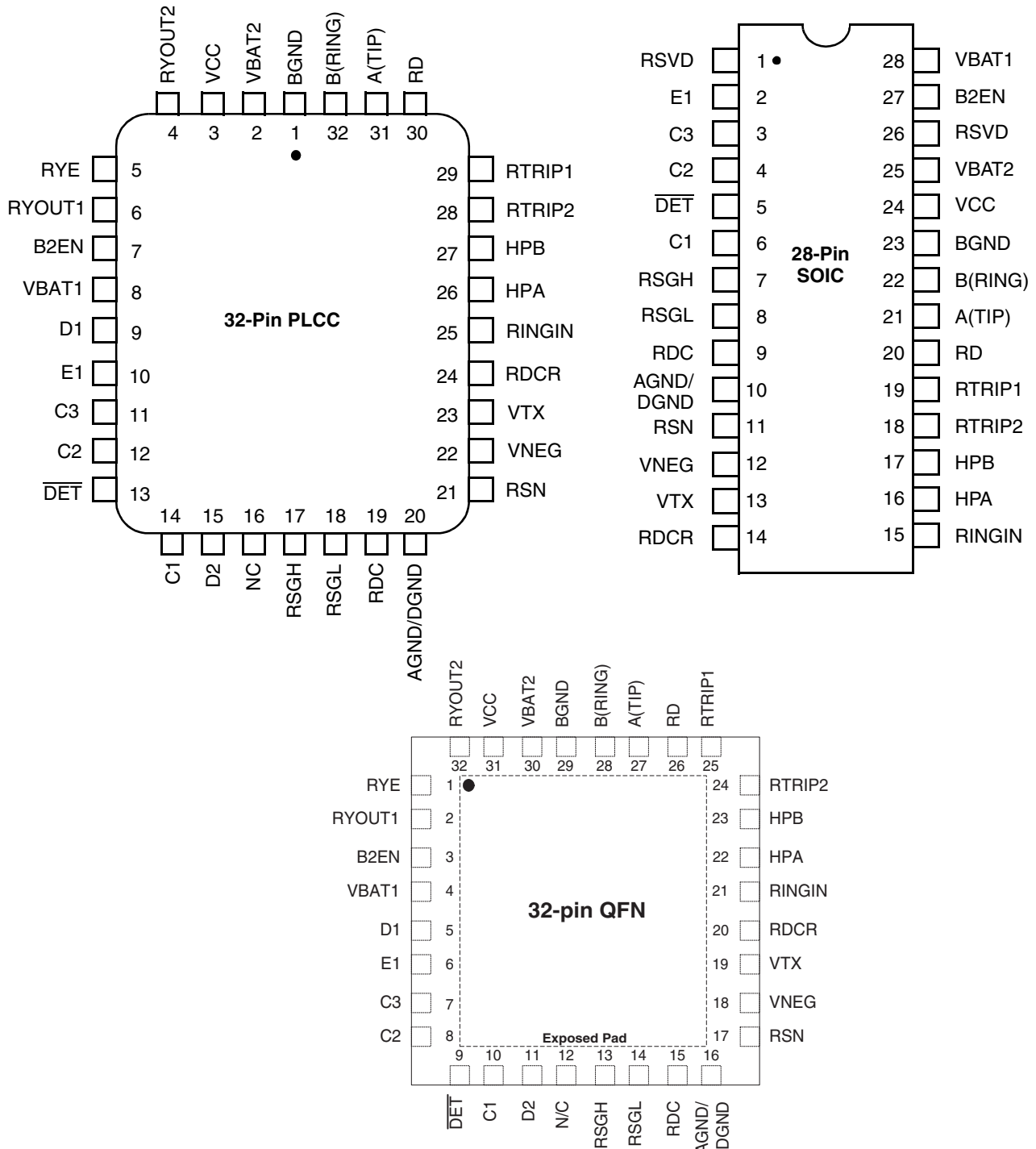
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Legerity sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on Legerity's standard military-grade products.

\*This product can be ordered using ordering part numbers Am79R70 or Le79R70. The Am79R70 ordering part number will be discontinued after 6/30/02, at which time the product will only be available using the Le79R70 ordering part number.

\*\*Due to size constraints, QFN devices are marked by omitting the "Le" prefix and the performance grade dash character. For example, Le79R70-1QC is marked 79R701QC.

## CONNECTION DIAGRAMS

### Top View



#### Notes:

1. Pin 1 is marked for orientation.
2. NC = No connect
3. RSVD = Reserved. Do not connect to this pin.
4. The thermally enhanced QFN package features an exposed pad on the underside which must be electrically tied to VBAT1.

## PIN DESCRIPTIONS

Pin Names	Type	Description
AGND/DGND	Gnd	Analog and digital ground are connected internally to a single pin.
A(TIP)	Output	Output of A(TIP) power amplifier.
B2EN	Input	V <sub>BAT2</sub> enable. Logic Low enables operation from V <sub>BAT2</sub> . Logic High enables operation from V <sub>BAT1</sub> . TTL compatible.
BGND	Gnd	Battery (power) ground
B(RING)	Output	Output of B(RING) power amplifier.
C3–C1	Input	Decoder. TTL compatible. C3 is MSB and C1 is LSB.
D1	Input	Relay1 control. TTL compatible. Logic Low activates the Relay1 relay driver.
D2	Input	(Option) Relay2 control. TTL compatible. Logic Low activates the Relay2 relay driver.
DET	Output	Detector. Logic Low indicates that the selected detector is tripped. Logic inputs C3–C1 and E1 select the detector. Open-collector with a built-in 15 kΩ pull-up resistor.
E1	Input	(Option) A logic High selects the off-hook detector. A logic Low selects the ground-key detector. TTL compatible.
HPA	Capacitor	High-pass filter capacitor. A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-pass filter capacitor. B(RING) side of high-pass filter capacitor.
RD	Resistor	Detect resistor. Threshold modification and filter point for the off-hook detector.
RDC	Resistor	DC feed resistor. Connection point for the DC-feed current programming network, which also connects to the receiver summing node (RSN). V <sub>RDC</sub> is negative for normal polarity and positive for reverse polarity.
RDCR	—	Connection point for feedback during ringing.
RINGIN	Input	Ring Signal Input. Pin for ring signal input. Square-wave shaped by external RC filter. Requires 50% duty cycle. CMOS-compatible input.
RSGH	Input	Saturation Guard High. Pin for resistor to adjust Open Circuit voltage when operating from V <sub>BAT1</sub> .
RSGL	Input	Saturation Guard Low. Pin for resistor to adjust the anti-saturation cut-in voltage when operating from both V <sub>BAT1</sub> and V <sub>BAT2</sub> .
RSN	Input	The metallic current (AC and DC) between A(TIP) and B(RING) is equal to 1000 x the current into this pin. The networks that program receive gain, two-wire impedance, and feed resistance all connect to this node.
RTRIP1	Input	Ring-trip detector. Ring-trip detector threshold set and filter pin.
RTRIP2	Input	Ring-trip detector threshold offset (switch to V <sub>BAT1</sub> ). For power conservation in any non-ringing state, this switch is open.
RYE	Output	Common Emitter of RYOUT1/RYOUT2. Emitter output of RYOUT1 and RYOUT2. Normally connected to relay ground.
RYOUT1	Output	Relay/switch driver. Open-collector driver with emitter internally connected to RYE.
RYOUT2	Output	(Option) Relay/switch driver. Open-collector driver with emitter internally connected to RYE.
VBAT1	Battery	Battery supply and connection to substrate.
VBAT2	Battery	Power supply to output amplifiers. Connect to off-hook battery through a diode.
VCC	Power	Positive analog power supply.
VNEG	Power	Negative analog power supply. This pin is the return for the internal VEE regulator.
VTX	Output	Transmit Audio. This output is a 0.5066 gain version of the A(TIP) and B(RING) metallic AC voltage. VTX also sources the two-wire input impedance programming network.
Exposed Pad	Battery	This must be electrically tied to VBAT1.

## ABSOLUTE MAXIMUM RATINGS

Storage temperature .....	–55°C to +150°C
V <sub>CC</sub> with respect to AGND/DGND .....	0.4 V to +7 V
V <sub>NEG</sub> with respect to AGND/DGND .....	0.4 V to V <sub>BAT2</sub>
V <sub>BAT2</sub> .....	V <sub>BAT1</sub> to GND
V <sub>BAT1</sub> with respect to AGND/DGND:	
Continuous .....	+0.4 V to –80 V
10 ms .....	+0.4 V to –85 V
BGND with respect to AGND/DGND.....	+3 V to –3 V
A(TIP) or B(RING) to BGND:	
Continuous .....	V <sub>BAT1</sub> –5 V to +1 V
10 ms (f = 0.1 Hz) .....	V <sub>BAT1</sub> –10 V to +5 V
1 μs (f = 0.1 Hz) .....	V <sub>BAT1</sub> –15 V to +8 V
250 ns (f = 0.1 Hz) .....	V <sub>BAT1</sub> –20 V to +12 V
Current from A(TIP) or B(RING).....	±150 mA
RYOUT1, RYOUT2 current.....	75 mA
RYOUT1, RYOUT2 voltage .....	RYE to +7 V
RYOUT1, RYOUT2 transient .....	RYE to +10 V
RYE voltage .....	BGND to V <sub>BAT1</sub>
C3–C1, D2–D1, E1, B2EN, and RINGIN	
Input voltage .....	–0.4 V to V <sub>CC</sub> + 0.4 V
Maximum continuous power dissipation*	
T <sub>A</sub> = 70°C	
In 28-pin SOIC package .....	1.25 W
In 32-pin PLCC package.....	1.67 W
In 32-pin QFN package.....	3.00 W
Thermal Data:.....	θ <sub>JA</sub>
In 28-pin SOIC package .....	60°C/W typ
In 32-pin PLCC package.....	45°C/W typ
In 32-pin QFN package** .....	25°C/W typ

\* Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. Continuous operation above 145°C junction temperature may degrade device reliability.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

\*\* The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to a large internal copper plane.

## OPERATING RANGES

### Commercial (C) Devices

Ambient temperature .....	0°C to +70°C*
V <sub>CC</sub> .....	4.75 V to 5.25 V
V <sub>NEG</sub> .....	–4.75 V to V <sub>BAT2</sub>
V <sub>BAT1</sub> .....	–40 V to –67 V
V <sub>BAT2</sub> .....	–19 V to V <sub>BAT1</sub>
AGND/DGND.....	0 V
BGND with respect to	
AGND/DGND .....	–100 mV to +100 mV
Load resistance on VTX to ground.....	20 kΩ min

The Operating Ranges define those limits between which the functionality of the device is guaranteed.

\* Legerity guarantees the performance of this device over the commercial (0°C to 70°C) temperature range by conducting electrical characterization and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore TR-TSY-000357 Component Reliability Assurance Requirements for Telecommunications Equipment.

## ELECTRICAL CHARACTERISTICS

Description		Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Transmission Performance							
2-wire return loss		200 Hz to 3.4 kHz (Test Circuit D)	26			dB	1, 4, 6
Z <sub>VTX</sub> , analog output impedance				3	20	Ω	4
V <sub>VTX</sub> , analog output offset voltage			−50		+50	mV	
Z <sub>RSN</sub> , analog input impedance				1	20	Ω	4
Overload level, 2-wire and 4-wire, off hook		Active state	2.5			V <sub>pk</sub>	2a
Overload level, 2-wire		On hook, R <sub>LAC</sub> = 600 Ω	0.88			V <sub>rms</sub>	2b
THD (Total Harmonic Distortion)		+3 dBm, BAT2 = −24 V		−64	−50	dB	5
THD, on hook, OHT state		0 dBm, R <sub>LAC</sub> = 600 Ω, BAT1 = −67 V			−40		
Longitudinal Performance (See Test Circuit C)							
Longitudinal to metallic L-T, L-4 balance		200 Hz to 3.4 kHz	40			dB	
Longitudinal signal generation 4-L		200 Hz to 800 Hz, Normal polarity	40				
Longitudinal current per pin (A or B)		Active or OHT state	12	28		mArms	4
Longitudinal impedance at A or B		0 to 100 Hz, T <sub>A</sub> = +25°C		25		Ω/pin	
Idle Channel Noise							
C-message weighted noise				+7	+14	dBrnC	
Psophometric weighted noise				−83	−76	dBmp	4
Insertion Loss and Four- to Four-Wire Balance Return Signal (See Test Circuits A and B)							
Gain accuracy	4- to 2-wire	0 dBm, 1 kHz	−0.20	0	+0.20	dB	3
Gain accuracy	2- to 4-wire and 4- to 4-wire	0 dBm, 1 kHz	−6.22	−6.02	−5.82		
Gain accuracy	4- to 2-wire	OHT state, on hook	−0.35	0	+0.35		
Gain accuracy	2- to 4-wire and 4- to 4-wire	OHT state, on hook	−6.37	−6.02	−5.77		
Gain accuracy over frequency		300 to 3400 Hz relative to 1 kHz	−0.10		+0.10		
Gain tracking		+3 dBm to −55 dBm relative to 0 dBm	−0.10		+0.10		3, 4
Gain tracking OHT state, on hook		0 dBm to −37 dBm +3 dBm to 0 dBm	−0.10 −0.35		+0.10 +0.35		3, 4 3
Group delay		0 dBm, 1 kHz		3		μs	1, 4, 6

## ELECTRICAL CHARACTERISTICS (CONTINUED)

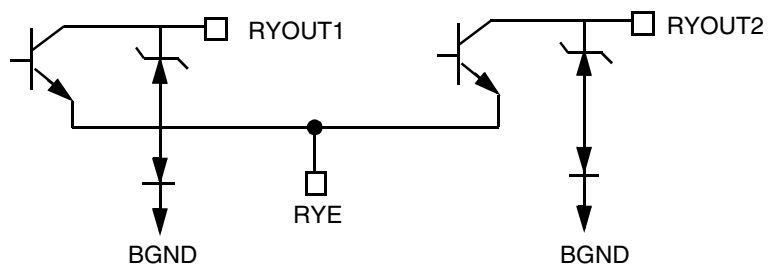
Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Line Characteristics						
I <sub>L</sub> , Loop-current accuracy	I <sub>L</sub> in constant-current region, B2EN = 0	0.9I <sub>L</sub>	I <sub>L</sub>	1.1I <sub>L</sub>	mA	
I <sub>L</sub> , Long loops, Active state	R <sub>LDC</sub> = 600 Ω, RSGL = open R <sub>LDC</sub> = 750 Ω, RSGL = short	20 20	21.7			
I <sub>L</sub> , Accuracy, Standby state	$I_L = \frac{ V_{BAT1}  - 10\text{ V}}{R_L + 400}$	0.8I <sub>L</sub>	I <sub>L</sub>	1.2I <sub>L</sub>		
	I <sub>L</sub> = constant-current region T <sub>A</sub> = 25°C	18	27	39		
I <sub>L</sub> LIM	Active, A and B to ground OHT, A and B to ground		55 55	110		
I <sub>L</sub> , Loop current, Open Circuit state	R <sub>L</sub> = 0			100	μA	
I <sub>A</sub> , Pin A leakage, Tip Open state	R <sub>L</sub> = 0			100		
I <sub>B</sub> , Pin B current, Tip Open state	B to ground		34		mA	
V <sub>A</sub> , Standby, ground-start signaling	A to –48 V = 7 kΩ, B to ground = 100 Ω	–7.5	–5			V
V <sub>AB</sub> , Open Circuit voltage		42				
Power Supply Rejection Ratio (V <sub>RI</sub> PPLE = 100 mVrms), Active Normal State						
V <sub>CC</sub>	50 Hz to 3400 Hz	33	50		dB	5
V <sub>NEG</sub>	50 Hz to 3400 Hz	30	40			
V <sub>BAT1</sub>	50 Hz to 3400 Hz	30	50			
V <sub>BAT2</sub>	50 Hz to 3400 Hz	30	50			
Power Dissipation						
On hook, Open Circuit state	V <sub>BAT1</sub>		48	100	mW	
On hook, Standby state	V <sub>BAT2</sub>		55	80		9
On hook, OHT state	V <sub>BAT1</sub>		200	300		
On hook, Active state	V <sub>BAT1</sub>		220	350		
Off hook, Standby state	V <sub>BAT1</sub> or V <sub>BAT2</sub> R <sub>L</sub> = 300 Ω		2000	2800		9
Off hook, OHT state	V <sub>BAT1</sub> R <sub>L</sub> = 300 Ω		2000	2200		
Off hook, Active state	V <sub>BAT2</sub> R <sub>L</sub> = 300 Ω		550	750		
Supply Currents						
I <sub>CC</sub> , On-hook V <sub>CC</sub> supply current	Open Circuit state		3.0	4.5	mA	
	Standby state		3.2	5.5		
	OHT state		6.2	8.0		
	Active state–normal		6.5	9.0		
I <sub>NEG</sub> , On-hook V <sub>NEG</sub> supply current	Open Circuit state		0.1	0.2		
	Standby state		0.1	0.2		
	OHT state		0.7	1.1		
	Active state–normal		0.7	1.1		
I <sub>BAT</sub> , On-hook V <sub>BAT</sub> supply current	Open Circuit state		0.45	1.0		
	Standby state		0.6	1.5		
	OHT state		2.0	4.0		
	Active state–normal		2.7	5.0		



## ELECTRICAL CHARACTERISTICS (continued)

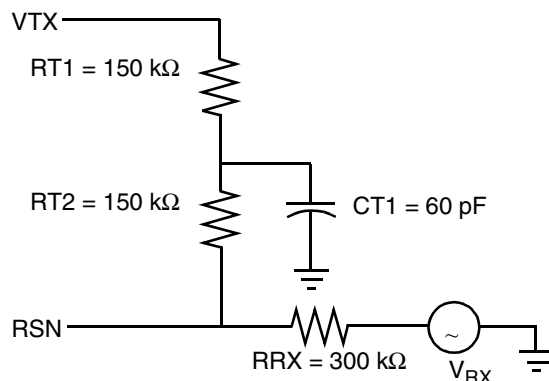
Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Logic Inputs (C3–C1, D2–D1, E1, and B2EN)						
V <sub>IH</sub> , Input High voltage		2.0			V	
V <sub>IL</sub> , Input Low voltage				0.8		
I <sub>IH</sub> , Input High current		–75		40	μA	
I <sub>IL</sub> , Input Low current		–400				
Logic Output $\overline{DET}$						
V <sub>OL</sub> , Output Low voltage	I <sub>OUT</sub> = 0.8 mA, 15 kΩ to V <sub>CC</sub>			0.40	V	
V <sub>OH</sub> , Output High voltage	I <sub>OUT</sub> = –0.1 mA, 15 kΩ to V <sub>CC</sub>	2.4				
Ring-Trip Detector Input						
Ring detect accuracy	$IRTD = \left( \frac{ BAT1  - 1}{RRT1} + 24 \mu A \right) \bullet 335$	–10		+10	%	
Ring Signal						
V <sub>AB</sub> , Ringing	Bat1 = –67 V, ringload = 1570 Ω	57	61		V <sub>pk</sub>	
V <sub>AB</sub> Ringing offset	V <sub>RINGIN</sub> = 2.5 V		0		V	
ΔV <sub>AB</sub> /ΔV <sub>RINGIN</sub> (RINGIN gain)			180		—	
Ground-Key Detector Thresholds						
Ground-key resistive threshold	B to ground	2	5	10	kΩ	
Ground-key current threshold	B to ground		11		mA	
Loop Detector						
R <sub>LTH</sub> , Loop-resistance detect threshold	Active, V <sub>BAT1</sub> Active, V <sub>BAT2</sub> Standby	–20 –20 –12		20 20 12	%	8
Relay Driver Output (RELAY1 and 2)						
V <sub>OL</sub> , On voltage (each output)	I <sub>OL</sub> = 30 mA		+0.25	+0.4	V	4
V <sub>OL</sub> , On voltage (each output)	I <sub>OL</sub> = 40 mA		+0.30	+0.8		
I <sub>OH</sub> , Off leakage (each output)	V <sub>OH</sub> = +5 V			100	μA	
Zener breakover (each output)	I <sub>Z</sub> = 100 μA	6.6	7.9		V	
Zener on voltage (each output)	I <sub>Z</sub> = 30 mA		11			

## RELAY DRIVER SCHEMATIC



**Notes:**

- Unless otherwise noted, test conditions are  $BAT1 = -67\text{ V}$ ,  $BAT2 = -24\text{ V}$ ,  $V_{CC} = +5\text{ V}$ ,  $V_{NEG} = -5\text{ V}$ ,  $R_L = 600\ \Omega$ ,  $R_{DC1} = 80\text{ k}\Omega$ ,  $R_{DC2} = 20\text{ k}\Omega$ ,  $R_D = 75\text{ k}\Omega$ , no fuse resistors,  $C_{HP} = 0.018\ \mu\text{F}$ ,  $C_{DC} = 1.2\ \mu\text{F}$ ,  $D_1 = D_2 = 1\text{N400x}$ , two-wire AC input impedance (ZSL) is a  $600\ \Omega$  resistance synthesized by the programming network shown below.  $R_{SGL} = \text{open}$ ,  $R_{SGH} = \text{open}$ ,  $R_{DCR} = 2\text{ k}\Omega$ ,  $R_{RT1} = 430\text{ k}\Omega$ ,  $R_{RT2} = 12\text{ k}\Omega$ ,  $C_{RT} = 1.5\ \mu\text{F}$ ,  $R_{SLEW} = 150\text{ k}\Omega$ ,  $C_{SLEW} = 0.33\ \mu\text{F}$ .



- Overload level is defined when  $THD = 1\%$ .
  - Overload level is defined when  $THD = 1.5\%$ .
- Balance return signal is the signal generated at  $V_{TX}$  by  $V_{RX}$ . This specification assumes that the two-wire AC load impedance matches the programmed impedance.
  - Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.
  - This parameter is tested at  $1\text{ kHz}$  in production. Performance at other frequencies is guaranteed by characterization.
  - Group delay can be greatly reduced by using a  $Z_T$  network such as that shown in Note 1 above. The network reduces the group delay to less than  $2\ \mu\text{s}$  and increases  $2\text{WRL}$ . The effect of group delay on linecard performance may also be compensated for by synthesizing complex impedance with the QSLAC or DSLAC device.
  - Open Circuit  $V_{AB}$  can be modified using  $R_{SGH}$ .
  - $R_D$  must be greater than  $56\text{ k}\Omega$ . Refer to Table 2 for typical value of  $R_{LTH}$ .
  - Lower power is achieved by switching into low-battery state in standby. Standby loop current is returned to  $V_{BAT1}$  regardless of the battery selected.

**Table 1. SLIC Decoding**

State	C3 C2 C1	2-Wire Status	(DET) Output		Battery Selection
			E1 = 1	E1 = 0	
0	0 0 0	Open Circuit	Ring trip	Ring trip	B2EN
1	0 0 1	Ringin	Ring trip	Ring trip	
2	0 1 0	Active	Loop detector	Ground key	
3	0 1 1	On-hook TX (OHT)	Loop detector	Ground key	
4	1 0 0	Tip Open	Loop detector	Ground key	B2EN = 1**
5	1 0 1	Standby	Loop detector	Ground key	$V_{BAT1}$
6*	1 1 0	Active Polarity Reversal	Loop detector	Ground key	B2EN
7*	1 1 1	OHT Polarity Reversal	Loop detector	Ground key	

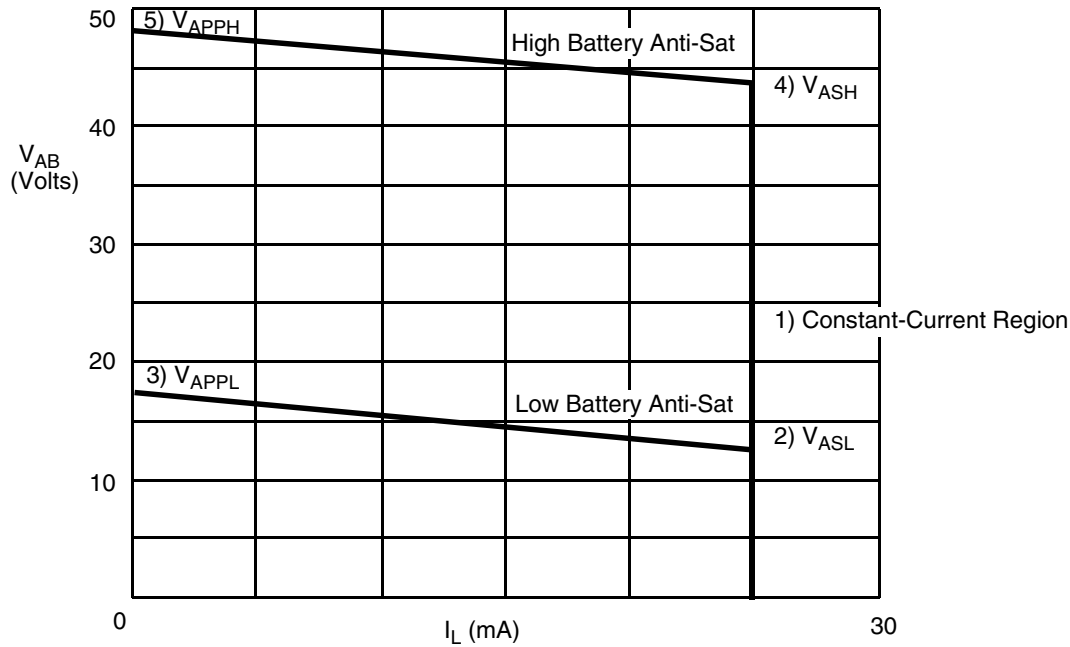
**Notes:**

- \* Only  $-1$  performance grade devices support polarity reversal.
- \*\* For correct ground-start operation using Tip Open,  $V_{BAT1}$  on-hook battery must be used.

**Table 2. User-Programmable Components**

$Z_T = 500(Z_{2WIN} - 2R_F)$	$Z_T$ is connected between the VTX and RSN pins. The fuse resistors are $R_F$ , and $Z_{2WIN}$ is the desired 2-wire AC input impedance. When computing $Z_T$ , the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{1000 \bullet Z_T}{Z_T + 500(Z_L + 2R_F)}$	$Z_{RX}$ is connected from $V_{RX}$ to $R_{SN}$ . $Z_T$ is defined above, and $G_{42L}$ is the desired receive gain.
$R_{DC1} + R_{DC2} = \frac{2500}{I_{LOOP}}$ $R_{DCR1} + R_{DCR2} = \frac{3000}{I_{ringlim}}$ $C_{DC} = 19 \text{ ms} \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1}R_{DC2}}$ $C_{DCR} = \frac{R_{DCR1} + R_{DCR2}}{R_{DCR1}R_{DCR2}} \bullet 150 \text{ } \mu\text{s}$	<p><math>R_{DC1}</math>, <math>R_{DC2}</math>, and <math>C_{DC}</math> form the network connected to the RDC pin. <math>I_{LOOP}</math> is the desired loop current in the constant-current region.</p> <p><math>R_{DCR1}</math>, <math>R_{DCR2}</math>, and <math>C_{DCR}</math> form the network connected to the RDCR pin. See Applications Circuit for these components.</p> <p><math>C_{DCR}</math> sets the ringing time constant, which can be between 15 <math>\mu\text{s}</math> and 150 <math>\mu\text{s}</math>.</p>
$R_D = R_{LTH} \bullet 12.67 \text{ for high battery state}$	$R_D$ is the resistor connected from the RD pin to GND and $R_{LTH}$ is the loop-resistance threshold between on-hook and off-hook detection. $R_D$ should be greater than 56 k $\Omega$ to guarantee detection will occur in the Standby state. Choose the value of $R_D$ for high battery state; then use the equation for $R_{LTH}$ to find where the threshold is for low battery.
<b>Loop-Threshold Detect Equations</b>	
$R_{LTH} = \frac{R_D}{12.67} \text{ for high battery}$	This is the same equation as for $R_D$ in the preceding equation, except solved for $R_{LTH}$ .
$R_{LTH} = \frac{R_D}{11.37} \text{ for low battery}$	For low battery, the detect threshold is slightly higher, which will avoid oscillating between states.
$R_{LTH} = \frac{ V_{BAT1}  - 10}{915} \bullet R_D - 400 - 2R_F$	$R_{LTH} \text{ standby} < R_{LTH} \text{ active } V_{BAT1} < R_{LTH} \text{ active } V_{BAT2}$ , which will guarantee no unstable states under all operating conditions. This equation will show at what resistance the standby threshold will be; it is actually a current threshold rather than a resistance threshold, which is shown by the Vbat dependency.

## DC FEED CHARACTERISTICS



**Figure 1. Typical  $V_{AB}$  vs.  $I_L$  DC Feed Characteristics**

$$R_{DC} = R_{DC1} + R_{DC2} = 20 \text{ k}\Omega + 80 \text{ k}\Omega = 100 \text{ k}\Omega$$

$$(V_{BAT1} = -67 \text{ V}, V_{BAT2} = -24 \text{ V})$$

**Notes:**

1. Constant-current region:  $V_{AB} = I_L R_L = \frac{2500}{R_{DC}} R_L$ ; where  $R_L = R_L + 2R_F$

2. Low battery  $V_{ASL} = \frac{1000 \cdot (104 \cdot 10^3 + R_{SGL})}{6720 \cdot 10^3 + (80 \cdot R_{SGL})}$ ; where  $R_{SGL}$  = resistor to GND, B2EN = logic Low.

Anti-sat region:  $V_{ASL} = \frac{1000 \cdot (R_{SGL} - 56 \cdot 10^3)}{6720 \cdot 10^3 + (80 \cdot R_{SGL})}$ ; where  $R_{SGL}$  = resistor to  $V_{CC}$ , B2EN = logic Low.

$R_{SGL}$  to  $V_{CC}$  must be greater than 100 k $\Omega$ .

3.  $V_{APPL} = 4.17 + V_{ASL}$

$$I_{LOOP} = \frac{V_{APPL}}{\frac{(R_{DC1} + R_{DC2})}{600} + 2R_F + R_{LOOP}}$$

4. High battery  $V_{ASH} = V_{ASHH} + V_{ASL}$

Anti-sat region:  $V_{ASHH} = \frac{1000 \cdot (70 \cdot 10^3 + R_{SGH})}{1934 \cdot 10^3 + (31.75 \cdot R_{SGH})}$ ; where  $R_{SGH}$  = resistor to GND, B2EN = logic High.

$$V_{ASHH} = \frac{1000 \cdot (R_{SGH} + 2.75 \cdot 10^3)}{1934 \cdot 10^3 + (31.75 \cdot R_{SGH})}$$

$R_{SGH}$  to  $V_{CC}$  must be greater than 100 k $\Omega$ .

5.  $V_{APPH} = 4.17 + V_{ASH}$

$$I_{LOOPH} = \frac{V_{APPH}}{\frac{(R_{DC1} + R_{DC2})}{600} + 2R_F + R_{LOOP}}$$

## RING-TRIP COMPONENTS

$$R_{RT2} = 12 \text{ k}\Omega$$

$$C_{RT} = 1.5 \text{ }\mu\text{F}$$

$$R_{RT1} = 320 \cdot CF \cdot \frac{V_{BAT1}}{V_{BAT1} - 5 - (24 \text{ }\mu\text{A} \cdot 320 \cdot CF \cdot (R_{LRT} + 150 + 2R_F))} \cdot (R_{LRT} + 150 + 2R_F)$$

where  $R_{LRT}$  = Loop-detection threshold resistance for ring trip and  $CF$  = Crest factor of ringing signal ( $\approx 1.25$ )

### $R_{SLEW}$ , $C_{SLEW}$

Ring waveform rise time  $\approx 0.214 \cdot (R_{SLEW} \cdot C_{SLEW}) \approx tr$ .

For a 1.25 crest factor @ 20 Hz,  $tr \approx 10 \text{ mS}$ .

$\therefore (R_{SLEW} = 150 \text{ k}\Omega, C_{SLEW} = 0.33 \text{ }\mu\text{F})$

$C_{SLEW}$  should be changed if a different crest factor is desired.

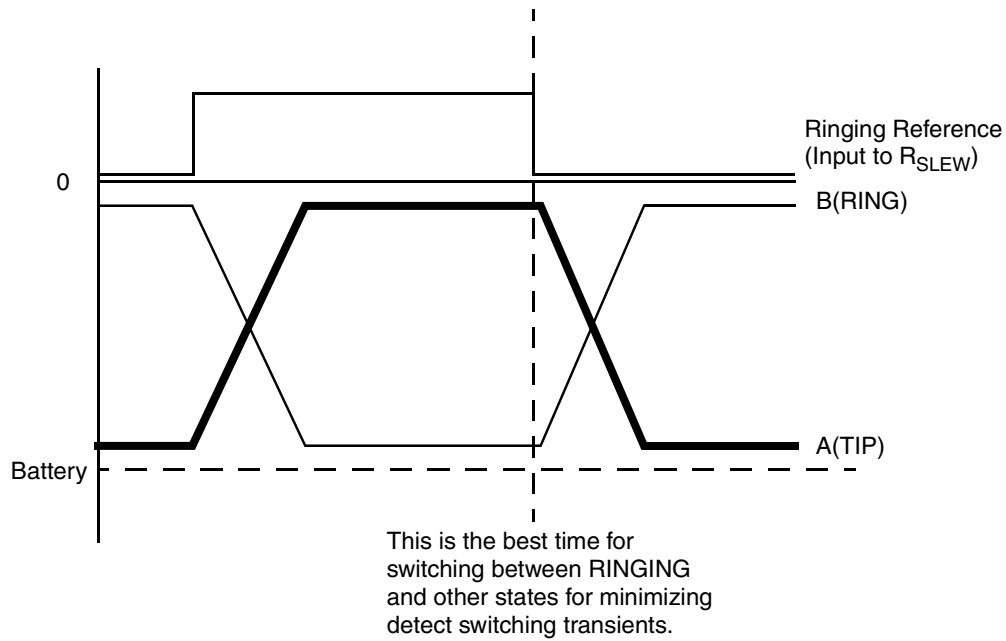
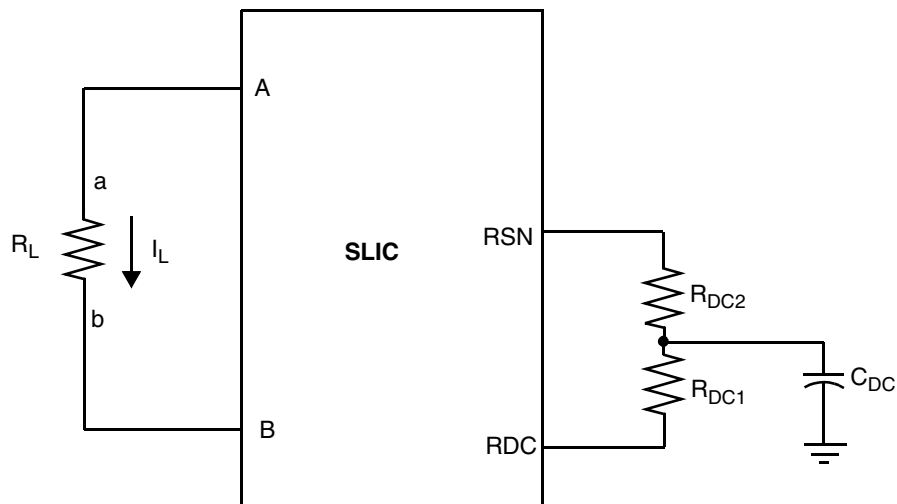


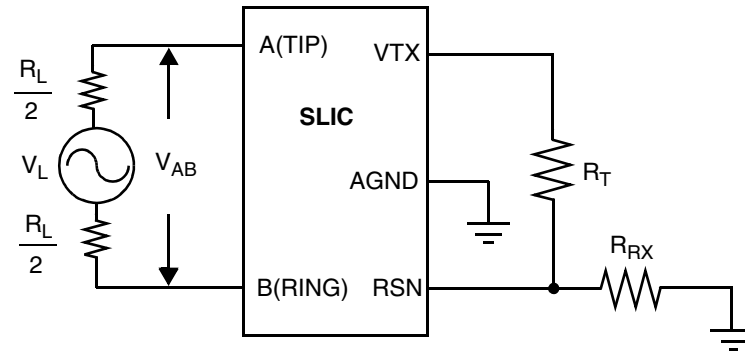
Figure 2. Ringing Waveforms



Feed current programmed by  $R_{DC1}$  and  $R_{DC2}$

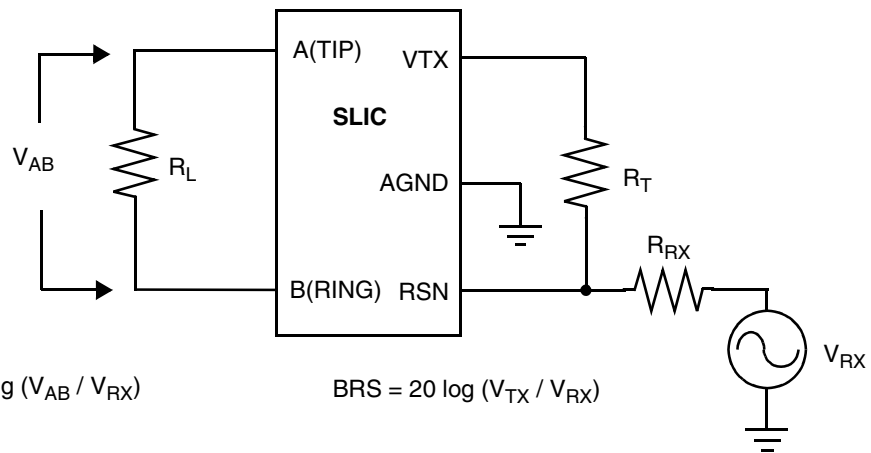
Figure 3. Feed Programming

## TEST CIRCUITS



$$I_{L2-4} = 20 \log (V_{TX} / V_{AB})$$

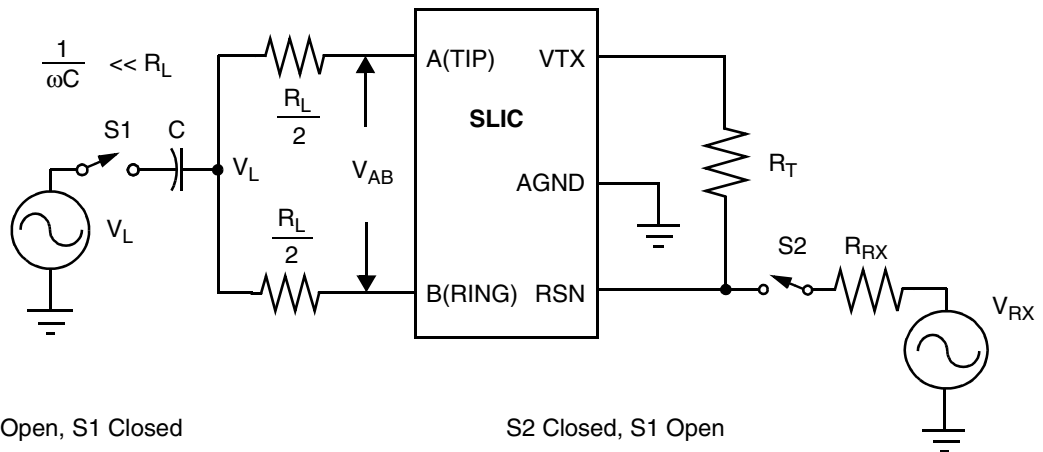
### A. Two- to Four-Wire Insertion Loss



$$I_{L4-2} = 20 \log (V_{AB} / V_{RX})$$

$$BRS = 20 \log (V_{TX} / V_{RX})$$

### B. Four- to Two-Wire Insertion Loss and Four- to Four-Wire Balance Return Signal



S2 Open, S1 Closed

$$L-T \text{ Long. Bal.} = 20 \log (V_{AB} / V_L)$$

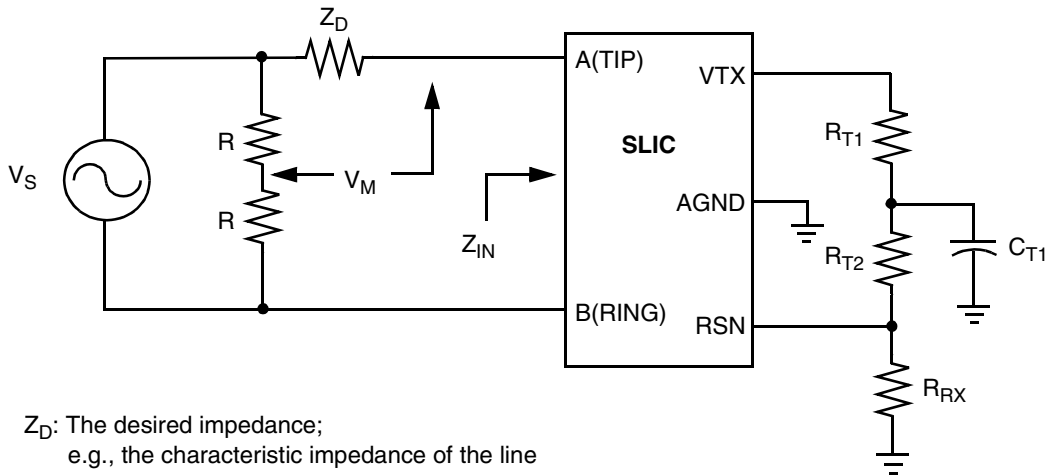
$$L-4 \text{ Long. Bal.} = 20 \log (V_{TX} / V_L)$$

S2 Closed, S1 Open

$$4-L \text{ Long. Sig. Gen.} = 20 \log (V_L / V_{RX})$$

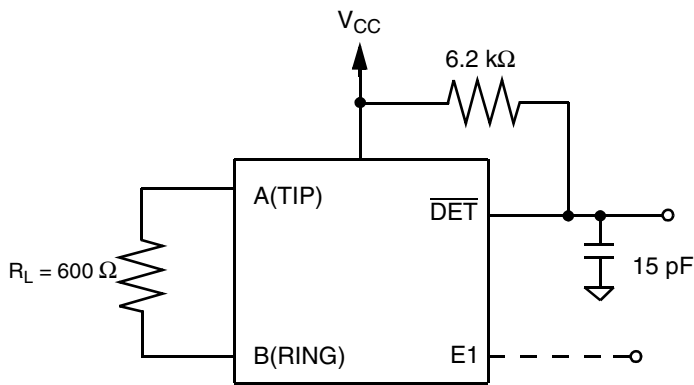
### C. Longitudinal Balance

## TEST CIRCUITS (continued)

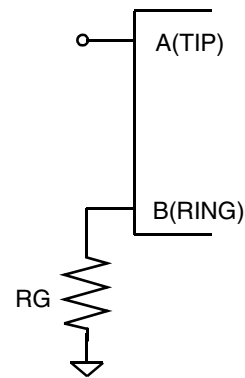


$$\text{Return loss} = -20 \log (2 V_M / V_S)$$

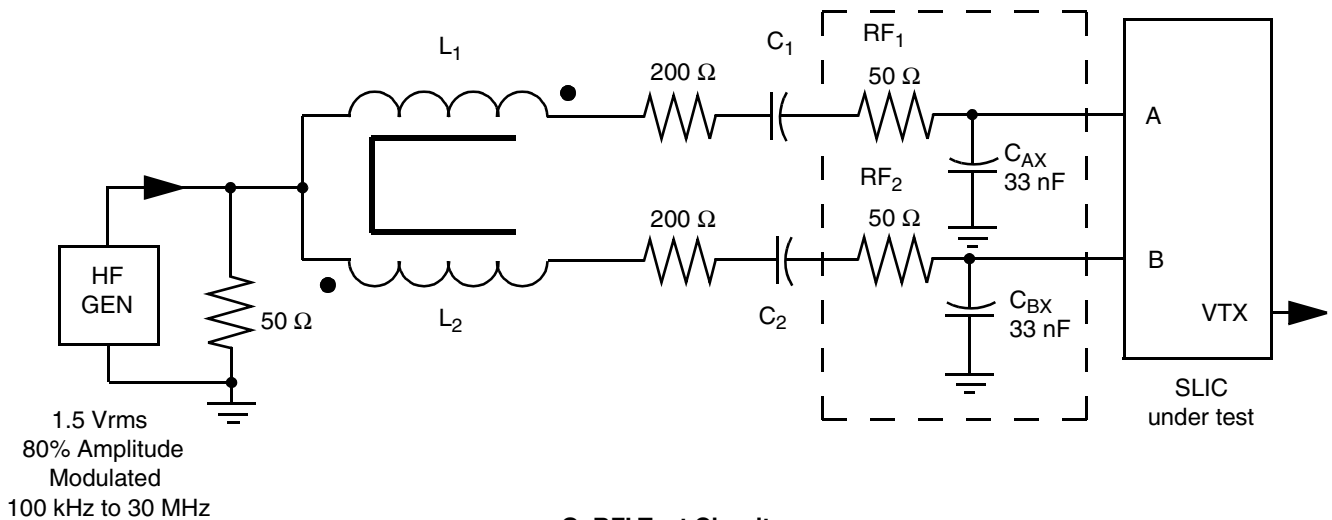
### D. Two-Wire Return Loss Test Circuit



### E. Loop-Detector Switching

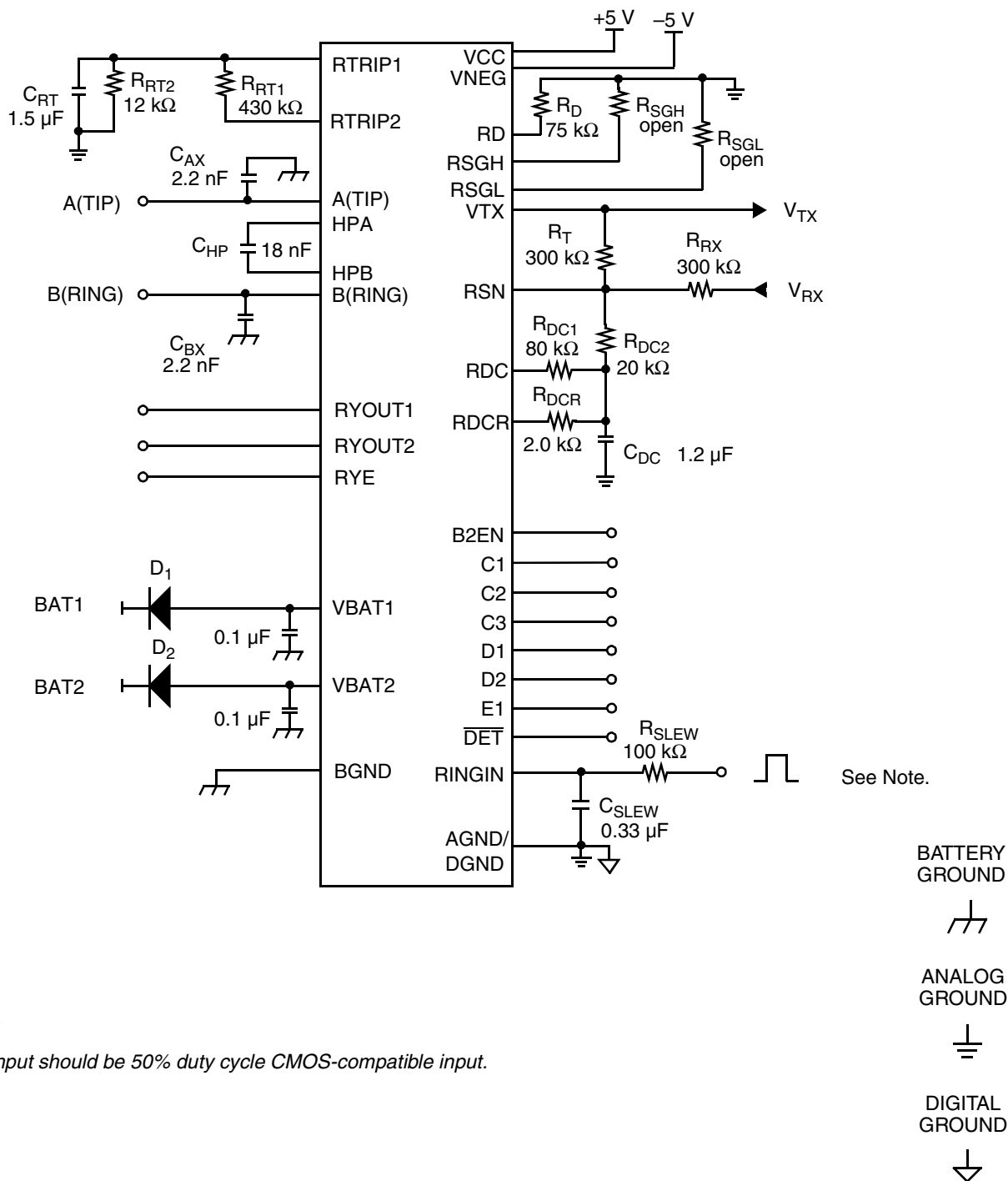


### F. Ground-Key Switching



### G. RFI Test Circuit

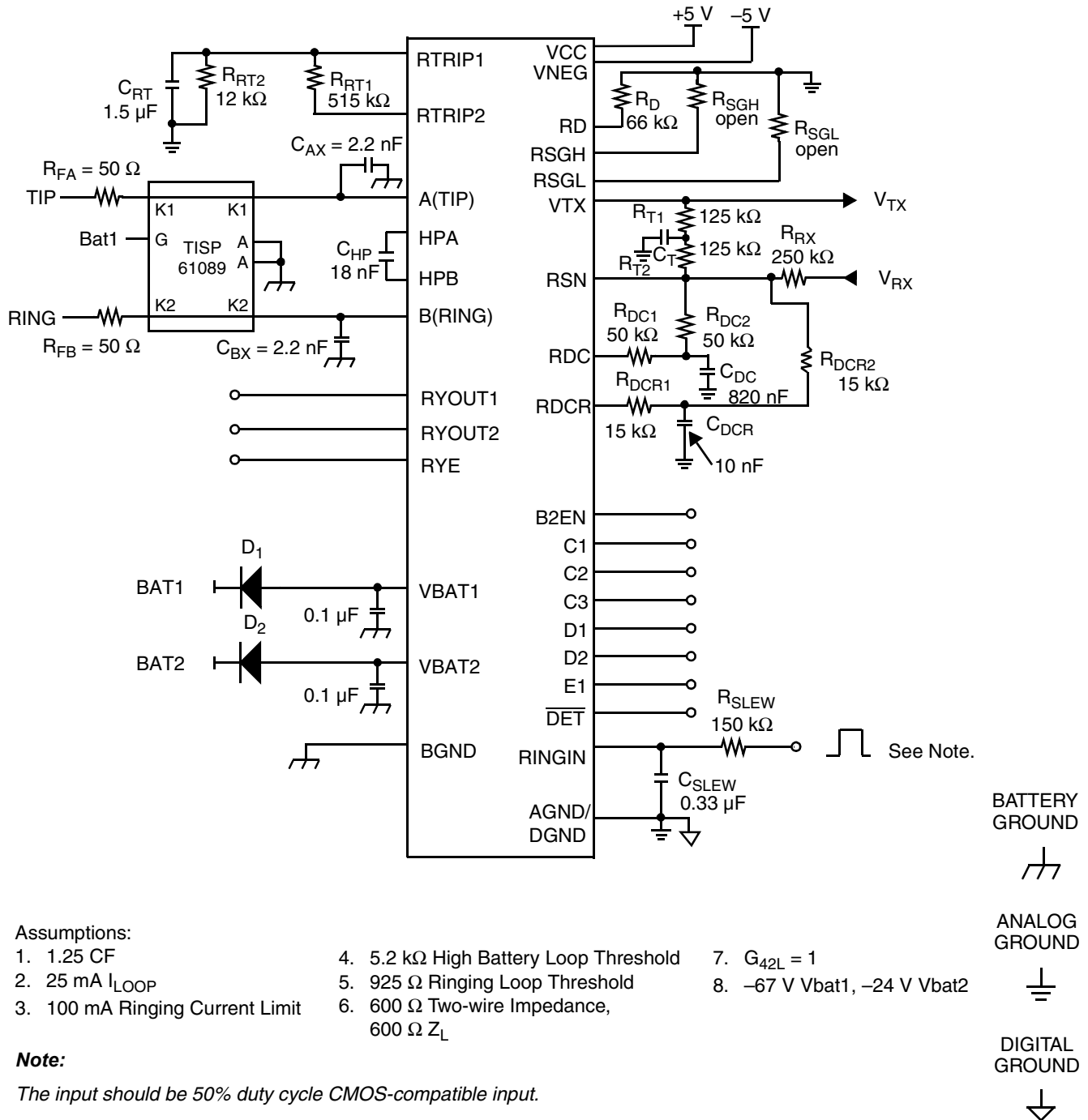
## TEST CIRCUITS (continued)



H. Le79R70 Test Circuit



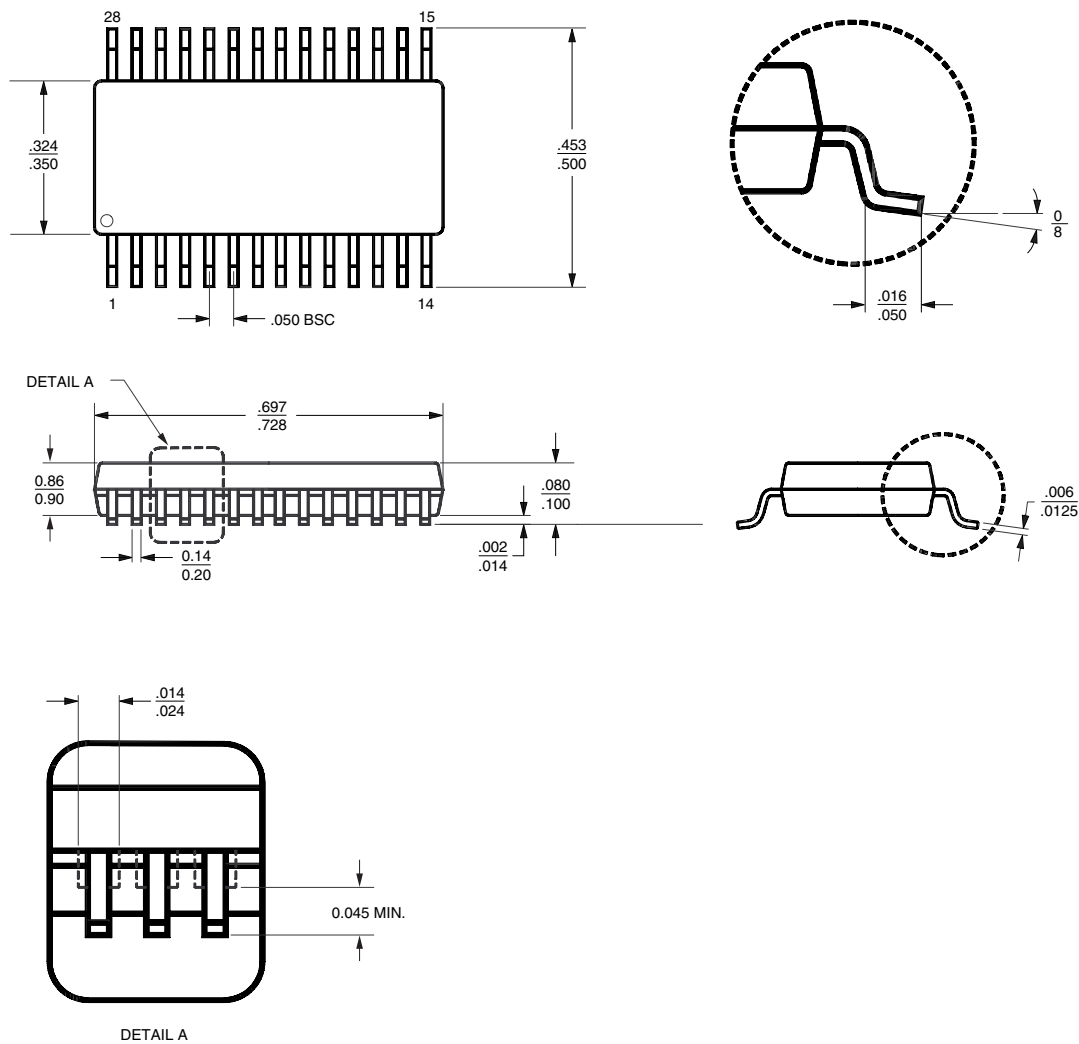
## APPLICATION CIRCUIT



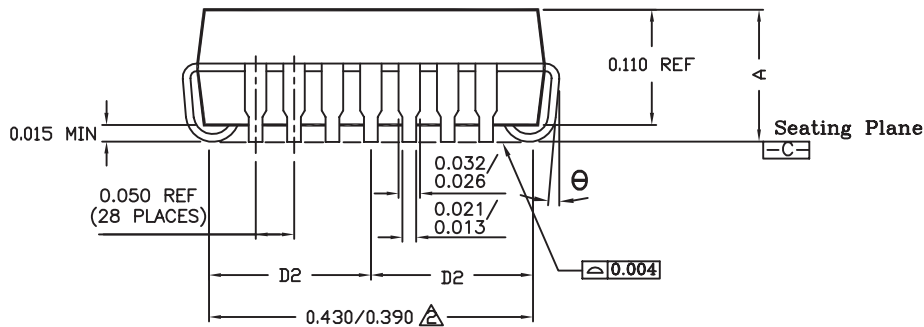
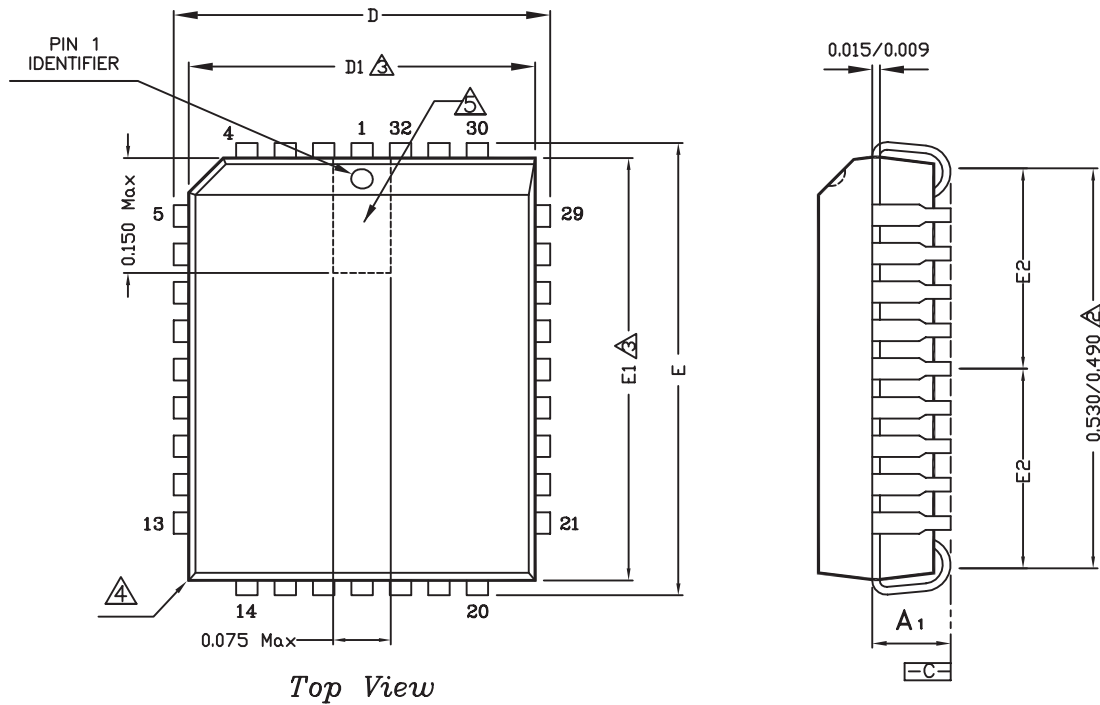
### I. Application Circuit

## PHYSICAL DIMENSIONS

### 28-Pin SOIC



## 32-Pin PLCC

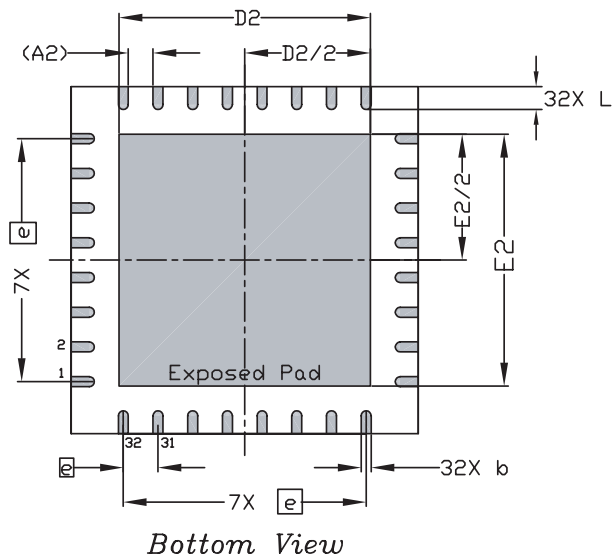
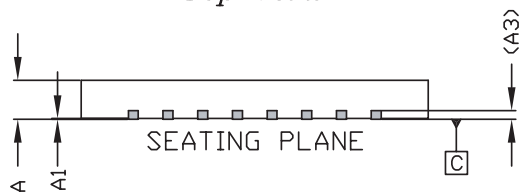
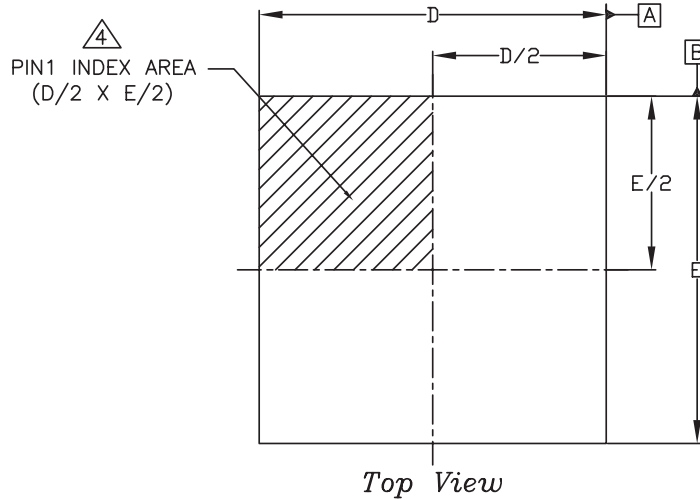


### NOTE :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
- △ TO BE MEASURED AT SEATING PLANE  $\square C \square$  CONTACT POINT.
- △ DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.010 IN PER SIDE. DIMENSIONS D, AND E, INCLUDE MOLD MISMATCH AND DETERMINED AT THE PARTING LINE; THAT IS D1 AND E1 ARE MEASURED AT THE EXTREME MATERIAL CONDITION AT THE UPPER OR LOWER PARTING LINE.
- △ EXACT SHAPE OF THIS FEATURE IS OPTIONAL.
- △ DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
6. SUM OF DAM BAR PROTRUSIONS TO BE 0.007 MAX PER LEAD.
7. CONTROLLING DIMENSION : INCH.
8. REFERENCE DOCUMENT : JEDEC MS-016

Symbol	Dimension in inch		
	Min	Nom	Max
A	0.125	—	0.140
A1	0.075	0.090	0.095
D	0.485	0.490	0.495
D1	0.447	0.450	0.453
D2	0.205 REF		
E	0.585	0.590	0.595
E1	0.547	0.550	0.553
E2	0.255 REF		
θ	0°	—	10°

## 32-Pin QFN



Symbol	Dimension in mm		
	Min	Nom	Max
A	0.80	0.90	1.00
A2	0.57 REF		
b	0.18	0.23	0.28
D	8.00 BSC		
D2	5.70	5.80	5.90
E	8.00 BSC		
E2	5.70	5.80	5.90
e	0.80 BSC		
L	0.43	0.53	0.63
N	32		
A1	0.00	0.02	0.05
A3	0.20 REF		

### NOTES :

- DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS,  $\theta$  IS IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEP 95-1 SSP-012. DETAILS OF THE TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- COPLANARITY APPLIES TO EXPOSED PAD AS WELL AS THE TERMINALS.
- REFERENCE DOCUMENT : JEDEC MO-220

## REVISION SUMMARY

### Revision A to Revision B

- Minor changes were made to the data sheet style and format to conform to Legerity standards.

### Revision B to Revision C

- The 28-pin SOIC information and package was added to the Ordering Information and the Connection Diagrams sections.
- The physical dimensions (PL032 and SOW28) were added to the Physical Dimensions section.
- Updated the Pin Description table to correct inconsistencies.

### Revision C to Revision D

- Changed Ring-Trip Components equation from:

$$R_{RT1} = 300 \cdot CF \cdot \frac{V_{BAT1}}{V_{bat} - 3.5 - (15 \mu A \cdot 300 \cdot CF \cdot (R_{LRT} + 150 + 2R_F))} \cdot (R_{LRT} + 150 + 2R_F)$$

To:

$$R_{RT1} = 320 \cdot CF \cdot \frac{V_{BAT1}}{V_{bat} - 5 - (24 \mu A \cdot 320 \cdot CF \cdot (R_{LRT} + 150 + 2R_F))} \cdot (R_{LRT} + 150 + 2R_F)$$

### Revision D to Revision E

- In “Ordering Information” section, added description for wafer foundry facility optional character.

### Revision E to F

- Updated device name from “Am79R70” to “Le79R70” throughout document.
- Added QFN package to “Connection Diagram,” “Absolute Maximum Ratings,” and “Physical Dimensions.”
- Removed reference to PLCC package type in “General Description.”
- Ordering Information: Temperature statement updated to standard.
- Absolute Maximum Ratings: Notes updated to standard.
- Operating Ranges: Temperature statement updated to standard.
- Removed obsolete “Sales Office Listing.”

The contents of this document are provided in connection with Legerity, Inc. products. Legerity makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to make changes to specifications and product descriptions at any time without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this publication. Except as set forth in Legerity's Standard Terms and Conditions of Sale, Legerity assumes no liability whatsoever, and disclaims any express or implied warranty, relating to its products including, but not limited to, the implied warranty of merchantability, fitness for a particular purpose, or infringement of any intellectual property right.

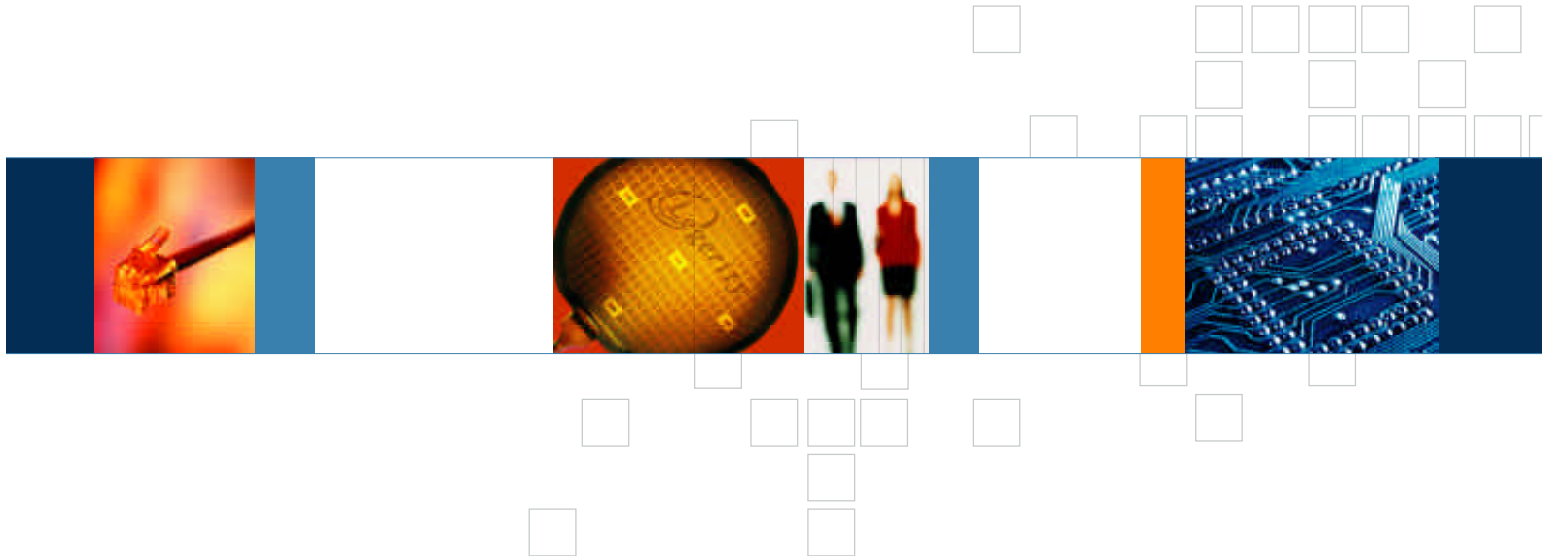
Legerity's products are not designed, intended, authorized or warranted for use as components in systems intended for surgical implant into the body, or in other applications intended to support or sustain life, or in any other application in which the failure of Legerity's product could create a situation where personal injury, death, or severe property or environmental damage may occur. Legerity reserves the right to discontinue or make changes to its products at any time without notice.

**© 2002 Legerity, Inc.**  
All rights reserved.

#### **Trademarks**

Legerity, the Legerity logo and combinations thereof, and DSLAC, QSLAC are trademarks of Legerity, Inc.

Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.



Legerity  
P.O. Box 18200  
Austin, Texas 78760-8200

512-228-5400 Corporate Office  
512-228-5507 Fax  
800-432-4009 North America Toll Free

To contact the Legerity Sales Office nearest you,  
or to download or order product literature, visit  
our web site at [www.legerity.com](http://www.legerity.com)

To order literature in North America,  
call: 800-572-4859  
or email: [americalit@legerity.com](mailto:americalit@legerity.com)

To order literature in Europe or Asia,  
call: 44-0-1179-341607  
or email: Europe - [eurolit@legerity.com](mailto:eurolit@legerity.com)  
Asia - [asialit@legerity.com](mailto:asialit@legerity.com)