

## Intelligent Subscriber Line Interface Circuit Am79R241\*/Le79R241 Device

### APPLICATIONS

- Enables a cost effective voice solution for long or short loop applications providing POTS and integrated test capabilities

- CO
- DLC
- PBX/KTS
- Pair gain

### FEATURES

- Monitor of two-wire interface voltages and currents supports

- Voice transmission
- Internal chip ring generation
- Programmable DC feed characteristics
  - Independent of battery
  - Current limited
- Selectable off-hook and ground-key thresholds
- Subscriber line diagnostics
  - Leakage resistance
  - Loop resistance
  - Line capacitance
  - Bell capacitance
  - Foreign voltage sensing
- Power cross and fault detection

- Supports internal short loop or external ringing

- +5 V and battery supplies

- Dual battery operation for system power saving

- Automatic battery switching
- Intelligent thermal management

- Compatible with inexpensive protection networks

- Accommodates low tolerance fuse resistors or PTC thermistors

- Metering capable

- 12 kHz and 16 kHz
- Smooth polarity reversal

- Tip-open state supports ground start signaling

- Integrated test load switches/relay drivers

- 5 REN with DC offset trapezoid.

For US standard:

- drives ring up to 4.4 kft of 26 gauge wire.

or

- drives ring up to 7 kft of 24 gauge wire.

For European (British) standard:

- drives ring up to 1.7 km of 0.5 mm copper cable.

- Space Saving Package Options (8x8 QFN)

### ORDERING INFORMATION

An ISLAC™ device must be used with this part.

| Device       | Package     |
|--------------|-------------|
| Am79R241JC*  | 32-Pin PLCC |
| Le79R241JC   | 32-Pin PLCC |
| Le79R241QC** | 32-Pin QFN  |

\*This product can be ordered using ordering part numbers Am79R241 or Le79R241. The Am79R241 ordering part number will be discontinued after 6/30/02, at which time the product will only be available using the Le79R241 ordering part number.

\*\*Due to size constraints, QFN devices are marked by omitting the "Le" prefix. For example, Le79R241QC is marked 79R241QC.

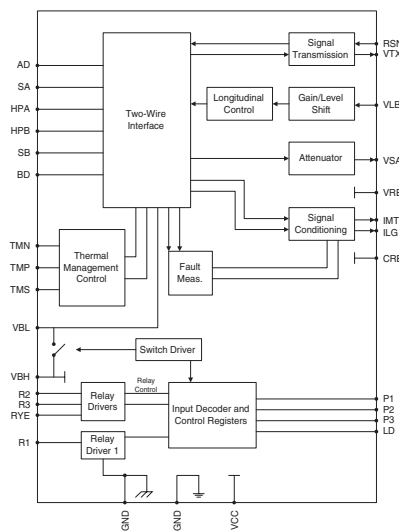
### DESCRIPTION

The Le79R241 device, in combination with an ISLAC™ device, implements the telephone line interface function. This enables the design of a low cost, high performance, fully software programmable line interface for multiple country applications worldwide. All AC, DC, and signaling parameters are fully programmable via microprocessor or GCI interfaces on the ISLAC device. Additionally, the Le79R241 device has integrated self-test and line-test capabilities to resolve faults to the line or line circuit. The integrated test capability is crucial for remote applications where dedicated test hardware is not cost effective.

### RELATED LITERATURE

- 080250 Le79Q2241/2242/2243 QISLAC Data Sheet
- 080262 Intelligent Access™ Voice Solutions Evaluation Board User's Guide
- 080344 Le79R2xx/Le79Q224x ISLIC™/Quad ISLAC™ Technical Reference

### BLOCK DIAGRAM



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## PRODUCT DESCRIPTION

Legerity's Intelligent Access™ voice chip sets integrate all functions of the subscriber line. Two chip types are used to implement the line card — an Le79R241 device and the Le79Q2241/2242/2243 ISLAC device. These provide the following basic functions:

1. The Le79R241 device: A high voltage, bipolar device that drives the subscriber line, maintains longitudinal balance and senses line conditions.
2. The Le79Q2241/2242/2243 ISLAC device: A low voltage CMOS IC that provides conversion, control and DSP functions for the Le79R241 device.

A complete schematic of the line card using an Intelligent Access voice chip set for internal and external ringing is shown in "Application Circuits" on page 19.

The Le79R241 device uses reliable, bipolar technology to provide the power necessary to drive a wide variety of subscriber lines. It can be programmed by the ISLAC device to operate in eight different modes that control power consumption and signaling. This enables it to have full control over the subscriber loop. The Le79R241 device is designed to be used exclusively with the ISLAC devices. The Le79R241 device requires only +5 V power and the battery supplies for its operation.

The Le79R241 device implements a linear loop-current feeding method with the enhancement of intelligent thermal management. This limits the amount of power dissipated on the Le79R241 device chip by dissipating power in external resistors in a controlled manner.

Each ISLAC device contains high-performance circuits that provide A/D and D/A conversion for the voice (codec), DC-feed and supervision signals. The ISLAC device contains a DSP core that handles signaling, DC-feed, supervision and line diagnostics for all channels.

The DSP core selectively interfaces with three types of backplanes:

- Standard PCM/MPI
- Standard GCI
- Modified GCI with a single analog line per GCI channel

The Intelligent Access voice chip set provides a complete software configurable solution to the BORSCHT functions as well as complete programmable control over subscriber line DC-feed characteristics, such as current limit and feed resistance. In addition, these chip sets provide system level solutions for the loop supervisory functions and metering. In total, they provide a programmable solution that can satisfy worldwide line card requirements by software configuration.

Software programmed filter coefficients, DC-feed data and supervision data are easily calculated with WinSLAC™ software. This PC software is provided free of charge. It allows the designer to enter a description of system requirements. WinSLAC then computes the necessary coefficients and plots the predicted system results.

The Le79R241 device interface unit inside the ISLAC device processes information regarding the line voltages, loop currents and battery voltage levels. These inputs allow the ISLAC device to place several key Le79R241 device performance parameters under software control.

The main functions that can be observed and/or controlled through the ISLAC backplane interface are:

- DC-feed characteristics
- Ground-key detection
- Off-hook detection
- Metering signal
- Longitudinal operating point
- Subscriber line voltage and currents
- Ring-trip detection
- Abrupt and smooth battery reversal
- Subscriber line matching
- Ringing generation
- Sophisticated line and circuit tests

To accomplish these functions, the ISLAC device collects the following information and feeds it, in analog form, to the ISLAC device:

- The metallic (IMT) and longitudinal (ILG) loop currents
- The AC (VTX) and DC (VSAB) loop voltage

The outputs supplied by the ISLAC device to the ISLAC device are then:

- A voltage ( $VHL_i^*$ ) that provides control for the following high-level ISLAC device outputs:
  - DC loop current

- Internal ringing signal
- 12 or 16 kHz metering signal
- A low-level voltage proportional to the voice signal ( $VOUT_i$ )
- A voltage that controls longitudinal offset for test purposes ( $VLB_i$ )

The ISLAC device performs the codec and filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters set the receive and transmit gain, perform the transhybrid balancing function, permit adjustment of the two-wire termination impedance and provide frequency attenuation adjustment (equalization) of the receive and transmit paths. Adaptive transhybrid balancing is also included. All programmable digital filter coefficients can be calculated using WinSLAC software. The PCM codes can be either 16-bit linear two's-complement or 8-bit companded A-law or  $\mu$ -law.

Besides the codec functions, the Intelligent Access voice chip set provides all the sensing, feedback, and clocking necessary to completely control ISLIC device functions with programmable parameters. System-level parameters under programmable control include active loop current limits, feed resistance, and feed mode voltages.

The ISLAC device supplies complete mode control to the ISLIC device using the control bus (P1-P3) and tri-level load signal ( $LD_i$ ).

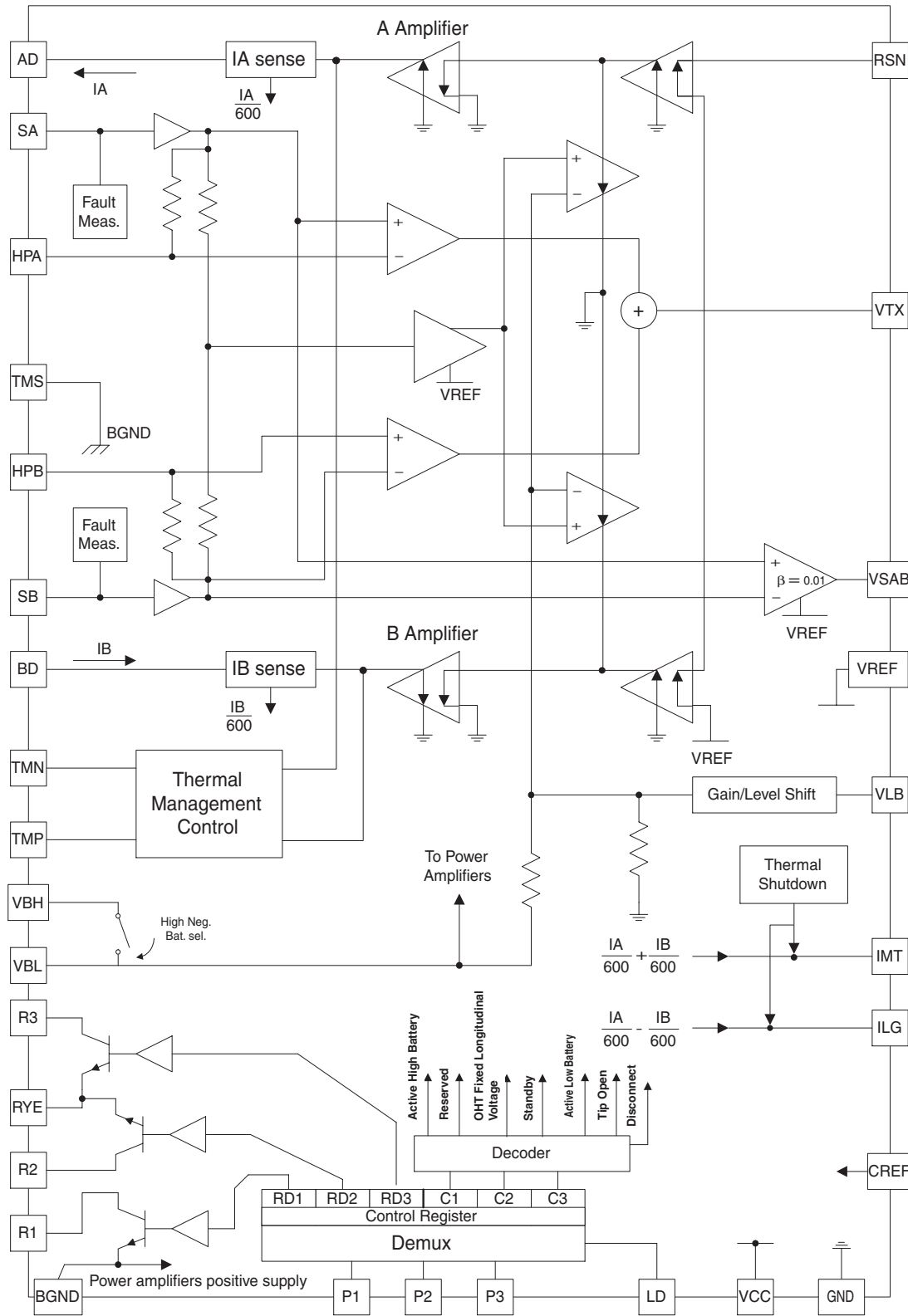
The Intelligent Access voice chip set provides extensive loop supervision capability including off-hook, ring-trip and ground-key detection. Detection thresholds for these functions are programmable. A programmable debounce timer is available that eliminates false detection due to contact bounce.

For subscriber line diagnostics, AC and DC line conditions can be monitored using built-in test tools. Measured parameters can be compared to programmed threshold levels to set a pass/fail bit. The user can choose to send the actual measurement data directly to a higher level processor by way of the PCM voice channel. Both longitudinal and metallic resistance and capacitance can be measured, which allows leakage resistance, line capacitance, and telephones to be identified.

**\*Note:**

*i = channel number*

## LE79R241 DEVICE INTERNAL BLOCK DIAGRAM

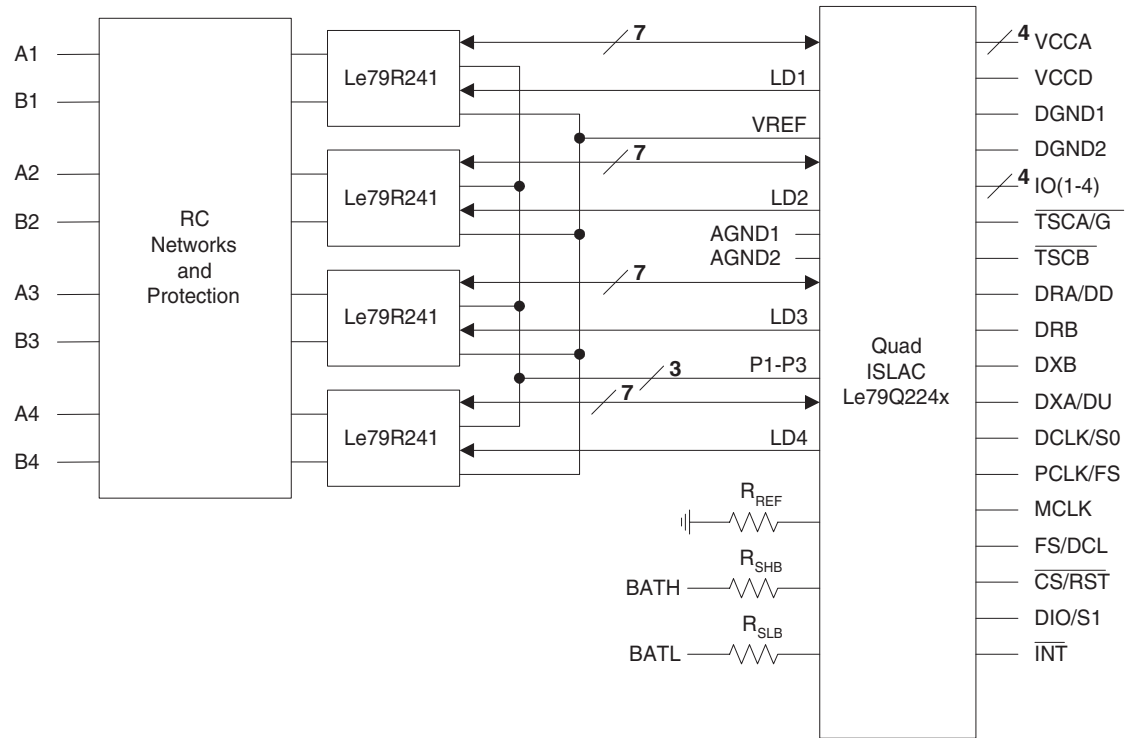


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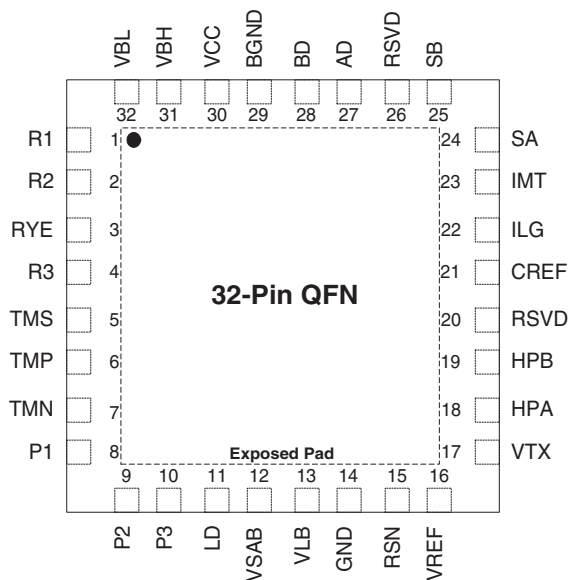
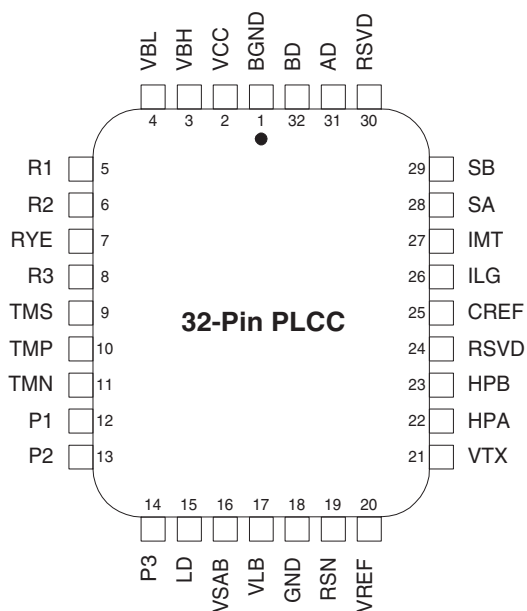
## FEATURES OF THE INTELLIGENT ACCESS™ CHIP SET

- Performs all battery feed, ringing, signaling, hybrid and test (BORSCHT) functions
- Two chip solution supports high density, multi-channel architecture
- Single hardware design meets multiple country requirements through software programming of:
  - Ringing waveform and frequency
  - DC loop-feed characteristics and current-limit
  - Loop-supervision detection thresholds
    - Off-hook debounce circuit
    - Ground-key and ring-trip filters
  - Off-hook detect de-bounce interval
  - Two-wire AC impedance
  - Transhybrid balance
  - Transmit and receive gains
  - Equalization
  - Digital I/O pins
  - A-law/ $\mu$ -law and linear selection
- Supports internal and external battery-backed ringing
  - Self-contained ringing generation and control
  - Supports external ringing generator and ring relay
  - Ring relay operation synchronized to zero crossings of ringing voltage and current
  - Integrated ring-trip filter and software enabled manual or automatic ring-trip mode
- Supports metering generation with envelope shaping
- Smooth or abrupt polarity reversal
- Adaptive transhybrid balance
  - Continuous or adapt and freeze
- Supports both loop-start and ground-start signaling
- Exceeds LSSGR and CCITT central office requirements
- Selectable PCM or GCI interface
  - Supports most available master clock frequencies from 512 kHz to 8.192 MHz
- On-hook transmission
- Power/service denial mode
- Line-feed characteristics independent of battery voltage
- Only 5 V, 3.3 V and battery supplies needed
- Low idle-power per line
- Linear power-feed with intelligent power-management feature
- Compatible with inexpensive protection networks; Accommodates low-tolerance fuse resistors while maintaining longitudinal balance
- Monitors two-wire interface voltages and currents for subscriber line diagnostics
- Built-in voice-path test modes
- Power-cross, fault, and foreign voltage detection
- Integrated line-test features
  - Leakage
  - Line and ringer capacitance
  - Loop resistance
- Integrated self-test features
  - Echo gain, distortion, and noise
- Guaranteed performance over commercial and industrial temperature ranges.
- Up to three relay drivers per ISLIC™ device
  - Configurable as test load switches

## CHIP SET BLOCK DIAGRAM - FOUR CHANNEL LINE CARD EXAMPLE



## CONNECTION DIAGRAMS



1. Pin 1 is marked for orientation.
2. RSVD = Reserved. Do not connect to this pin.
3. The thermally enhanced QFN package features an exposed pad on the underside which must be electrically tied to VBH.



## PIN DESCRIPTIONS

| Pin Name      | Type              | Description   |
|---------------|-------------------|---|
| AD, BD        | Output            | Provide the currents to the A and B leads of the subscriber loop.   |
| BGND          | Ground            | Ground return for high and low battery supplies.  |
| CREF          | +3.3 VDC          | VCCD reference. It is the digital high logic supply rail, used by the ISLIC to ISLAC interface.   |
| GND           | Ground            | Analog and digital ground return for VCC.   |
| HPA, HPB      | Output            | These pins connect to CHP, the external high-pass filter capacitor that separates the DC loop-voltage from the voice transmission path.   |
| ILG           | Output            | ILG is proportional to the common-mode line current (IAD+IBD), except in disconnect mode, where ILG is proportional to the current into grounded SB.  |
| IMT           | Output            | IMT is proportional to the differential line current (IAD + IBD), except in disconnect mode, where IMT is proportional to the current into grounded SA. The Le79R241 device indicates thermal overload by pulling IMT to CREF.  |
| LD            | Input             | The LD pin controls the input latch and responds to a 3-level input. When the LD pin is a logic 1 ( $C_{REF} - 1$ ), the logic levels on P1–P3 latch into the Am79241 control register bits that operate the mode-decoder. When the LD pin is a logic 0 ( $< 0.6$ ), the logic levels on P1–P3 latch into the Am79241 control register bits that control the relay drivers (RD1–RD3). When the LD pin level is at $\sim V_{REF} \pm 0.3$ V, the control register contents are locked. |
| P1–P3         | Input             | Inputs to the latch for the operating-mode decoder and the relay-drivers.   |
| R1            | Output            | Collector connection for relay 1 driver. Emitter internally connected to BGND.  |
| R2            | Output            | Collector connection for relay 2 driver. Emitter internally connected to RYE  |
| R3            | Output            | Collector connection for relay 3 driver. Emitter internally connected to RYE.   |
| RSN           | Input             | The metallic current between AD and BD is equal to 500 times the current into this pin. Networks that program receive gain and two-wire impedance connect to this node. This input is at a virtual potential of VREF.   |
| RSVD          | Reserved          | These pins are used during Legerity testing. In the application, they must be left floating.  |
| RYE           | Output            | Emitter connection for R2 and R3. Normally connected to relay ground.   |
| SA, SB        | Input             | Sense the voltages on the line side of the fuse resistors at the A and B leads. External sense resistors, RSA and RSB, protect these pins from lightning or power-cross.  |
| TMP, TMN, TMS | Output            | External resistors connected from TMP to TMS and TMN to VBL to offload excess power from the Le79R241 device.   |
| VBH           | Battery (Power)   | Connection to high-battery supply used for ringing and long loops. Connects to the substrate. When only a single battery is available, it connects to both VBH and VBL.   |
| VBL           | Battery (Power)   | Connection to low-battery supply used for short loops. When only a single battery is available, this pin can be connected to VBH.   |
| VCC           | +5 V Power Supply | Positive supply for low voltage analog and digital circuits in the Le79R241 device.   |
| VLB           | Input             | Sets the DC longitudinal voltage of the Le79R241 device. It is the reference for the longitudinal control loop. When the VLB pin is greater than VREF, the Le79R241 device sets the longitudinal voltage to a voltage approximately half-way between the positive and negative power supply battery rails. When the VLB pin is driven to levels between 0V and VREF, the longitudinal voltage decreases linearly with the voltage on the VLB pin.                                     |
| VREF          | Input             | The ISLAC chip provides this voltage which is used by the Le79R241 device for internal reference purposes. All analog input and output signals interfacing to the ISLAC chip are referenced to this pin.  |
| VSAB          | Output            | Scaled-down version of the voltage between the sense points SA and SB on this pin.  |
| VTX           | Output            | The voltage between this pin and VREF is a scaled down version of the AC component of the voltage sensed between the SA and SB pins. One end of the two-wire input impedance programming network connects to VTX. The voltage at VTX swings positive and negative with respect to VREF.   |
| Exposed Pad   | Battery           | This must be electrically tied to VBH.  |

## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

Stresses greater than those listed under "Absolute Maximum Ratings" can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability

|  |                                   |
|--|-----------------------------------|
| Storage temperature                          | –55 to +150°C                     |
| Ambient temperature, under bias              | –40 to +85°C                      |
| Humidity                                     | 5% to 95%                         |
| VCC with respect to GND                      | –0.4 to +7 V                      |
| VBH, VBL with respect to GND (See note 2)    | +0.4 to –104 V                    |
| BGND with respect to GND                     | –3 to +3 V                        |
| Voltage on relay outputs                     | +7 V                              |
| AD or BD to BGND:                            |                                   |
| Continuous                                   | VBH – 1 to BGND + 1               |
| 10 ms (F = 0.1 Hz)                           | VBH – 5 to BGND + 5               |
| 1 $\mu$ s (F = 0.1 Hz)                       | VBH – 10 to BGND + 10             |
| 250 ns (F = 0.1 Hz)                          | VBH – 15 to BGND + 15             |
| Current into SA or SB:                       |                                   |
| 10 $\mu$ s rise to I <sub>peak</sub>         | I <sub>peak</sub> = $\pm$ 5 mA    |
| 1000 $\mu$ s fall to 0.5 I <sub>peak</sub> ; |                                   |
| 2000 $\mu$ s fall to I = 0                   |                                   |
| Current into SA or SB:                       |                                   |
| 2 $\mu$ s rise to I <sub>peak</sub>          | I <sub>peak</sub> = $\pm$ 12.5 mA |
| 10 $\mu$ s fall to 0.5 I <sub>peak</sub> ;   |                                   |
| 20 $\mu$ s fall to I = 0                     |                                   |
| SA SB continuous                             | 5 mA                              |
| Current through AD or BD                     | $\pm$ 150 mA                      |
| P1, P2, P3, LD to GND                        | –0.4 to VCC + 0.4 V               |
| Maximum power dissipation (see note 1)       |                                   |
| T <sub>A</sub> = 70° C                       |                                   |
| In 32-pin PLCC package                       | 1.67 W                            |
| In 32-pin QFN package                        | 3.00 W                            |
| T <sub>A</sub> = 85° C                       |                                   |
| In 32-pin PLCC package                       | 1.33 W                            |
| In 32-pin QFN package                        | 2.40 W                            |
| ESD Immunity (Human Body Model)              | 1.5 kV min                        |

**Note:**

1. Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. Operation above 145°C junction temperature may degrade device reliability.

*The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to a large internal copper plane.*

2. Rise time of VBH (dv/dt) must be limited to less than 27 v/ms.

### Thermal Resistance

The junction to air thermal resistance of the Le79R241 device in a 32-pin PLCC package is 45° C/W and in a 32-pin QFN package is 25° C/W (measured under free air convection conditions and without external heat sinking).

### Electrical Operating Ranges

Legerity guarantees the performance of this device over commercial (0°C to 70°C) and industrial (–40°C to 85°C) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore TR-TSY-000357 Component Reliability Assurance Requirements for Telecommunications Equipment.

### Environmental Ranges

|                           |                                    |
|---------------------------|------------------------------------|
| Ambient Temperature       | 0 to 70°C Commercial               |
|                           | –40 to +85 °C extended temperature |
| Ambient Relative Humidity | 15 to 85%                          |

## Electrical Ranges

|                                 |                       |
|---------------------------------|-----------------------|
| VCC                             | 5 V $\pm$ 5%          |
| VBL                             | –15 V to VBH          |
| VBH                             | –42.5 to –99 V        |
| BGND with respect to GND        | –100 to +100 mV       |
| Load resistance on VTX to Vref  | 20 k $\Omega$ minimum |
| Load resistance on VSAB to Vref | 20 k $\Omega$ minimum |

## SPECIFICATIONS

### Power Dissipation

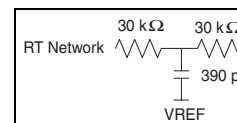
Loop resistance = 0 to  $\infty$  unless otherwise noted (not including fuse resistors), 2 x 50  $\Omega$  fuse resistors, BATL = –36 V, BATH = –90 V, VCC = +5 V. For power dissipation measurements, DC-feed conditions are as follows:

- ILA (Active mode current limit) = 25 mA (IRSN = 50  $\mu$ A)
- RFD (Feed resistance) = 500  $\Omega$
- VAS (Anti-sat activate voltage) = 10 V
- VAPP (Apparent Battery Voltage) = 48 V
- RMGLi = RMGPi (Thermal management resistors) = 1 k $\Omega$

| Description                       | Test Conditions                                    | Min          | Typ        | Max | Unit |
|-----------------------------------|--|--------------|------------|-----|------|
| Power Dissipation Normal Polarity | On-Hook Disconnect                                 |              | 55         | 70  | mW   |
|                                   | On-Hook Standby                                    |              | 80         | 100 |      |
|                                   | On-Hook Transmission<br>Fixed Longitudinal Voltage | ISLIC        | 175        | 215 |      |
|                                   | On-Hook Active High Battery                        | ISLIC        | 340        | 400 |      |
|                                   | Off-Hook Active Low Battery<br>RL = 294 $\Omega$   | ISLIC<br>TMG | 700<br>200 | 800 |      |
| Power Supply Currents             | On-Hook Disconnect                                 | VBH          | 0.4        | 0.7 | mA   |
|                                   |  | VBL          | 0.1        |     |      |
|                                   |  | VCC          | 3.0        | 3.5 |      |
|                                   | On-Hook Standby                                    | VBH          | 0.75       | 1.1 |      |
|                                   |  | VBL          | 0          |     |      |
|                                   |  | VCC          | 3.1        | 3.5 |      |
|                                   | On-Hook Transmission<br>Fixed Longitudinal Voltage | VBH          | 1.85       | 2.5 |      |
|                                   |  | VBL          | 0          |     |      |
|                                   |  | VCC          | 5          | 6   |      |
|                                   | On-Hook Active High Battery                        | VBH          | 3.6        | 4.5 |      |
|                                   |  | VBL          | 0          |     |      |
|                                   |  | VCC          | 7.3        | 8.0 |      |
|                                   | Off-Hook Active Low Battery<br>RL = 294 $\Omega$   | VBH          | 0.9        | 2.0 |      |
|                                   |  | VBL          | 26.9       |     |      |
|                                   |  | VCC          | 7.5        | 10  |      |

## DC Specifications

Unless otherwise specified, test conditions are: VCC = 5 V, RMGPi = RMGLi = 1 k $\Omega$ , BATH = -90 V, BATL = -36 V, RRX = 150 k $\Omega$ , RL = 600  $\Omega$ , RSA = RSB = 200 k $\Omega$ , RFA = RFB = 50  $\Omega$ , CHP = 22 nF, CAD = CBD = 22 nF, IRSN = 50  $\mu$ A, Active low battery. DC-feed conditions are normally set by the ISLAC device. When the Le79R241 device is tested by itself, its operating conditions must be simulated as if it were connected to an ideal ISLAC device.

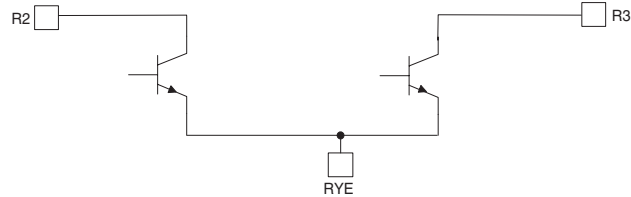


| No. | Item   | Condition  | Min                                | Typ                         | Max                            | Unit   | Note        |
|-----|--|--|------------------------------------|-----------------------------|--------------------------------|--|-------------|
| 1   | Two-wire loop voltage (including offset)   | Standby mode, open circuit,<br> VBH  < 55 V<br> VBH  > 55 V<br>GND – VB<br>Any Active mode (does not include OHT),<br>RL = 600 $\Omega$ , IRSN = 50 $\mu$ A<br>OHT mode, RL = 2200 $\Omega$<br>IRSN = 20 $\mu$ A | VBH – 8<br>48<br>13.88<br><br>19.8 | VBH–7<br>51<br>15<br><br>22 | VBH–6<br>55.5<br>55.5<br>16.13 | V  | 2           |
| 2   | Feed resistance per leg at pins AD & BD  | Standby mode   | 130                                | 250                         | 375                            | W  | 2           |
| 3   | Feed current limit   | Feed current<br>Standby mode, RL = 600 $\Omega$  | 18                                 | 34                          | 45                             | mA   |             |
|     | IMT current  | Standby mode, RL = 2200 $\Omega$   | 44.6                               | 56                          |                                |  |             |
|     | ILG current  | Standby mode<br>A to VBH<br>B to Ground  | 28<br>28                           |                             |                                | $\mu$ A                                      |             |
| 4   | Ternary input voltage boundaries for LD pin. Mid-level input source must be Vref.        | Low boundary<br>Mid boundary<br>High boundary<br>Input high current<br>Input low current<br>Mid-level current  | VREF–0.3<br>CREF – 1               | VREF<br><br>108<br>47<br>51 | 0.6<br>VREF+0.3                | V<br>V<br>V<br>$\mu$ A<br>$\mu$ A<br>$\mu$ A | 2<br>2<br>2 |
| 5   | Logic Inputs P1, P2, P3  | Input high voltage<br>Input low voltage<br>Input high current<br>Input low current   | 2.0<br><br>-20<br>-20              | <br><br>0<br>0              | <br><br>0.8<br>20<br>20        | V<br>V<br>$\mu$ A<br>$\mu$ A                 |             |
| 6   | VTX output offset  |  | -50                                | 0                           | +50                            | mV   |             |
| 7   | VREF input current   | VREF = 1.4 V   |                                    | 50                          |                                | $\mu$ A                                      | 2           |
| 8   | CREF input current   | CREF = 3.3 V   | -3                                 | 0                           | 3                              | $\mu$ A                                      | 2           |
| 9   | $\beta$ , DC Ratio of VSAB to loop voltage:<br>$\beta = \frac{V_{SAB}}{V_{SA} - V_{SB}}$ | Tj < 145°C, VSA – VSB = 22 V   | 0.0088                             | 0.0097                      | 0.0106                         | V/V  |             |
| 10  | Fault Indicator Threshold  | Voltage Output on IMT  | 2.8                                | CREF – 0.3 V                | CREF                           | V  | 2           |
| 11  | Gain from VLB pin to A or B pin, KLG   |  |                                    | 30                          |                                | V/V  |             |
| 12  | VLB pin input current  | VLB = VREF $\pm$ 1 V   |                                    | 0                           | 100                            | $\mu$ A                                      | 2           |
| 13  | ILOOP/IMT  | ILOOP = 10 mA  | 275                                | 300                         | 325                            | A/A  |             |
| 14  | ILONG/ILG  | ILONG = 10 mA  | 565                                | 605                         | 645                            | A/A  |             |
| 15  | Input current, SA and SB pins  | Active modes   |                                    | 1.0                         | 3.0                            | $\mu$ A                                      | 2           |
| 16  | K1   | Incremental DC current gain  | 462.5                              | 500                         | 537.5                          |  | 2           |
| 17  | ISA/IMT  | Disconnect ISA = 2 mA  | 4                                  | 6                           | 8.75                           | A/A  |             |
| 18  | ISB/ILG  | Disconnect ISB = 2 mA  | 10                                 | 12                          | 16                             |  |             |
| 19  | VSAB output offset   | -40°C<br>+25°C<br>+85°C  |                                    | 7.0<br>3.6<br>1.4           |                                | mV   |             |
| 20  | IMT output offset  |  | -3                                 | 0                           | 3                              | $\mu$ A                                      |             |
| 21  | ILG output offset  |  | -1                                 | 0                           | 1                              | $\mu$ A                                      |             |

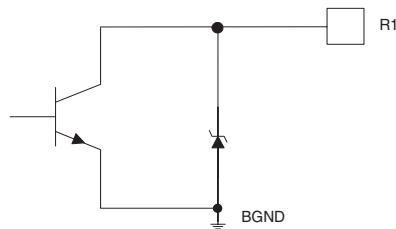
## Relay Driver Specifications

| Item              | Condition                 | Min | Typ | Max | Unit          | Note |
|-------------------|---------------------------|-----|-----|-----|---------------|------|
| On Voltage        | 25 mA/relay sink          |     | 0.4 | 0.5 | V             |      |
|                   | 40 mA/relay sink          |     | 0.8 | 1.0 |               |      |
| R2,R3 Off Leakage | R2,R3 = BGND<br>RYE = VBH |     | 0   | 100 | $\mu\text{A}$ |      |
| Zener Break Over  | $I_z = 100 \mu\text{A}$   | 6.6 | 7.9 | 10  | V             |      |
| Zener On Voltage  | $I_z = 30 \text{ mA}$     | 6   | 11  | 17  |               |      |

**Figure 1. Relay Drivers**



**A. Relay Driver Configuration**



**B. Ring Relay**

## Transmission Specifications

| No. | Item   | Condition   | Min              | Typ              | Max              | Unit     | Note            |
|-----|--|---|------------------|------------------|------------------|----------|-----------------|
| 1   | RSN input impedance                                | f = 300 to 3400 Hz  |                  | 1                |                  | $\Omega$ | 2               |
| 2   | VTX output impedance                               |   |                  | 3                |                  |          |                 |
| 3   | Max, AC + DC loop current                          | Active High Battery or Active Low Battery                               | 70               |                  |                  | mA       |                 |
| 4   | Longitudinal impedance, A or B to GND              | Active mode   |                  | 70               | 135              | $\Omega$ |                 |
| 5   | 2-4 wire gain                                      | -10 dBm, 1 kHz, 0 to 70°C<br>T <sub>A</sub> = -40°C to 85°C             | -14.13<br>-14.18 | -13.98<br>-13.98 | -13.83<br>-13.78 | dB       | 2               |
| 6   | 2-4 wire gain variation with frequency             | 300 to 3400 Hz, relative to 1 kHz<br>T <sub>A</sub> = -40°C to 85°C     | -0.1<br>-0.15    |                  | +0.1<br>+0.15    |          | 2               |
| 7   | 2-4 wire gain tracking                             | +3 dBm to -55 dBm<br>Reference: -10 dBm<br>T <sub>A</sub> = -40 to 85°C | -0.1<br>-0.15    |                  | +0.1<br>+0.15    |          | 2,5             |
| 8   | 4-2 wire gain                                      | -10 dBm, 1 kHz<br>T <sub>A</sub> = -40°C to 85°C                        | -0.15<br>-0.2    |                  | +0.15<br>+0.2    |          | 2               |
| 9   | 4-2 wire gain variation with frequency             | 300 to 3400 Hz, relative to 1 kHz                                       | -0.1             |                  | +0.1             |          |                 |
| 10  | 4-2 wire gain tracking                             | +3 dBm to -55 dBm<br>Reference: -10 dBm<br>-40°C to 85°C                | -0.1<br>-0.15    |                  | +0.1<br>+0.15    |          | 2, 5            |
| 11  | Total harmonic distortion level                    | 300 Hz to 3400 Hz   |                  |                  |                  | dB       |                 |
|     | 2-wire   | 0 dBm   |                  |                  | -50              |          |                 |
|     | 4-wire   | 11.2 dBm  |                  |                  | -40              |          |                 |
|     | 4-wire overload level at VTX OHT                   | -12 dBm<br>-0.8 dBm<br>RLOAD = 600 $\Omega$<br>VAB - 50 V 0 dBm         |                  | $\pm 1$<br>-50   | -48<br>-38       |          | 2<br>2          |
| 12  | Idle channel noise C-message                       | Active modes, R <sub>L</sub> = 600 $\Omega$                             |                  | +9               | +11              | dBrnC    |                 |
|     | Weighted   | 2-wire  |                  | -5               |                  |          |                 |
|     | Psophometric                                       | 4-wire  |                  | -81              | -79              | dBmp     |                 |
|     | Weighted   | 2-wire  |                  | -95              |                  | —        |                 |
| 13  | Longitudinal balance (IEEE method) Normal Polarity | L - T 200 to 1000 Hz<br>T <sub>A</sub> = -40°C to 85°C                  | 58<br>53         |                  |                  | dB       | 2               |
|     |  | 1000 to 3400 Hz<br>T <sub>A</sub> = -40°C to 85°C                       | 53<br>48         |                  |                  |          | 2               |
|     |  | T - L 200 to 3400 Hz  | 40               |                  |                  |          |                 |
|     |  | L - T, IL = 0 50 to 3400 Hz   |                  | 63               |                  |          | 3               |
|     | Reverse Polarity                                   | L - T 200 to 1000 Hz<br>T <sub>A</sub> = -40°C to 85°C                  | 50<br>48         |                  |                  |          | 2               |
| 14  | PSRR (VBH, VBL)                                    | 50 to 3400 Hz<br>3.4 to 50 kHz  | 25               | 45<br>40         |                  |          | 3, 4<br>1, 2, 4 |
| 15  | PSRR (VCC)   | 50 to 3400 Hz<br>3.4 to 50 kHz  | 25               | 45<br>35         |                  |          | 3, 4<br>1, 2, 4 |
| 16  | Longitudinal AC current per wire                   | F = 15 to 60 Hz Active mode   | 20               | 30               |                  | mArms    | 2               |
| 17  | Metering distortion                                | Freq = 12 kHz 2.8 Vrms<br>Freq = 16 kHz<br>metering load = 200 $\Omega$ | 40               |                  |                  | dB       | 2               |

## Ringling Specifications

| Item                 | Condition               | Min | Typ   | Max | Unit | Note |
|----------------------|-------------------------|-----|-------|-----|------|------|
| Peak Ringing Voltage | Active Internal Ringing |     | VBH+6 |     | V    | 7    |

## Current-Limit Behavior

| SLIC Mode      | Condition  | Min      | Typ           | Max      | Unit         | Note |
|----------------|--|----------|---------------|----------|--------------|------|
| Disconnect     | Applied fault between ground and T/R<br>VBH applied to Tip or Ring |          | 1<br>VBH/200K | 100      | $\mu$ A<br>A | 6    |
| Tip Open       | Ring Short to GND  | 20       | 35            | 46       | mA           |      |
| Standby        | Short Tip-to-VBH<br>Short Ring-to-GND                              | 24<br>26 | 38<br>35      | 47<br>44 |              |      |
| Active Ringing | ISLAC generating internal ringing                                  |          | 100           |          |              | 2    |

## Thermal Shutdown Fault Indications

| Fault            | Indication                                 |
|------------------|--|
| No Fault         | IMT operates normally ( $V_{REF} \pm 1$ V) |
| Thermal Shutdown | KG, IMT above 2.8 V; ILG operates normally |

### Note:

- These tests are performed with the following load impedances:  
Frequency < 12 kHz – Longitudinal impedance = 500  $\Omega$ ; metallic impedance = 300  $\Omega$   
Frequency > 12 kHz – Longitudinal impedance = 90  $\Omega$ ; metallic impedance = 135  $\Omega$
- Not tested or partially tested in production. This parameter is guaranteed by characterization or correlation to other tests.
- This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.
- When the Le79R241 device and ISLAC device is in the anti-sat operating region, this parameter is degraded. The exact degradation depends on system design.
- 55 dBm gain tracking level not tested in production. This parameter is guaranteed by characterization and correlation to other tests.
- This spec is valid from 0 V to VBL or –50 V, whichever is lower in magnitude.
- Other ringing-voltage characteristics are set by the ISLAC device.

## OPERATING MODES

The Le79R241 device receives multiplexed control data on the P1, P2 and P3 pins. The LD pin then controls the loading of P1, P2, and P3 values into the proper bits in the Le79R241 device control register. When the LD pin is less than 0.3 V below VREF (< ( $V_{REF} - 0.3$  V)), P1–P3 must contain data for relay control bits RD1, RD2 and RD3. These are latched into the first three bits in the Le79R241 device control register. When the LD pin is more than 0.3 V above VREF, P1–P3 must contain ISLIC control data C1, C2, and C3, which are latched into the last three bits of the Le79R241 device control register. Connecting the LD pin to VREF locks the contents of the Le79R241 device control register.

The operating mode of the Le79R241 device is determined by the C1, C2, and C3 bits in the control register of the Le79R241 device. Table 1 defines the Le79R241 device operating modes set by these signals.

Under normal operating conditions, the ISLIC device does not have active relays. The Le79R241 device to ISLAC device interface is designed to allow continuous real-time control of the relay drivers to avoid incorrect data loads to the relay bit latches of the Le79R241 devices.

To perform external ringing, the ISLAC device from the Intelligent Access voice family is set to external ringing mode (RMODE = 1), enables the ring relay, and puts the Le79R241 device in the Standby mode.

**Table 1. Operating Modes**

| C3 | C2 | C1 | Operating Mode                                   | Battery Voltage Selection    | Operating Mode   | Connection to RMGPI & RMGLI Resistors |
|----|----|----|--|------------------------------|--|---------------------------------------|
| 0  | 0  | 0  | Standby (See note 1)                             | High Battery (BATH) and BGND | (High ohmic feed): Loop supervision active, A and B amplifiers shut down | Open                                  |
| 0  | 0  | 1  | Tip Open (See note 1)                            | High Battery (BATH) and BGND | Tip Open: AD at High-Impedance, Channel A power amplifier shut down      | Open                                  |
| 0  | 1  | 0  | On-Hook Transmission, Fixed Longitudinal Voltage | High Battery (BATH) and BGND | Fixed longitudinal voltage of –28 V                                      | A and B Amplifier Output              |
| 0  | 1  | 1  | Disconnect                                       | Low Battery selection at VBL | AD and BD at High-Impedance, Channel A and B power amplifiers shut down  |                                       |
| 1  | 0  | 0  | RSVD   |                              | Active feed, normal or reverse polarity                                  |                                       |
| 1  | 0  | 1  | Active High Battery                              | High Battery (BATH) and BGND |  |                                       |
| 1  | 1  | 0  | Active Low Battery                               | Low Battery (BATL) and BGND  |  |                                       |
| 1  | 1  | 1  | Active Internal Ringing                          | High Battery (BATH) and BGND | Active internal ringing  |                                       |

**Note:**

1. In these modes, the ring lead (B-lead) output has a –50 V internal clamp to battery ground (BGND).

**Operating Mode Descriptions**

| Operating Mode   | Description   |
|--|---|
| Disconnect   | This mode disconnects both A and B output amplifiers from the AD and BD outputs. The A and B amplifiers are shut down and the Le79R241 device selects the low battery voltage at the VBL pin. In the Disconnect state, the currents on IMT and ILG represent the voltages on the SA and SB pins, respectively. These currents are scaled to produce voltages across RMTi and RLGi of $\frac{V_{SA}}{400}$ and $\frac{V_{SB}}{400}$ , respectively.  |
| Standby  | The power amplifiers are turned off. The AD output is driven by an internal 250 $\Omega$ (typical) resistor, which connects to ground. The BD output is driven by an internal 250 $\Omega$ (typical) resistor, which connects to the high battery (BATH) at the VBH pin, through a clamp circuit, which clamps to approximately –50 V with respect to BGND. For VBH values above –55 V, the open-circuit voltage, which appears at this output is $\sim VBH + 7$ V. If VBH is below –55 V, the voltage at this output is –50 V. The battery selection for the balance of the circuitry on the chip is VBL. Line supervision remains active. Current limiting is provided on each line to limit power dissipation under short-loop conditions as specified in “Current-Limit Behavior” on page 15. In external ringing, the standby ISLIC state is selected. |
| Tip Open   | In this mode, the AD (Tip) lead is opened and the BD (Ring) lead is connected to a clamp, which operates from the high battery on VBH pin and clamps to approximately –50 V with respect to BGND through a resistor of approximately 250 $\Omega$ (typical). The battery selection for the balance of the circuitry on the chip is VBL.   |
| Active High Battery                                    | In the Active High Battery mode, battery connections are connected as shown in Table 1. Both output amplifiers deliver the full power level determined by the programmed DC-feed conditions. Active High Battery mode is enabled during a call in applications when a long loop can be encountered.   |
| Active Low Battery                                     | Both output amplifiers deliver the full power level determined by the programmed DC-feed conditions. VBL, the low negative battery, is selected in the Active Low Battery mode. This is typically used during the voice part of a call.   |
| Active Internal Ringing                                | In the Internal Ringing mode, the Le79R241 device selects the battery connections as shown in Table 1. When using internal ringing, both the AD and BD output amplifiers deliver the ringing signal determined by the programmed ringing level.   |
| On-Hook Transmission (OHT), Fixed Longitudinal Voltage | In the On-Hook Transmission, Fixed Longitudinal Voltage mode, battery connections are as shown in Table 1. The longitudinal voltage is fixed at the voltage shown in Table 1 to allow compliance with safety specifications for some classes of products.   |



## Driver Descriptions

| Driver | Description  |
|--------|--|
| R1     | A logic 1 on RD1 turns the R1 driver on and operates a relay connected between the R1 pin and VCCD. R1 drives the ring relay when external ringing is selected.  |
| R2     | A logic 1 on the RD2 signal turns the R2 driver on and routes current from the R2 pin to the RYE pin. In the option where the RYE pin is connected to ground, the R2 pin can sink current from a relay connected to VCCD.<br>Another option is to connect the RYE pin to the BD (Ring) lead and connect a test load between R2 and the AD (Tip) lead. This technique avoids the use of a relay to connect a test load. However, it does not isolate the subscriber line from the line card. The test load must be connected to the Le79R241 device side of the protection resistor to avoid damage to the R2 driver. |
| R3     | A logic 1 on the RD3 signal turns the R3 driver on and routes current from the R3 pin to the RYE pin. In the option where the RYE pin is connected to ground, the R3 pin can sink current from a relay connected to VCCD.<br>Another option is to connect the RYE pin to the B (Ring) lead and connect a test load between R3 and the A (Tip) lead. This technique avoids the use of a relay to connect a test load. However, it does not isolate the subscriber line from the line card. The test load must be connected to the Le79R241 device side of the protection resistor to avoid damage to the R3 driver.   |

Control bits RD1, RD2, and RD3 do not affect the operating mode of the Le79R241 device. These signals usually perform the following functions.

## Thermal-Management Equations

Applies to all modes except Standby and Ringing, which have no thermal management.

| Equation   | Description  |
|--|--|
| $I_L < 5 \text{ mA}$<br>$P_{SLIC} = (S_{BAT} - I_L(R_L + 2R_{FUSE})) \cdot I_L + 0.3 \text{ W}$<br>$P_{RTMG} = 0$  | TMG resistor-current is limited to be $5 \text{ mA} < I_L$ . If $I_L < 5 \text{ mA}$ , no current flows in the TMG resistor and it all flows in the Am79241.   |
| $I_L > 5 \text{ mA}$<br>$RMGPi = RMGLi = R_{TMG}$<br>$P_{RTMG}$ : total power dissipation of RMGPi and RMGLi<br>$R_{TMG} = (S_{BAT} - I_L(R_L + 2R_{FUSE})) / (2(I_L - 5 \text{ mA}))$<br>$P_{SLIC} = I_L(S_{BAT} - I_L(R_L + 2R_{FUSE})) + 0.3 \text{ W} - P_{RTMG}$<br>$P_{RTMG} = (I_L - 5 \text{ mA})^2(2R_{TMG})$ | These equations are valid when<br>$R_{TMG} \cdot (I_L - 5 \text{ mA}) < (S_{BAT} - (R_F + R_L)I_L) / 2 - 2$<br>because the longitudinal voltage is one-half the battery voltage and the TMG switches require approximately 2 V.<br>To choose a power rating for RTMG:<br>$P_{RATING} > P_{RTMG} / 2$ |

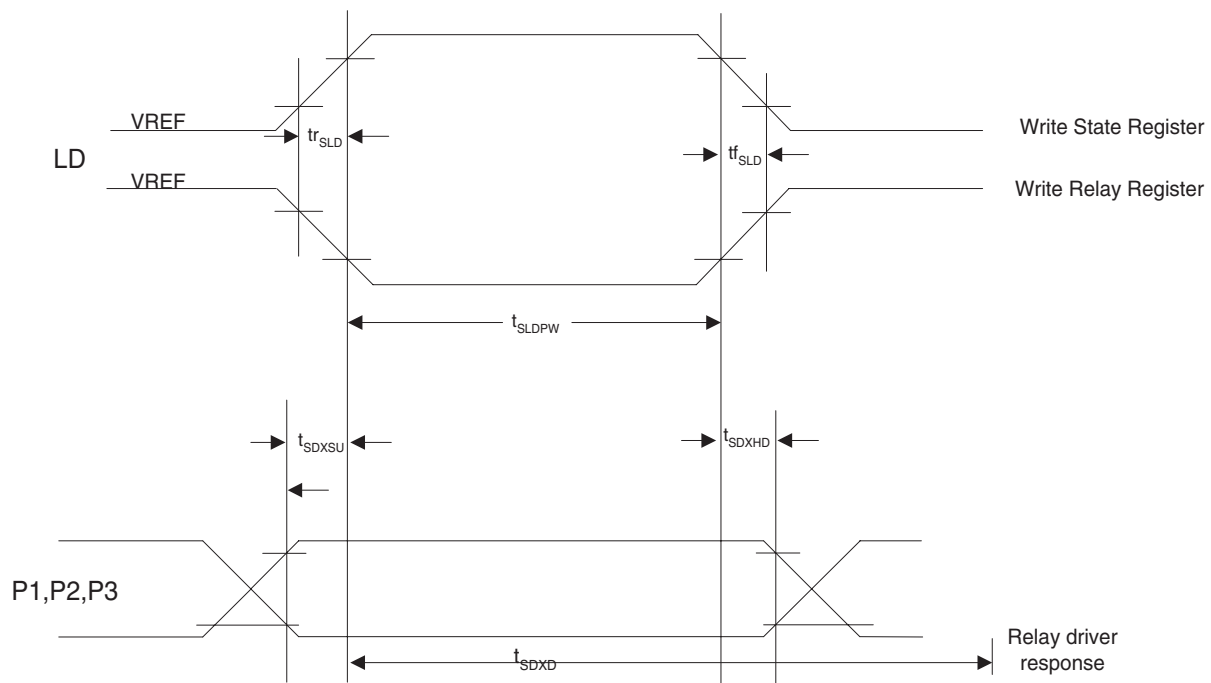
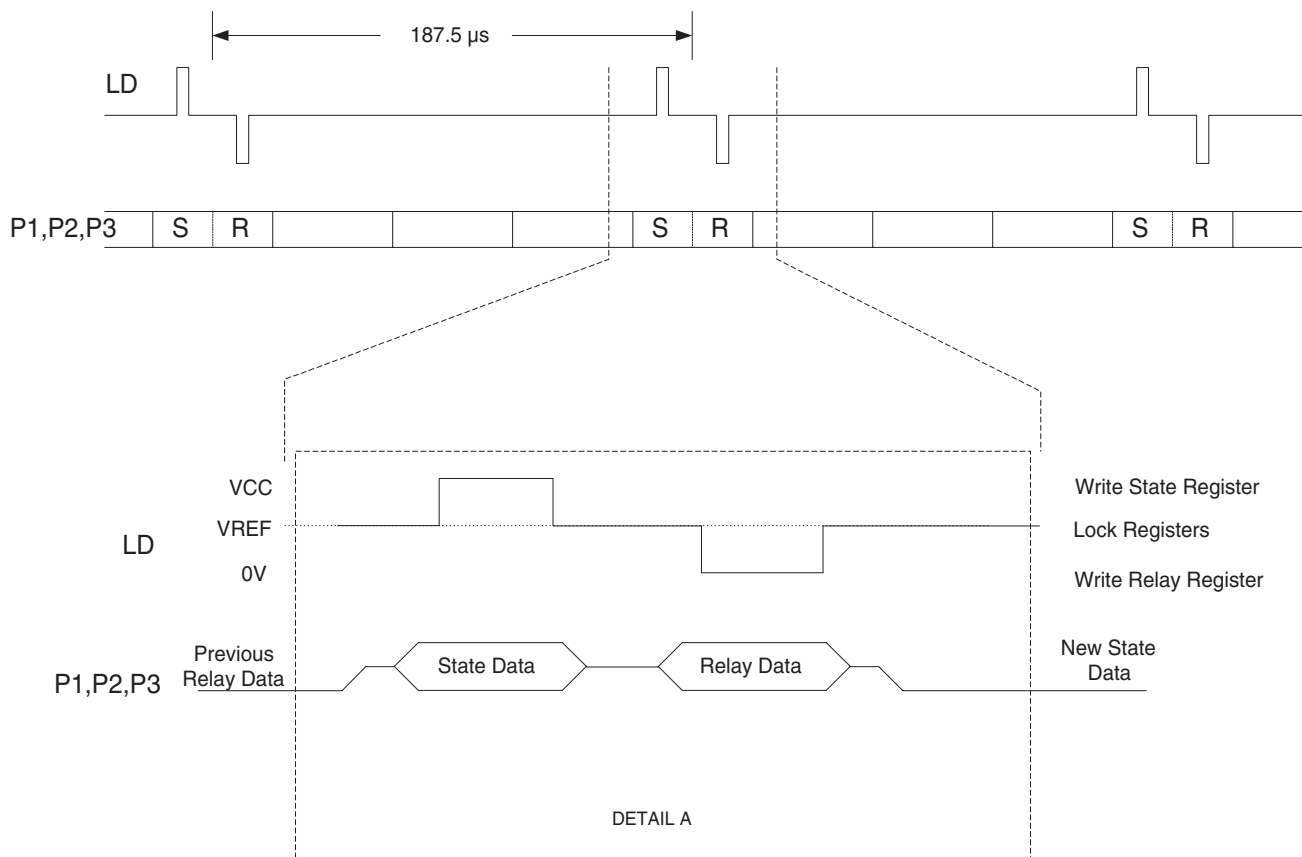
## TIMING SPECIFICATIONS

| Symbol | Signal   | Parameter                        | Min | Typ | Max | Unit |
|--------|----------|----------------------------------|-----|-----|-----|------|
| trSLD  | LD       | Rise time Le79R241 device LD pin |     |     | 2   | ms   |
| tfSLD  | LD       | Fall time Le79R241 device LD pin |     |     | 2   |      |
| tSLDPW | LD       | LD minimum pulse width           | 3   |     |     |      |
| tSDXSU | P1,P2,P3 | P1–3 data Setup time             | 4.5 |     |     |      |
| tSDXHD | P1,P2,P3 | P1–3 data hold time              | 4.5 |     |     |      |
| tSDXD  | P1,P2,P3 | Max P1–3 data delay              |     |     | 5   |      |

### Notes:

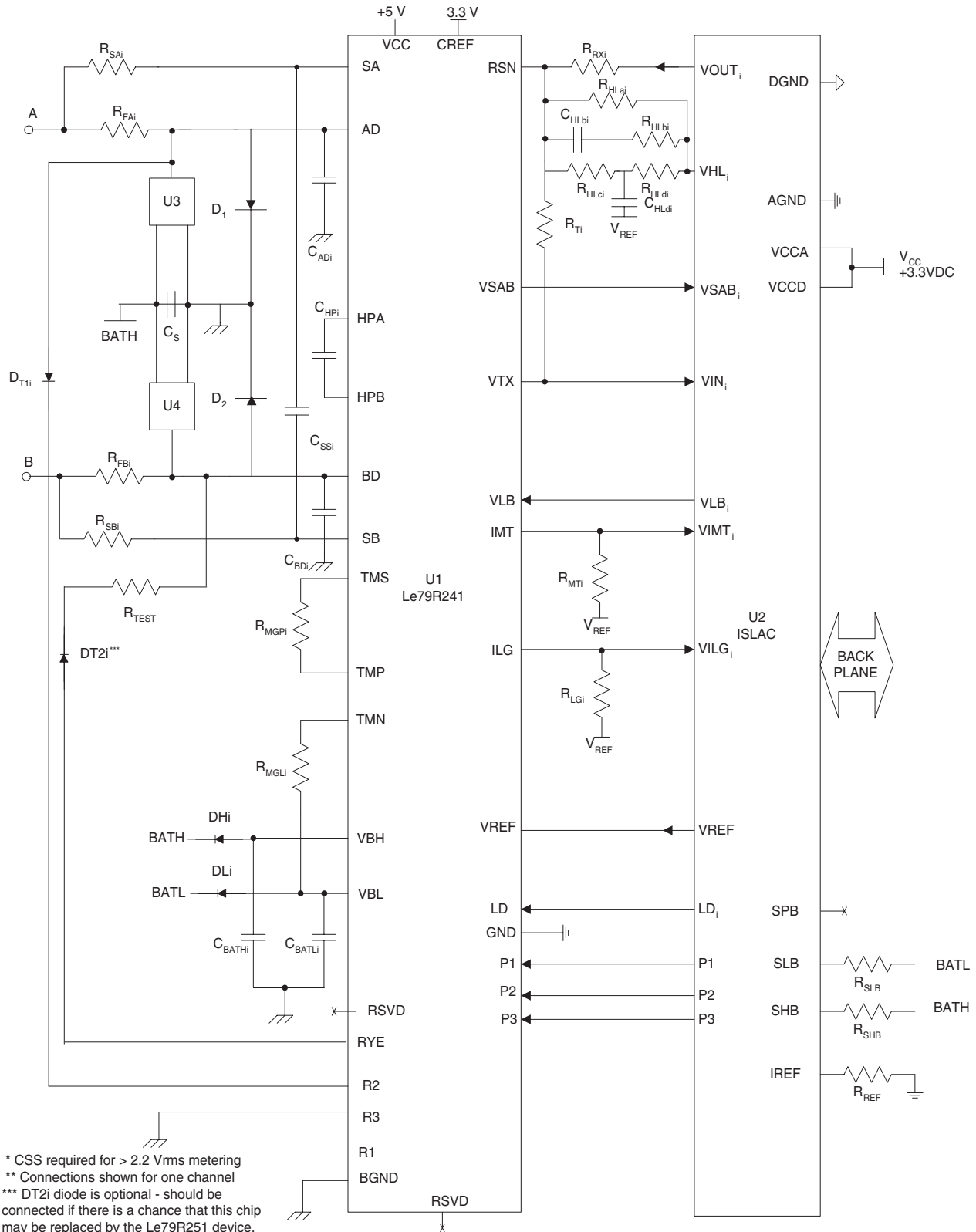
- The P1–3 pins are updated continuously during operation by the LD signal.
- After a power-on reset or hardware reset, the relay outputs from the Le79R241 device turn all relays off. An unassuming state is to place the relay control pins, which are level triggered, to a reset state for all relays. Any noise encountered only raises the levels toward the register lock state.
- When writing to the ISLIC registers, the sequence is:
  - Set LD pin to mid-state.
  - Place appropriate data on the P1–3 pins.
  - Assert the LD pin to High or Low to write the proper data.
  - Return LD pin to mid-state.
- Le79R241 device registers are refreshed at 5.33 kHz when used with an ISLAC device.
- If the clock or MPI becomes disabled, the LD pins and P1–3 returns to 0 V state, protecting the Le79R241 device and the line connection.
- Not tested in production. Guaranteed by characterization.

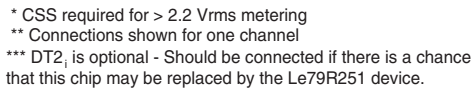
## WAVEFORMS



## APPLICATION CIRCUITS

### Internal Ringing Line card Schematic





## LINE CARD PARTS LIST

The following list defines the parts and part values required to meet target specification limits for channel i of the line card (i = 1, 2, 3, 4).

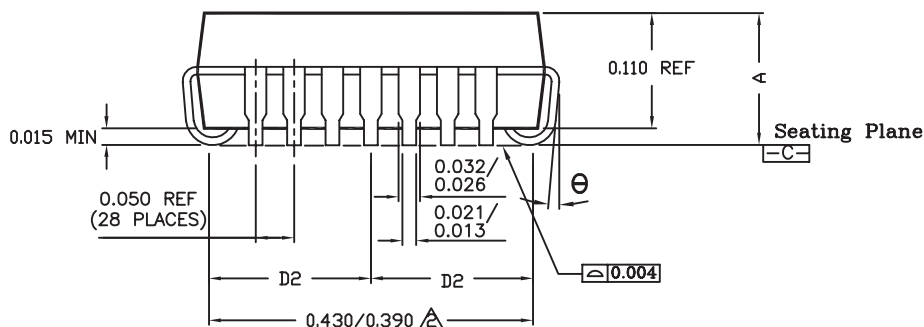
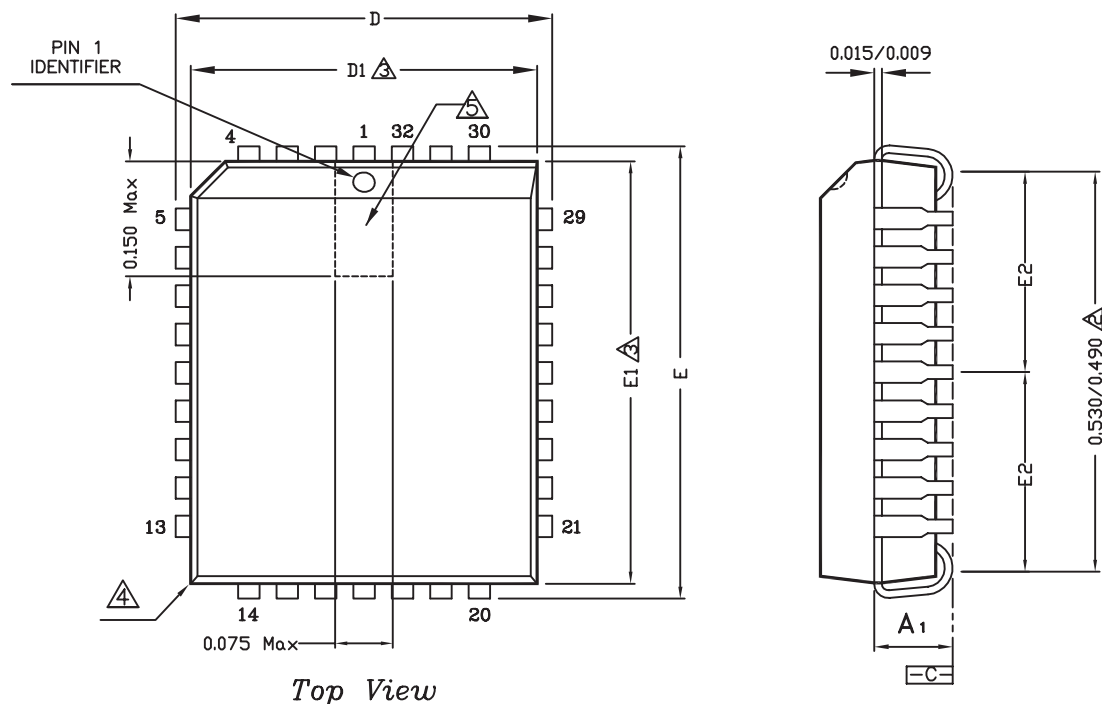
| Item                                   | Type            | Value           | Tol | Rating | Comments  | Note |
|--|-----------------|-----------------|-----|--------|---|------|
| U1                                     | Le79R241 device |                 |     |        | ISLIC device  |      |
| U2                                     | Le79Q224x       |                 |     |        | ISLAC device  |      |
| U3, U4                                 | B1100CC         |                 |     | 100 V  | TECCOR Battrax protector  |      |
| U5                                     | TISP61089A      |                 |     |        | Transient Voltage Suppressor, Power Innovations   |      |
| D1, D2                                 | Diode           | 1 A             |     | 100 V  |   |      |
| DHi, DLi, DT1i, DT2i (See note 4)      | Diode           | 100 mA          |     | 100 V  | 50 ns   |      |
| RFAi, RFBi                             | Resistor        | 50 $\Omega$     | 2%  | 2 W    | Fusible PTC protection resistors  |      |
| RSAi, RSBi                             | Resistor        | 200 k $\Omega$  | 2%  | 1/4 W  | Sense resistors   |      |
| RTi                                    | Resistor        | 80.6 k $\Omega$ | 1%  | 1/10 W |   |      |
| RRXi                                   | Resistor        | 100 k $\Omega$  | 1%  | 1/10 W |   |      |
| RREF                                   | Resistor        | 69.8 k $\Omega$ | 1%  | 1/10 W | Current reference   |      |
| RMGLi, RMGPi                           | Resistor        | 1 k $\Omega$    | 5%  | 1 W    | Thermal management resistors  |      |
| RSHB, RSLB                             | Resistor        | 750 k $\Omega$  | 1%  | 1/8 W  |   |      |
| RHLai                                  | Resistor        | 40.2 k $\Omega$ | 1%  | 1/10 W |   |      |
| RHLbi                                  | Resistor        | 4.32 k $\Omega$ | 1%  | 1/10 W |   |      |
| RHLci                                  | Resistor        | 2.87 k $\Omega$ | 1%  | 1/10 W |   |      |
| RHLdi                                  | Resistor        | 2.87 k $\Omega$ | 1%  | 1/10 W |   |      |
| CHLbi                                  | Capacitor       | 3.3 nF          | 10% | 10 V   | Not Polarized   |      |
| CHLdi                                  | Capacitor       | 0.82 mF         | 10% | 10 V   | Ceramic   |      |
| RMTi                                   | Resistor        | 3.01 k $\Omega$ | 1%  | 1/8 W  |   |      |
| RLGi                                   | Resistor        | 6.04 k $\Omega$ | 1%  | 1/8 W  |   |      |
| RTEST                                  | Resistor        | 2 k $\Omega$    | 1%  | 1 W    | Test board  |      |
| CADi, CBDi (See note 1)                | Capacitor       | 22 nF           | 10% | 100 V  | Ceramic, not voltage sensitive  |      |
| CBATHi, CBATLi                         | Capacitor       | 100 nF          | 20% | 100 V  | Ceramic   |      |
| CHPi                                   | Capacitor       | 22 nF           | 20% | 100 V  | Ceramic   |      |
| CSi                                    | Capacitor       | 100 nF          | 20% | 100 V  | Protector speed up capacitor  | 1    |
| CSSi                                   | Capacitor       | 56 pF           | 5%  | 100 V  | Ceramic   | 3    |
| <b>Components for External Ringing</b> |                 |                 |     |        |   |      |
| RGFDi                                  | Resistor        | 510 $\Omega$    | 2%  | 2 W    | 1.2 W typ   |      |
| RSRbi, RSRc                            | Resistor        | 750 k $\Omega$  | 2%  | 1/4 W  | Matched to within 0.2% for initial tolerance and 0 to 70° C ambient temperature range. <sup>2</sup> 17 mW typ | 2    |
| KRI                                    | Relay           | 5 V Coil        |     |        | DPDT  |      |

**Note:**






- Value can be adjusted to suit application.
- Can be looser for relaxed ring-trip requirements.
- Required for metering > 2.2 Vrms, otherwise may be omitted.
- DT2i is optional - Should be put if there is a chance that this chip may be replaced by Am79R251.

## PHYSICAL DIMENSIONS

## 32-Pin PLCC

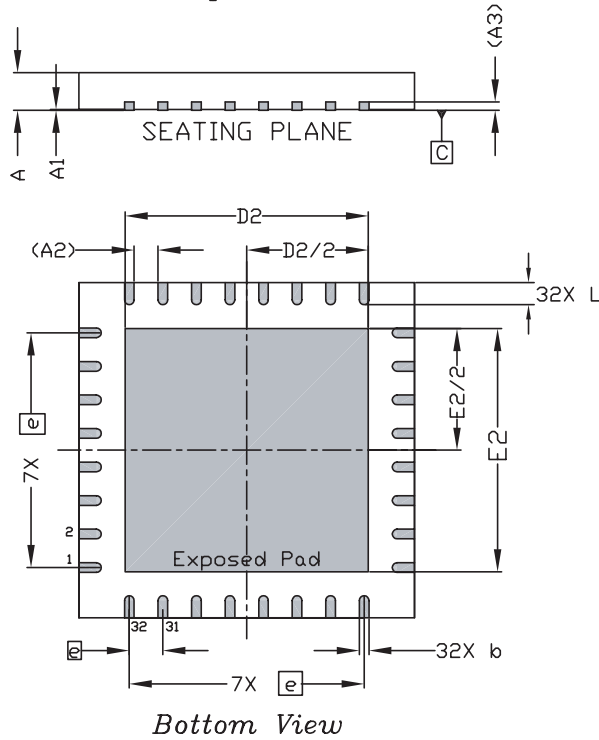
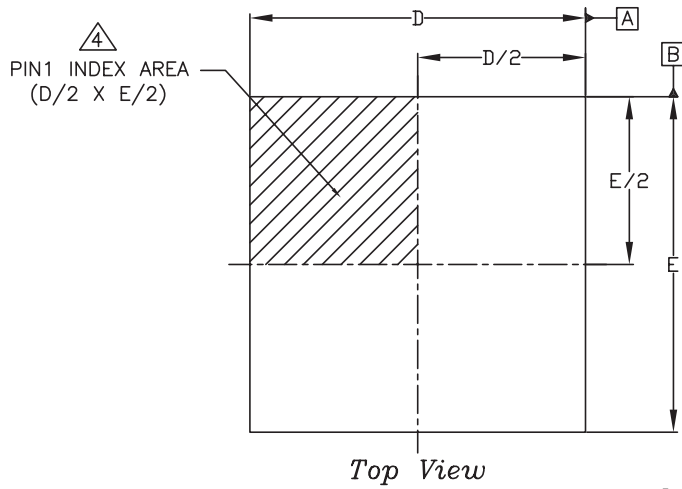


NOTE :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.  
 TO BE MEASURED AT SEATING PLANE  CONTACT POINT.  
 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.010 IN PER SIDE. DIMENSIONS D, AND E, INCLUDE MOLD MISMATCH AND DETERMINED AT THE PARTING LINE; THAT IS D1 AND E1 ARE MEASURED AT THE EXTREME MATERIAL CONDITION AT THE UPPER OR LOWER PARTING LINE.  
 EXACT SHAPE OF THIS FEATURE IS OPTIONAL.  
 DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
6. SUM OF DAM BAR PROTRUSIONS TO BE 0.007 MAX PER LEAD.
7. CONTROLLING DIMENSION : INCH.
8. REFERENCE DOCUMENT : JEDEC MS-016

| Symbol    | Dimension in inch |       |       |
|-----------|-------------------|-------|-------|
|           | Min               | Nom   | Max   |
| <b>A</b>  | 0.125             | —     | 0.140 |
| <b>A1</b> | 0.075             | 0.090 | 0.095 |
| <b>D</b>  | 0.485             | 0.490 | 0.495 |
| <b>D1</b> | 0.447             | 0.450 | 0.453 |
| <b>D2</b> | 0.205 REF         |       |       |
| <b>E</b>  | 0.585             | 0.590 | 0.595 |
| <b>E1</b> | 0.547             | 0.550 | 0.553 |
| <b>E2</b> | 0.255 REF         |       |       |
| <b>θ</b>  | 0°                | —     | 10°   |

## 32-Pin QFN



| Symbol | Dimension in mm |      |      |
|--------|-----------------|------|------|
|        | Min             | Nom  | Max  |
| A      | 0.80            | 0.90 | 1.00 |
| A2     | 0.57 REF        |      |      |
| b      | 0.18            | 0.23 | 0.28 |
| D      | 8.00 BSC        |      |      |
| D2     | 5.70            | 5.80 | 5.90 |
| E      | 8.00 BSC        |      |      |
| E2     | 5.70            | 5.80 | 5.90 |
| e      | 0.80 BSC        |      |      |
| L      | 0.43            | 0.53 | 0.63 |
| N      | 32              |      |      |
| A1     | 0.00            | 0.02 | 0.05 |
| A3     | 0.20 REF        |      |      |

### NOTES :

- DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS,  $\theta$  IS IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEP 95-1 SSP-012. DETAILS OF THE TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- COPLANARITY APPLIES TO EXPOSED PAD AS WELL AS THE TERMINALS.
- REFERENCE DOCUMENT : JEDEC MO-220

## REVISION SUMMARY

### Revision H to Revision I

- Page 11, Figure 3, DT1i was added and the last note was modified.
- Page 12, Figure 4, DT1i was added and the last note was modified.
- Page 15, Electrical Characteristics, Numbers changed in the Max column.
- Page 16, Absolute Maximum Ratings, The "Humidity" row was deleted.
- Page 17, Specifications, There were changes to rows one, four, six, 12, and 17–21, and to the Note column.
- Page 18, Relay Driver Specifications, There were changes in the last two rows.
- Page 19, Transmission Specifications, There were changes to rows, six, eight, 10, and 13, and to the Note column.
- Page 20, Fault Indications, "ILG operates normally" was deleted from the Indication column on the second row.

### Revision I to Revision J

- Applied new format.
- Global change: RTMG1 to RMGLi, and RTMG2 to RMGPi.
- Updated "Target Specifications" for rows 10, and 19.
- Updated "Transmission Specifications" for row 12.
- "Thermal Management Equations" modified.
- Added "Applications" section.

### Revision J to K

- Added 5 REN bullet to Features.
- Updated Device Internal Block Diagram.
- Modified description of LD pin.
- In "Thermal Resistance" section, updated temperature to 43° C.
- New Temperature statement added to "Chipset Features".
- New Temperature statement added to "Environmental Ranges".
- Removed reference to  $V_{LOOPMAX}$  in the "Electrical Ranges" section.
- "Waveforms," new image.
- In "DC Specificaitons" section, the following changes were made:
  - Added test conditions for two-wire loop voltage.
  - Added a typical value for Ternary input voltage, Mid boundary.
  - Removed references to  $T_A$  under test conditions for idle channel noise.
- "DC Specifications," "Transmission Specifications," and "Line Card Parts List," corrected W's to omega's.
- Added typical value for Ringing Specifications.
- Renamed "Fault Indications" table to "Thermal Shutdown Fault Indications"; modified text.
- Modified text in "Operating Modes" section.
- "Thermal-Management Equations," corrected " $P_{TMG}$ " to " $PT_{RTMG}$ " and corrected " $(R_{LL})$ " to " $(R_F + R_L)_{LL}$ ".
- "Application Circuits," added line to arrow head at DT1i, and deleted "H" from R2 and R3.
- Modified note for External Ringing Line card schematic.

### Revision K to L

- Added QFN package data to "Connection Diagram," "Absolute Maximum Ratings," and "Physical Dimensions."
- Updated "Am" OPNs (Ordering Part Numbers) to "Le" throughout document
- In "Ordering Information" the following changes were made:
  - Added entries for Le79R241JC and Le79R241QC
  - Removed the chip graphic
  - Added notes
- In "Features," added bullet for space savings feature
- Removed references to DISLAC documents in "Related Literature"
- In "Pin Descriptions," added row describing exposed pad
- Standardized notes in "Absolute Maximum Ratings" section



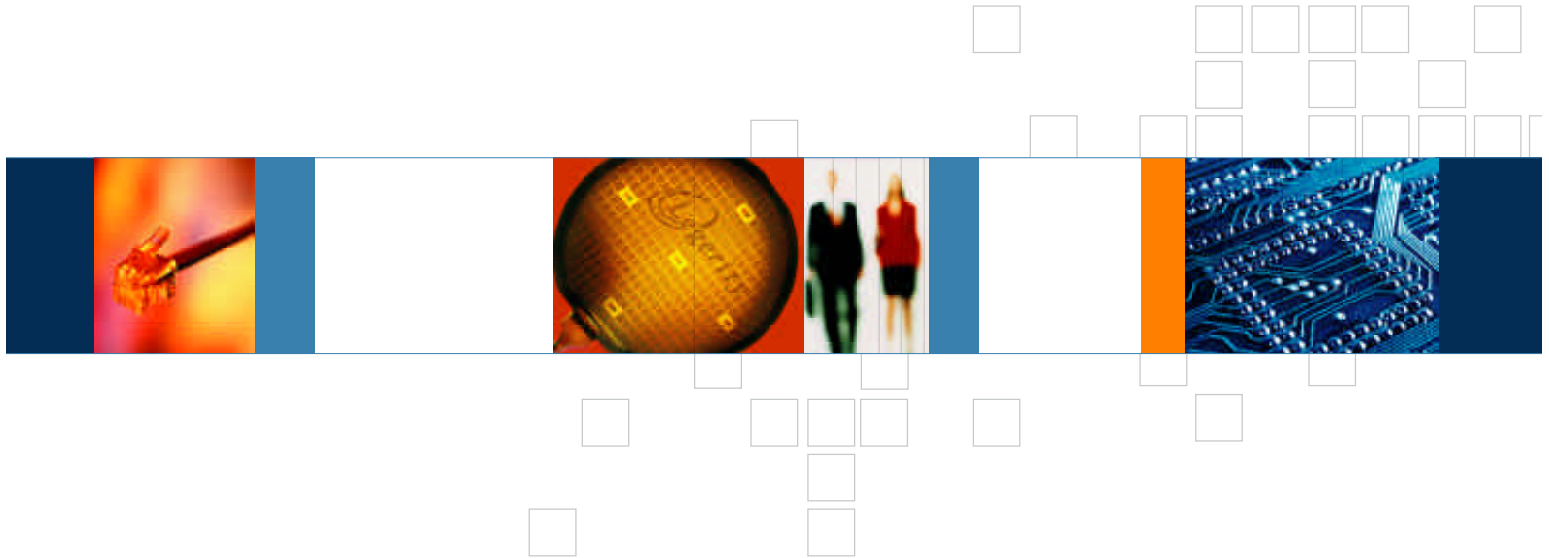
- In "Thermal Management Equations",  $I_L > 5 \text{ mA}$ , deleted the last sentence in the Description section
- Updated 32-Pin PLCC physical dimensions graphic

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