ISLIC™

Intelligent Subscriber Line Interface Circuit
Am79231*/Le79231 Device

APPLICATIONS

- **Enables a cost effective voice solution for long or short loop applications providing POTS and integrated test capabilities**
  - — CO
  - — DLC
  - — PBX/KTS
  - — Pair Gain

FEATURES

- **Monitor of two-wire interface voltages and currents supports**
  - — Voice transmission
  - — Programmable DC feed characteristics
    - – Independent of battery
    - – Current limited
  - — Selectable off-hook and ground-key thresholds
  - — Subscriber line diagnostics
    - – Leakage resistance
    - – Loop resistance
    - – Line capacitance
    - – Bell capacitance
    - – Foreign voltage sensing
  - — Power cross and fault detection
- **Ring relay driver for external ringing**
- **+5 V and battery supplies**
- **Dual battery operation for system power saving**
  - — Automatic battery switching
  - — Intelligent thermal management
- **Compatible with inexpensive protection networks**
  - — Accommodates low tolerance fuse resistors or PTC thermistors
- **Metering capable**
  - — 12 kHz and 16 kHz
  - — Smooth polarity reversal
- **Tip-open state supports ground start signaling**
- **Integrated test load switches/relay drivers**
- **Space Saving Package Options (8x8 QFN)**

RELATED LITERATURE

- **080250 Le79Q2241/2242/2243 QISLAC Data Sheet**
- **080262 Intelligent Access™ Voice Solutions Evaluation Board User's Guide**
- **080344 Le79R2xx/Le79Q224x ISLIC™/Quad ISLAC™ Technical Reference**

ORDERING INFORMATION

An ISLAC device must be used with this part

Device	Package
Am79231JC*	32-pin PLCC
Le79231JC	32-pin PLCC
Le79231QC**	32-pin QFN

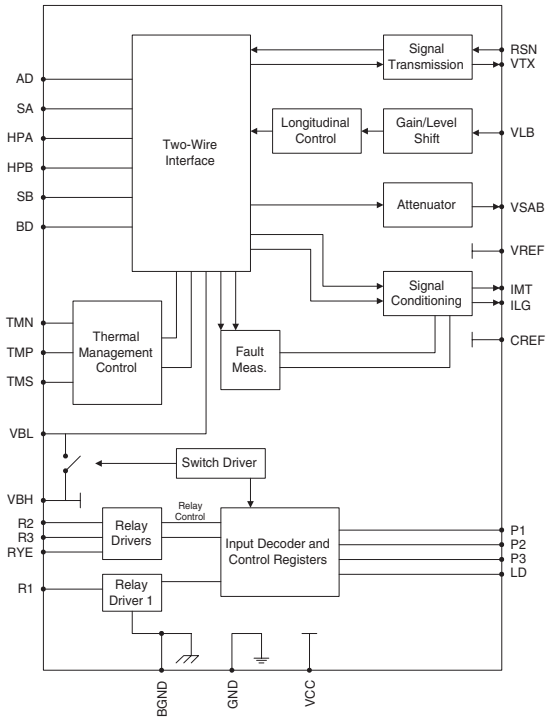
**This product can be ordered using ordering part numbers Am79231 or Le79231. The Am79231 ordering part number will be discontinued after 6/30/02, at which time the product will only be available using the Le79231 ordering part number.*

***Due to size constraints, QFN devices are marked by omitting the "Le" prefix. For example, Le79231QC is marked 79231QC.*

DESCRIPTION

The Le79231 device, in combination with an ISLAC™ device, implements the telephone line interface function. This enables the design of a low cost, high performance, fully software programmable line interface for multiple country applications worldwide. All AC, DC, and signaling parameters are fully programmable via microprocessor or GCI interfaces on the ISLAC device. Additionally, the Le79231 device has integrated self-test and line-test capabilities to resolve faults to the line or line circuit. The integrated test capability is crucial for remote applications where dedicated test hardware is not cost effective.

BLOCK DIAGRAM



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PRODUCT DESCRIPTION

The Intelligent Access™ voice chip sets integrate all the functions of the subscriber line. Two chip types are used to implement the line card — an Le79231 device and the Le79Q2241/2242/2243 ISLAC device. These provide the following basic functions:

1. The Le79231 device: A high voltage, bipolar device that drives the subscriber line, maintains longitudinal balance and senses line conditions.
2. The Le79Q2241/2242/2243 ISLAC device: A low voltage CMOS IC that provides conversion, control and DSP functions for the Le79231 device.

A complete schematic of the line card using the Intelligent Access voice chip sets for external ringing is shown in the “Application Circuit” on page 19.

The Le79231 device uses reliable, bipolar technology to provide the power necessary to drive a wide variety of subscriber lines. It can be programmed by the ISLAC device to operate in eight different modes that control power consumption and signaling. This enables it to have full control over the subscriber loop. The Le79231 device is designed to be used exclusively with the ISLAC devices. The Le79231 device requires only +5 V power and the battery supplies for its operation.

The Le79231 device implements a linear loop-current feeding method with the enhancement of intelligent thermal management. This limits the amount of power dissipated on the Le79231 device by dissipating power in external resistors in a controlled manner.

Each ISLAC device contains high-performance circuits that provide A/D and D/A conversion for the voice (codec), DC-feed and supervision signals. The ISLAC device contains a DSP core that handles signaling, DC-feed, supervision and line diagnostics for all channels.

The DSP core selectively interfaces with three types of backplanes:

- Standard PCM/MPI
- Standard GCI
- Modified GCI with a single analog line per GCI channel

The Intelligent Access voice chip set provides a complete software configurable solution to the BORSCHT functions as well as complete programmable control over subscriber line DC-feed characteristics, such as current limit and feed resistance. In addition, these chip sets provide system level solutions for the loop supervisory functions and metering. In total, they provide a programmable solution that can satisfy worldwide line card requirements by software configuration.

Software programmed filter coefficients, DC-feed data and supervision data are easily calculated with the WinSLAC™ software. This PC software is provided free of charge. It allows the designer to enter a description of system requirements. WinSLAC then computes the necessary coefficients and plots the predicted system results.

The Le79231 device interface unit inside the ISLAC device processes information regarding the line voltages, loop currents and battery voltage levels. These inputs allow the ISLAC device to place several key Le79231 device performance parameters under software control.

The main functions that can be observed and/or controlled through the ISLAC backplane interface are:

- DC-feed characteristics
- Ground-key detection
- Off-hook detection
- Metering signal
- Longitudinal operating point
- Subscriber line voltage and currents
- Ring-trip detection
- Abrupt and smooth battery reversal
- Subscriber line matching
- Ringing
- Sophisticated line and circuit tests

To accomplish these functions, the ISLIC device collects the following information and feeds it, in analog form, to the ISLAC device:

- The metallic (IMT) and longitudinal (ILG) loop currents
- The AC (VTX) and DC (VSAB) loop voltage

The outputs supplied by the ISLAC device to the ISLIC device are then:

- A voltage (VHL_i*) that provides control for the following high-level ISLIC device outputs:
  - DC loop current

  - 12 or 16 kHz metering signal
- A low-level voltage proportional to the voice signal ($VOUT_i$)
- A voltage that controls longitudinal offset for test purposes (VLB_i)

The ISLAC device performs the codec and filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters set the receive and transmit gain, perform the transhybrid balancing function, permit adjustment of the two-wire termination impedance and provide frequency attenuation adjustment (equalization) of the receive and transmit paths. Adaptive transhybrid balancing is also included. All programmable digital filter coefficients can be calculated using WinSLAC software. The PCM codes can be either 16-bit linear two's-complement or 8-bit companded A-law or µ-law.

Besides the codec functions, the Intelligent Access voice chip set provides all the sensing, feedback, and clocking necessary to completely control ISLIC device functions with programmable parameters. System-level parameters under programmable control include active loop current limits, feed resistance, and feed mode voltages.

The ISLAC device supplies complete mode control to the ISLIC device using the control bus (P1-P3) and tri-level load signal (LD_i).

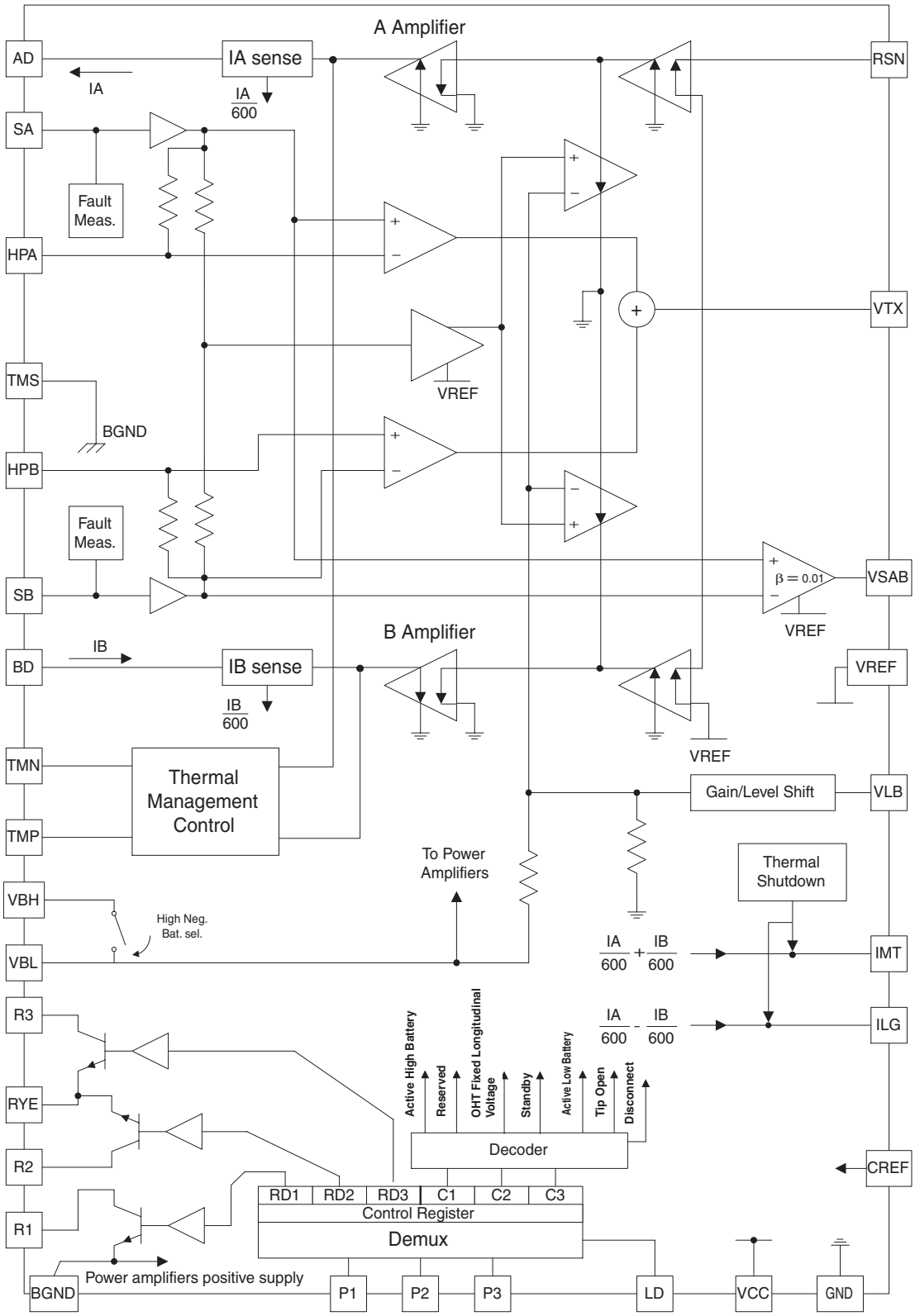
The Intelligent Access voice chip set provides extensive loop supervision capability including off-hook, ring-trip and ground-key detection. Detection thresholds for these functions are programmable. A programmable debounce timer is available that eliminates false detection due to contact bounce.

For subscriber line diagnostics, AC and DC line conditions can be monitored using built-in test tools. Measured parameters can be compared to programmed threshold levels to set a pass/fail bit. The user can choose to send the measurement data directly to a higher level processor by way of the PCM voice channel. Both longitudinal and metallic resistance and capacitance can be measured, which allows leakage resistance, line capacitance, and telephones to be identified.

Note:

i = channel number

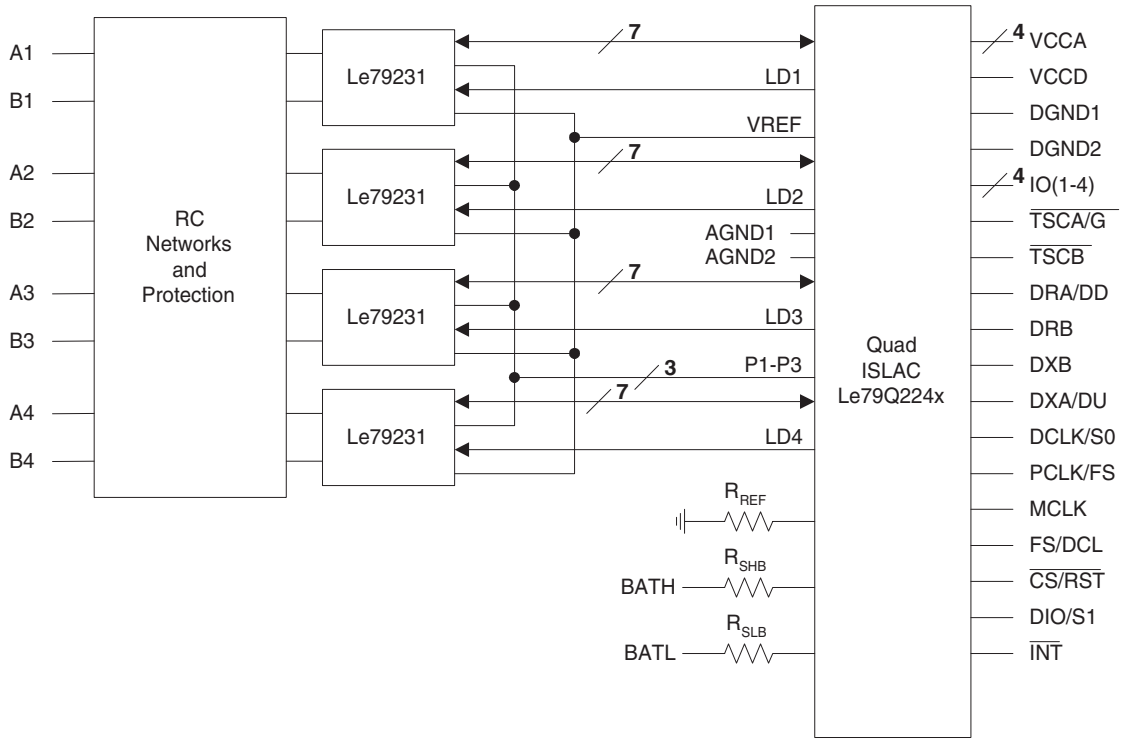
LE79231 DEVICE INTERNAL BLOCK DIAGRAM



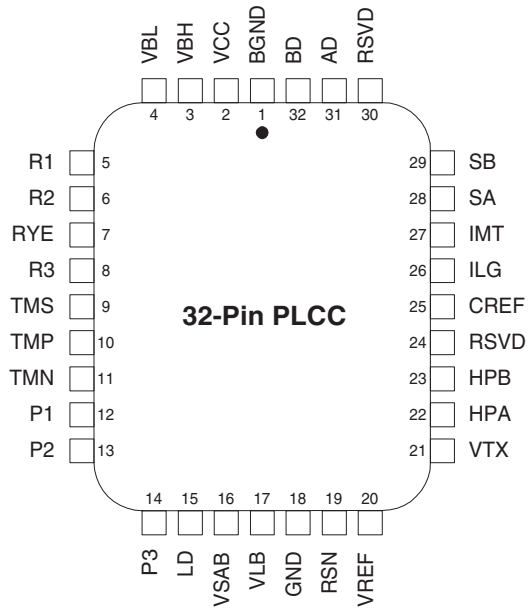
FEATURES OF THE INTELLIGENT ACCESS™ VOICE CHIP SET

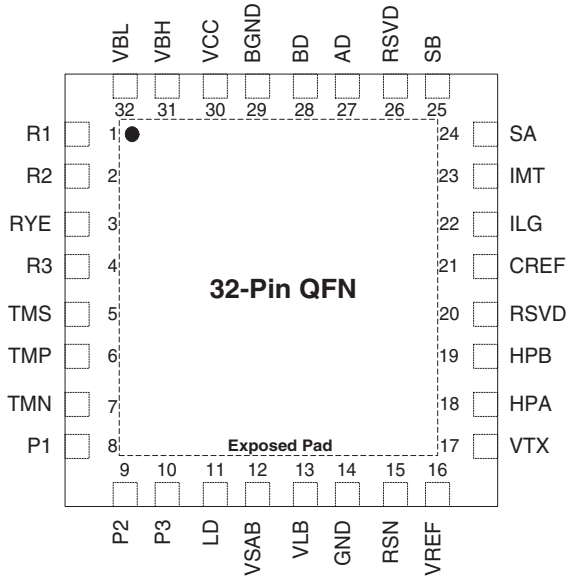
- Performs all battery feed, overvoltage, ring-trip, signaling, coding, hybrid and test (BORSCHT) functions
- Two chip solution supports high density, multi-channel architecture
- Single hardware design meets multiple country requirements through software programming of:
  - DC loop-feed characteristics and current-limit
  - Loop-supervision detection thresholds
    - Off-hook debounce circuit
    - Ground-key and ring-trip filters
  - Off-hook detect de-bounce interval
  - Two-wire AC impedance
  - Transhybrid balance
  - Transmit and receive gains
  - Equalization
  - Digital I/O pins
  - A-law/μ-law and linear selection
- Supports external battery-backed ringing
  - Unbalanced ringing
  - Ring relay driver
  - Ring relay operation synchronized to zero crossings of ringing voltage and current
  - Integrated ring-trip filter and software enabled manual or automatic ring-trip mode
- Supports metering generation with envelope shaping
- Smooth or abrupt polarity reversal
- Adaptive transhybrid balance
  - Continuous or adapt and freeze
- Supports both loop-start and ground-start signaling
- Exceeds LSSGR and CCITT central office requirements
- Selectable PCM or GCI interface
  - Supports most available master clock frequencies from 512 kHz to 8.192 MHz
- On-hook transmission
- Power/service denial mode
- Line-feed characteristics independent of battery voltage
- Only 5 V, 3.3 V and battery supplies needed
- Low idle-power per line
- Linear power-feed with intelligent power-management feature
- Compatible with inexpensive protection networks; Accommodates low-tolerance fuse resistors while maintaining longitudinal balance
- Monitors two-wire interface voltages and currents for subscriber line diagnostics
- Built-in voice-path test modes
- Power-cross, fault, and foreign voltage detection
- Integrated line-test features
  - Leakage
  - Line and ringer capacitance
  - Loop resistance
- Integrated self-test features
  - Echo gain, distortion, and noise
- Guaranteed performance over commercial and industrial temperature ranges.
- Up to three relay drivers per ISLIC™ device
  - Configurable as test load switches

CHIP SET BLOCK DIAGRAM - FOUR CHANNEL LINE CARD EXAMPLE



CONNECTION DIAGRAMS





Notes:

1. *Pin 1 is marked for orientation.*
2. *RSVD = Reserved. Do not connect to this pin.*
3. *The thermally enhanced QFN package features an exposed pad on the underside which must be electrically tied to VBH.*

PIN DESCRIPTIONS

Pin Name	Type	Description
AD, BD	Output	Provide the currents to the A and B leads of the subscriber loop.
BGND	Ground	Ground return for high and low battery supplies.
CREF	+3.3 VDC	VCCD reference. It is the digital high logic supply rail, used by the ISLIC to ISLAC interface.
GND	Ground	Analog and digital ground return for VCC.
HPA, HPB	Output	These pins connect to CHP, the external high-pass filter capacitor that separates the DC loop-voltage from the voice transmission path.
ILG	Output	ILG is proportional to the common-mode line current (IAD–IBD), except in disconnect mode, where ILG is proportional to the current into grounded SB.
IMT	Output	IMT is proportional to the differential line current (IAD + IBD), except in disconnect mode, where IMT is proportional to the current into grounded SA. The Le79231 device indicates thermal overload by pulling IMT to CREF.
LD	Input	The LD pin controls the input latch and responds to a 3-level input. When the LD pin is a logic 1 (C_{REF} – 1), the logic levels on P1–P3 latch into the Le79231 device control register bits that operate the mode-decoder. When the LD pin is a logic 0 (< 0.6), the logic levels on P1–P3 latch into the Le79231 device control register bits that control the relay drivers (RD1–RD3). When the LD pin level is at ~V_{REF} ± 0.3 V, the control register contents are locked.
P1–P3	Input	Inputs to the latch for the operating-mode decoder and the relay-drivers.
R1	Output	Collector connection for ring relay driver. Emitter internally connected to BGND.
R2	Output	Collector connection for relay 2 driver. Emitter internally connected to RYE
R3	Output	Collector connection for relay 3 driver. Emitter internally connected to RYE.
RSN	Input	The metallic current between AD and BD is equal to 500 times the current into this pin. Networks that program receive gain and two-wire impedance connect to this node. This input is at a virtual potential of VREF.
RSVD	Reserved	These pins are used during Legerity testing. In the application, these pins must be left floating.
RYE	Output	Emitter connection for R2 and R3. Normally connected to relay ground.
SA, SB	Input	Sense the voltages on the line side of the fuse resistors at the A and B leads. External sense resistors, RSA and RSB, protect these pins from lightning or power-cross.
TMP, TMN, TMS	Output	External resistors connected from TMP to TMS and TMN to VBL to offload excess power from the Le79231 device.
VBH	Battery (Power)	Connection to high-battery supply used for ringing and long loops. Connects to the substrate. When only a single battery is available, it connects to both VBH and VBL.
VBL	Battery (Power)	Connection to low-battery supply used for short loops. When only a single battery is available, this pin can be connected to VBH.
VCC	Power	+5 V Power Supply supply for low voltage analog and digital circuits in the Le79231 device.
VLB	Input	Sets the DC longitudinal voltage of the Le79231 device. It is the reference for the longitudinal control loop. When the VLB pin is greater than V_{REF}, the Le79231 device sets the longitudinal voltage to a voltage approximately half-way between the positive and negative power supply battery rails. When the VLB pin is driven to levels between 0 V and V_{REF}, the longitudinal voltage decreases linearly with the voltage on the VLB pin.
VREF	Input	The ISLAC chip provides this voltage which is used by the Le79231 device for internal reference purposes. All analog input and output signals interfacing to the ISLAC chip are referenced to this pin.
VSAB	Output	Scaled-down version of the voltage between the sense points SA and SB on this pin.
VTX	Output	The voltage between this pin and V_{REF} is a scaled down version of the AC component of the voltage sensed between the SA and SB pins. One end of the two-wire input impedance programming network connects to VTX. The voltage at VTX swings positive and negative with respect to V_{REF}.
Exposed Pad	Battery	This must be electrically tied to VBH.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Storage temperature	–55° to +150° C
Ambient temperature, under bias	–40° to +85° C
Humidity	5% to 95%
VCC with respect to GND	–0.4 to +7 V
VBH, VBL with respect to GND (see note 2)	+0.4 to –70 V
BGND with respect to GND	–3 to +3 V
Voltage on relay outputs	+7 V
AD or BD to BGND: Continuous 10 ms (F = 0.1 Hz) 1 µs (F = 0.1 Hz) 250 ns (F = 0.1 Hz)	 VBH – 1 to BGND + 1 VBH – 5 to BGND + 5 VBH – 10 to BGND + 10 VBH – 15 to BGND + 15
Current into SA or SB: 10 µs rise to Ipeak 1000 µs fall to 0.5 Ipeak; 2000 µs fall to I =0	Ipeak = ±5 mA
Current into SA or SB: 2 µs rise to Ipeak 10 µs fall to 0.5 Ipeak; 20 µs fall to I = 0	Ipeak = ±12.5 mA
SA SB continuous	5 mA
Current through AD or BD	± 150 mA
P1, P2, P3, LD to GND	–0.4 to VCC + 0.4 V
Maximum power dissipation (see note 1) T_A = 70° C In 32-pin PLCC package In 32-pin QFN package T_A = 85° C In 32-pin PLCC package In 32-pin QFN package	 1.67 W 3.00 W 1.33 W 2.40 W
ESD Immunity (Human Body Model)	1.5 kV min

Notes:

1. *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165° C. Operation above 145° C junction temperature may degrade device reliability.*

   The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to a large internal copper plane.

2. *Rise time of VBH (dv/dt) must be limited to less than 27 v/µs.*

Thermal Resistance

The junction to air thermal resistance of the Le79231 device in a 32-pin PLCC package is 45° C/W and in a 32-pin QFN package is 25° C/W (measured under free air convection conditions and without external heat sinking).

Electrical Operating Ranges

Legerity guarantees the performance of this device over commercial (0° to 70° C) and industrial (–40° to 85° C) temperature ranges by conducting electrical characterization over each range, and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore TR-TSY-000357 Component Reliability Assurance Requirements for Telecommunications Equipment.

Environmental Ranges

Ambient Temperature	0 to 70° C Commercial
	–40 to +85 ° C extended temperature
Ambient Relative Humidity	15 to 85%

Electrical Ranges

VCC	5 V ± 5%
VBL	–15 V to VBH
VBH	–42.5 to –70 V
BGND with respect to GND	–100 to +100 mV
Load resistance on VTX to V_{REF}	20 kΩ minimum
Load resistance on VSAB to V_{REF}	20 kΩ minimum

SPECIFICATIONS

Power Dissipation

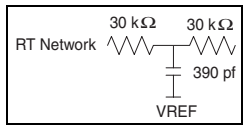
Loop resistance = 0 to ∞ unless otherwise noted (not including fuse resistors), 2 x 50 Ω fuse resistors, BATL = –36 V, BATH = –65 V, VCC = +5 V. For power dissipation measurements, DC-feed conditions are as follows:

- ILA (Active mode current limit) = 25 mA (IRSN = 50 µA)
- RFD (Feed resistance) = 500 Ω
- VAS (Anti-sat activate voltage) = 10 V
- VAPP (Apparent Battery Voltage) = 48 V
- RMGLi = RMGPi (Thermal management resistors) = 1 kΩ

Description	Test Conditions		Min	Typ	Max	Unit
Power Dissipation Normal Polarity	On-Hook Disconnect			50		mW
	On-Hook Standby			65		
	On-Hook Transmission Fixed Longitudinal Voltage	ISLIC		145		
	On-Hook Active High Battery	ISLIC		270		
	Off-Hook Active Low Battery RL = 294 Ω	ISLIC TMG		620 200		
Power Supply Currents	On-Hook Disconnect	VBH VBL VCC		0.4 0.1 3.1		mA
	On-Hook Standby	VBH VBL VCC		0.75 0 3.1		
	On-Hook Transmission Fixed Longitudinal Voltage	VBH VBL VCC		1.85 0 5		
	On-Hook Active High Battery	VBH VBL VCC		3.6 0 7.3		
	Off-Hook Active Low Battery RL = 294 Ω	VBH VBL VCC		0.7 26.9 7.5		

DC SPECIFICATIONS

Unless otherwise specified, test conditions are: VCC = 5 V, RMGPi = RMGLi = 1 kΩ, BATH = –65 V, BATL = –36 V, RRX = 150 kΩ, RL = 600 Ω, RSA = RSB = 200 kΩ, RFA = RFB = 50 Ω, CHP = 22 nF, CAD = CBD = 22 nF, IRSN = 50 mA. DC-feed conditions are normally set by the ISLAC device. When the Le79231 device is tested by itself, its operating conditions must be simulated as if it were connected to an ideal ISLAC device.

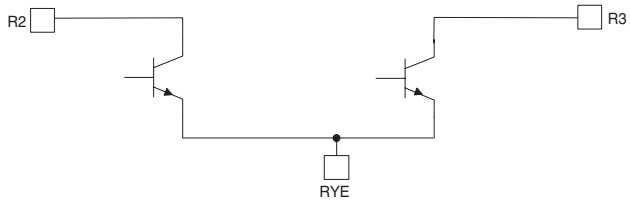


No.	Item	Condition	Min	Typ	Max	Unit	Note
1	Two-wire loop voltage (including offset)	Standby mode, open circuit, |VBH| < 55 V |VBH| > 55 V GND – VB Any Active mode (does not include OHT), RL = 600 Ω, I_{RSN} = 50 µA OHT mode, RL = 2200 Ω I_{RSN} = 20 µA	 VBH–8 48 13.88 8.64 19.8	 VBH–7 51 15 10.8 22	 VBH–6 55.5 55.5 16.13 12.96	V	2
2	Feed resistance per leg at pins AD & BD	Standby mode	130	250	375	Ω	
3	Feed current limit	Feed current Standby mode, RL = 600 Ω	18	34	45	mA	
	IMT current	Standby mode, RL = 2200 Ω	44.6	56		µA	
	ILG current	Standby mode A to VBH B to Ground	 28 28				
4	Ternary input voltage boundaries for LD pin. Mid-level input source must be V_{REF}.	Low boundary Mid boundary High boundary Input high current Input low current Mid-level current	 VREF–0.3 CREF–1	 V_{REF} 108 47 51	0.6 VREF+0.3	V V V µA µA µA	 2 2 2
5	Logic Inputs P1, P2, P3	Input high voltage Input low voltage Input high current Input low current	2.0 –20 –20	 0 0	 0.8 20 20	V V µA µA	
6	VTX output offset		–50	0	+50	mV	
7	VREF input current	VREF = 1.4 V		50		µA	2
8	CREF input current	CREF = 3.3 V	–3	0	3	mA	2
9	ß, DC Ratio of VSAB to loop voltage: $\beta = \frac{V_{SAB}}{V_{SA} - V_{SB}}$	Tj < 145° C, VSA – VSB = 22 V	0.0088	0.0097	0.0106	V/V	
10	Fault Indicator Threshold	Voltage Output on IMT	2.8	CREF - 0.3 V	CREF	V	2
11	Gain from VLB pin to A or B pin			30		V/V	
12	VLB pin input current	VLB = VREF ±1 V		0	100	µA	2
13	ILOOP/IMT	ILOOP = 10 mA	275	300	325	A/A	
14	ILONG/ILG	ILONG = 10 mA	560	600	640	A/A	
15	Input current, SA and SB pins	Active modes		1.0	3.0	µA	2
16	K1	Incremental DC current gain		500		A/A	2
17	ISA/IMT	Disconnect, ISA = 2 mA		6			
18	ISB/ILG	Disconnect, ISB = 2 mA		12			
19	VSAB output offset	–40° C +25° C +85° C		7.0 3.6 1.4		mV	
20	IMT output offset		-3	0	3	µA	
21	ILG output offset		-1	0	1	µA	

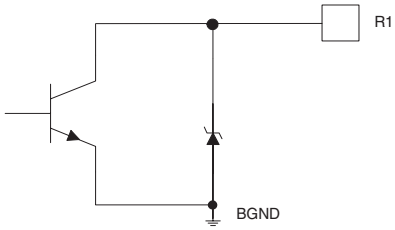
Relay Driver Specifications

Item	Condition	Min	Typ	Max	Unit	Note
On Voltage	25 mA/relay sink		0.4	0.5	V	2
	40 mA/ relay sink		0.8	1.0		
R2,R3 Off Leakage	R2,R3 = BGND RYE = VBH		0	100	µA	
Zener Break Over	Iz = 100 µA	6.6	7.9	10	V	
Zener On Voltage	Iz = 30 mA	6	11	17		

Figure 1. Relay Drivers



A. Relay Driver Configuration



B. Ring Relay

Transmission Specifications

No.	Item	Condition	Min	Typ	Max	Unit	Note
1	RSN input impedance	f = 300 to 3400 Hz		1		Ω	2
2	VTX output impedance			3			
3	Max, AC + DC loop current	Active High Battery or Active Low Battery	70			mA	2
4	Input impedance, A or B to GND	Active mode		70	135	Ω	
5	2-4 wire gain	–10 dBm, 1 kHz, 0 to 70° C T_A = –40° to 85° C	–14.13 –14.18	–13.98 –13.98	–13.83 –13.78	dB	2
6	2-4 wire gain variation with frequency	300 to 3400 Hz, relative to 1 kHz T_A=–40° to 85° C	–0.10 –0.15		+.10 +.15	dB	2
7	2-4 wire gain tracking	+3 dBm to –55 dBm Reference: –10 dBm T_A = –40 to 85° C	–0.10 –0.15		+0.10 +0.15	dB	2, 5
8	4-2 wire gain	–10 dBm, 1 kHz T_A= –40° to 85° C	–0.15 –0.20		+0.15 +0.20	dB	2
9	4-2 wire gain variation with frequency	300 to 3400 Hz, relative to 1 kHz	–0.1		+0.1	dB	
10	4-2 wire gain tracking	+3 dBm to –55 dBm Reference: –10 dBm T_A = –40 to 85° C	–0.1 –0.15		+0.1 +.15	dB	2, 5
11	Total harmonic distortion level 2-wire 4-wire 4-wire overload level at VTX	300 Hz to 3400 Hz 0 dBm 11.2 dBm –12 dBm –0.8 dBm RLOAD = 600 Ω		 ±1	 –50 –40 –48 –38	 dB dB dB dB Vp	2
12	Idle channel noise C-message Weighted Psophometric Weighted	Active modes, R_L = 600 Ω 2-wire 4-wire 2-wire 4-wire		 +9 –5 –81 –95	 +11 –79	 dBrnC dBmp —	
13	Longitudinal balance (IEEE method) Normal Polarity	L - T 200 to 1000 Hz T_A = –40° to 85° C 1000 to 3400 Hz T_A = –40° to 85° C	58 53 53 48			dB	
		T - L 200 to 3400 Hz	40				
		L - T, IL = 0 50 to 3400 Hz		63			3
	Reverse Polarity	L - T 200 to 1000 Hz T_A = –40° to 85° C	50 48				
14	PSRR (VBH, VBL)	50 to 3400 Hz 3.4 to 50 kHz	25	45 40			3, 4 1, 2, 4
15	PSRR (VCC)	50 to 3400 Hz 3.4 to 50 kHz	25	45 35			3, 4 1, 2, 4
16	Longitudinal AC current per wire	F = 15 to 60 Hz Active mode	20	30		mArms	2
17	Metering distortion	Freq = 12 kHz 2.8 Vrms Freq = 16 kHz metering load = 200 Ω	40			dB	2

Current-Limit Behavior

SLIC Mode	Condition	Min	Typ	Max	Unit	Note
Disconnect	Applied fault between ground and T/R VBH applied to Tip or Ring		1 VBH/200 kΩ	100	µA A	6
Tip Open	Ring Short to GND	20	35	46	mA	
Standby	Short Tip-to-VBH Short Ring-to-GND	24 26	38 35	47 44		

Thermal Shutdown Fault Indications

Fault	Indication
No Fault	IMT operates normally (V_{REF} ±1 V)
Thermal Shutdown	KG, IMT above 2.8 V; ILG operates normally

Note:

1. *These tests are performed with the following load impedances:*
   Frequency < 12 kHz – Longitudinal impedance = 500 Ω; metallic impedance = 300 Ω
   Frequency > 12 kHz – Longitudinal impedance = 90 Ω; metallic impedance = 135 Ω
2. *Not tested or partially tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
3. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
4. *When the Le79231 device and ISLAC device is in the anti-sat operating region, this parameter is degraded. The exact degradation depends on system design.*
5. *–55 dBm gain tracking level not tested in production. This parameter is guaranteed by characterization and correlation to other tests.*
6. *This spec is valid from 0 V to VBL or –50 V, whichever is lower in magnitude.*

OPERATING MODES

The Le79231 device receives multiplexed control data on the P1, P2 and P3 pins. The LD pin then controls the loading of P1, P2, and P3 values into the proper bits in the Le79231 device control register. When the LD pin is less than 0.3 V below V_{REF} (< (V_{REF} – 0.3 V)), P1–P3 must contain data for relay control bits RD1, RD2 and RD3. These are latched into the first three bits in the Le79231 device control register. When the LD pin is more than 0.3 V above V_{REF}, P1–P3 must contain ISLIC control data C1, C2, and C3, which are latched into the last three bits of the Le79231 device control register. Connecting the LD pin to VREF locks the contents of the Le79231 device control register.

The operating mode of the Le79231 device is determined by the C1, C2, and C3 bits in the control register of the Le79231 device. Table 1 defines the Le79231 device operating modes set by these signals.

Under normal operating conditions, the ISLIC device does not have active relays. The Le79231 device to ISLAC device interface is designed to allow continuous real-time control of the relay drivers to avoid incorrect data loads to the relay bit latches of the Le79231 device.

To perform external ringing, the ISLAC device from the Intelligent Access voice family is set to external ringing mode (RMODE = 1), enables the ring relay, and puts the Le79231 device in the Standby mode.

Table 1. Operating Modes

C3	C2	C1	Operating Mode	Battery Voltage Selection	Operating Mode	Note
0	0	0	Standby	High Battery (BATH) and BGND	(High ohmic feed): Loop supervision active, A and B amplifiers shut down	1
0	0	1	Tip Open	High Battery (BATH) and BGND	Tip Open: AD at High-Impedance, Channel A power amplifier shut down	1
0	1	0	On-Hook Transmission, Fixed Longitudinal Voltage	High Battery (BATH) and BGND	Fixed longitudinal voltage of –28 V	
0	1	1	Disconnect	Low Battery selection at VBL	AD and BD at High-Impedance, Channel A and B power amplifiers shut down	

Table 1. Operating Modes(Continued)

C3	C2	C1	Operating Mode	Battery Voltage Selection	Operating Mode	Note
1	0	0	RSVD		Active feed, normal or reverse polarity	
1	0	1	Active High Battery	High Battery (BATH) and BGND		
1	1	0	Active Low Battery	Low Battery (BATL) and BGND		
1	1	1	RSVD			

Note:

1. In these modes, the ring lead (B-lead) output has a –50 V internal clamp to battery ground (BGND).

Operating Mode Descriptions

Operating Mode	Description
Disconnect	This mode disconnects both A and B output amplifiers from the AD and BD outputs. The A and B amplifiers are shut down and the Le79231 device selects the low battery voltage at the VBL pin. In the Disconnect state, the currents on IMT and ILG represent the voltages on the SA and SB pins, respectively. These currents are scaled to produce voltages across RMTi and RLGi of $\frac{V_{SA}}{400}$ and $\frac{V_{SB}}{400}$, respectively.
Standby	The power amplifiers are turned off. The AD output is driven by an internal 250 Ω (typical) resistor, which connects to ground. The BD output is driven by an internal 250 Ω (typical) resistor, which connects to the high battery (BATH) at the VBH pin, through a clamp circuit, which clamps to approximately –50 V with respect to BGND. For VBH values above –55 V, the open-circuit voltage, which appears at this output is ~VBH + 7 V. If VBH is below –55 V, the voltage at this output is –50 V. The battery selection for the balance of the circuitry on the chip is VBL. Line supervision remains active. Current limiting is provided on each line to limit power dissipation under short-loop conditions as specified in the “Le79231 device Current-Limit Behavior” section. In external ringing, the standby ISLIC state is selected.
Tip Open	In this mode, the AD (Tip) lead is opened and the BD (Ring) lead is connected to a clamp, which operates from the high battery on VBH pin and clamps to approximately –50 V with respect to BGND through a resistor of approximately 250 Ω (typical). The battery selection for the balance of the circuitry on the chip is VBL.
Active High Battery	In the Active High Battery mode, battery connections are as shown in Table 1. Both output amplifiers deliver the full power level determined by the programmed DC-feed conditions. Active High Battery mode is enabled during a call in applications when a long loop can be encountered.
Active Low Battery	Both output amplifiers deliver the full power level determined by the programmed DC-feed conditions. VBL, the low negative battery, is selected in the Active Low Battery mode. This is typically used during the voice part of a call.
On-Hook Transmission (OHT), Fixed Longitudinal Voltage	In the On-Hook Transmission, Fixed Longitudinal Voltage mode, battery connections are as shown in Table 1. The longitudinal voltage is fixed at the voltage shown in Table 1 to allow compliance with safety specifications for some classes of products.

Driver Descriptions

Driver	Description
R1	A logic 1 on RD1 turns the R1 driver on and operates a relay connected between the R1 pin and VCCD. R1 drives the ring relay when external ringing is selected.
R2	A logic 1 on the RD2 signal turns the R2 driver on and routes current from the R2 pin to the RYE pin. In the option where the RYE pin is connected to ground, the R2 pin can sink current from a relay connected to VCCD. Another option is to connect the RYE pin to the BD (Ring) lead and connect a test load between R2 and the AD (Tip) lead. This technique avoids the use of a relay to connect a test load. However, it does not isolate the subscriber line from the line card. The test load must be connected to the Le79231 device side of the protection resistor to avoid damage to the R2 driver.

Driver	Description
R3	A logic 1 on the RD3 signal turns the R3 driver on and routes current from the R3 pin to the RYE pin. In the option where the RYE pin is connected to ground, the R3 pin can sink current from a relay connected to VCCD. Another option is to connect the RYE pin to the B (Ring) lead and connect a test load between R3 and the A (Tip) lead. This technique avoids the use of a relay to connect a test load. However, it does not isolate the subscriber line from the line card. The test load must be connected to the Le79231 device side of the protection resistor to avoid damage to the R3 driver.

Control bits RD1, RD2, and RD3 do not affect the operating mode of the Le79231 device. These signals usually perform the following functions.

Thermal-Management Equations

Applies to all modes except Standby, which has no thermal management..

Equation	Description
$I_L < 5$ mA $P_{SLIC} = (S_{BAT} – I_L(R_L + 2R_{FUSE})) • I_L + 0.3$ W $PT_{RTMG} = 0$	TMG resistor-current is limited to be 5 mA < I_L. If $I_L < 5$ mA, no current flows in the TMG resistor and it all flows in the Le79231 device.
$I_L > 5$ mA RMGPi = RMGLi = R_{TMG} PT_{RTMG}: total power dissipation of RMGPi and RMGLi $R_{TMG} = (S_{BAT} – I_L(R_L + 2R_{FUSE})) / (2(I_L – 5$ mA)) $P_{SLIC} = I_L(S_{BAT} – I_L(R_L + 2R_{FUSE})) + 0.3$ W – PT_{RTMG} $PT_{RTMG} = (I_L – 5$ mA$)^2(2R_{TMG})$	These equations are valid when $R_{TMG} • (I_L – 5$ mA$) < (S_{BAT} – (R_L + R_F)I_L) / 2 – 2$ because the longitudinal voltage is one-half the battery voltage and the TMG switches require approximately 2 V. To choose a power rating for RTMG: $P_{RATING} > PT_{RTMG} / 2$

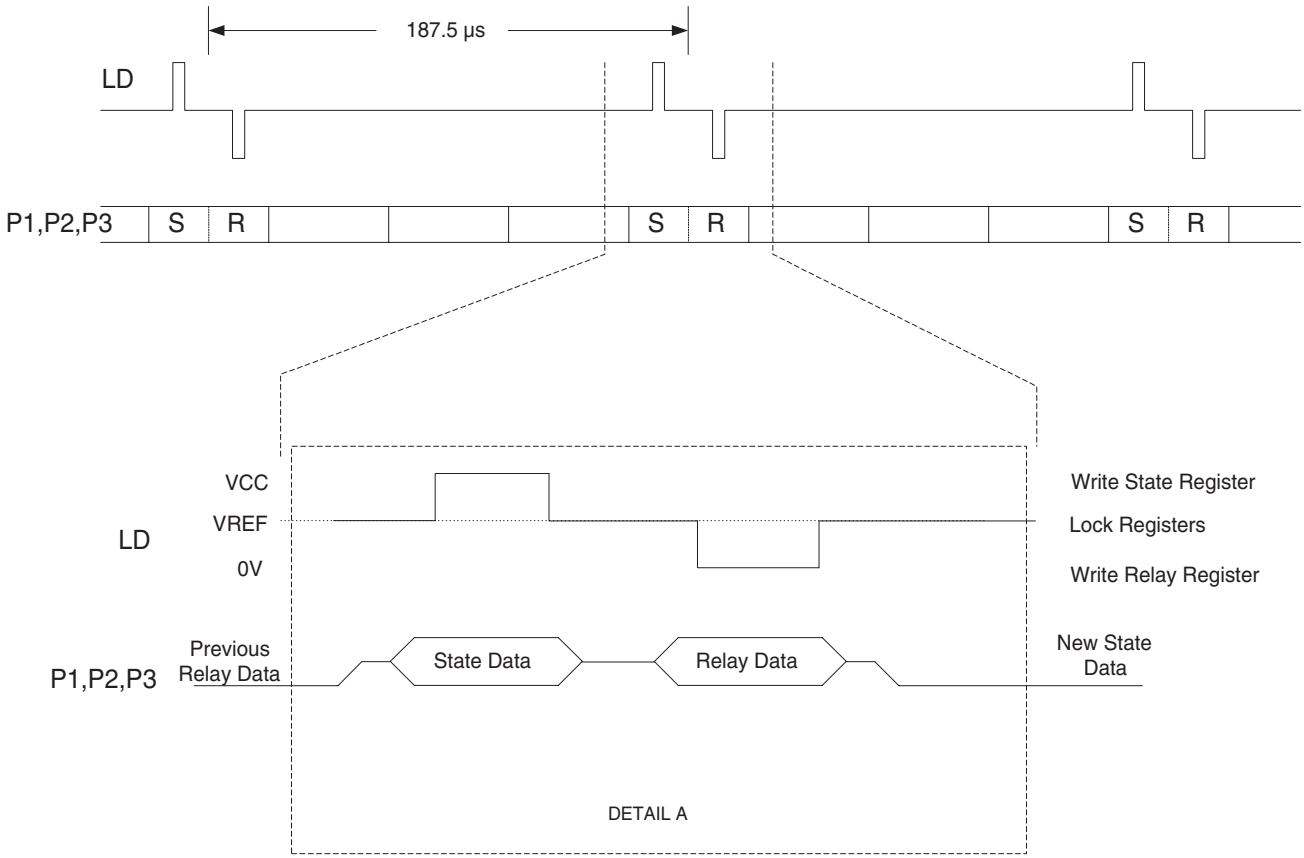
TIMING SPECIFICATIONS

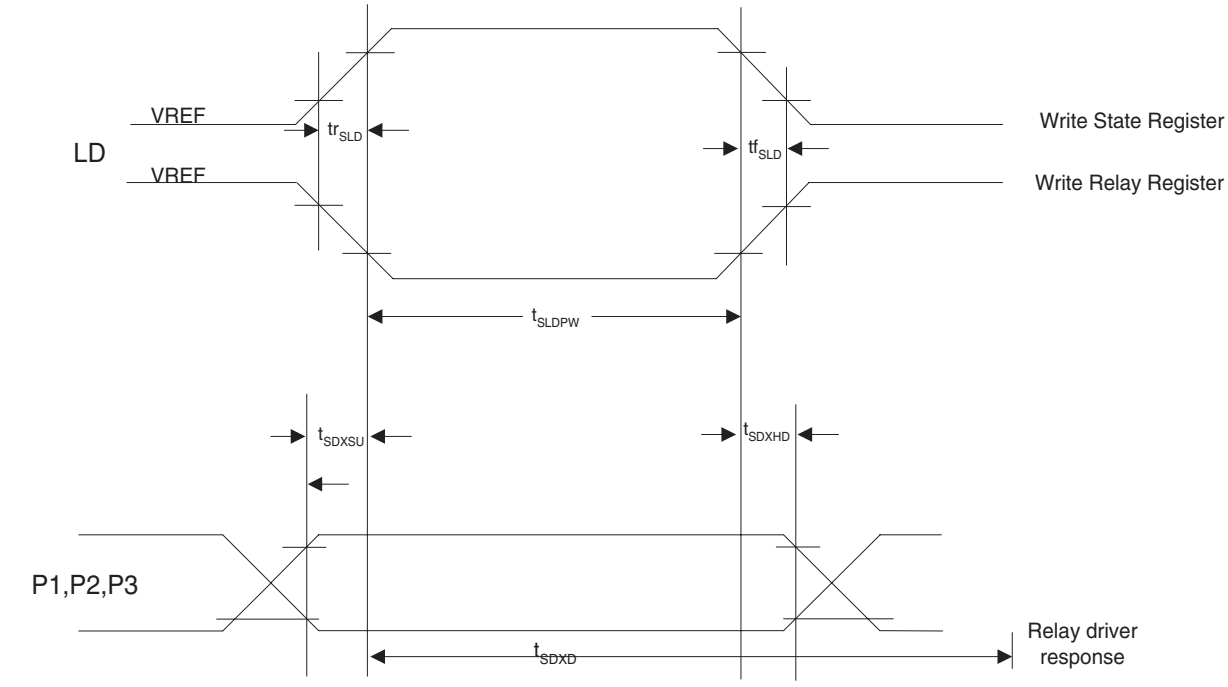
Symbol	Signal	Parameter	Min	Typ	Max	Unit
trSLD	LD	Rise time Le79231 device LD pin			2	µs
tfSLD	LD	Fall time Le79231 device LD pin			2	
tSLDPW	LD	LD minimum pulse width	3			
tSDXSU	P1,P2,P3	P1–3 data Setup time	4.5			
tSDXHD	P1,P2,P3	P1–3 data hold time	4.5			
tSDXD	P1,P2,P3	Max P1–3 data delay			5	

Note:

1. *The P1–3 pins are updated continuously during operation by the LD signal.*
2. *After a power-on reset or hardware reset, the relay outputs from the Le79231 device turn all relays off. An unassuming state is to place the relay control pins, which are level triggered, to a reset state for all relays. Any noise encountered only raises the levels toward the register lock state.*
3. *When writing to the ISLIC device registers, the sequence is:*
   a) *Set LD pin to mid-state*
   b) *Place appropriate data on the P1–3 pins*
   c) *Assert the LD pin to High or Low to write the proper data*
   d) *Return LD pin to mid-state*
4. *Le79231 device registers are refreshed at 5.33 kHz when used with an ISLAC device.*
5. *If the clock or MPI becomes disabled, the LD pins and P1–3 returns to 0 V state, thus protecting the Le79231 device and the line connection.*
6. *Not tested in production. Guaranteed by characterization.*

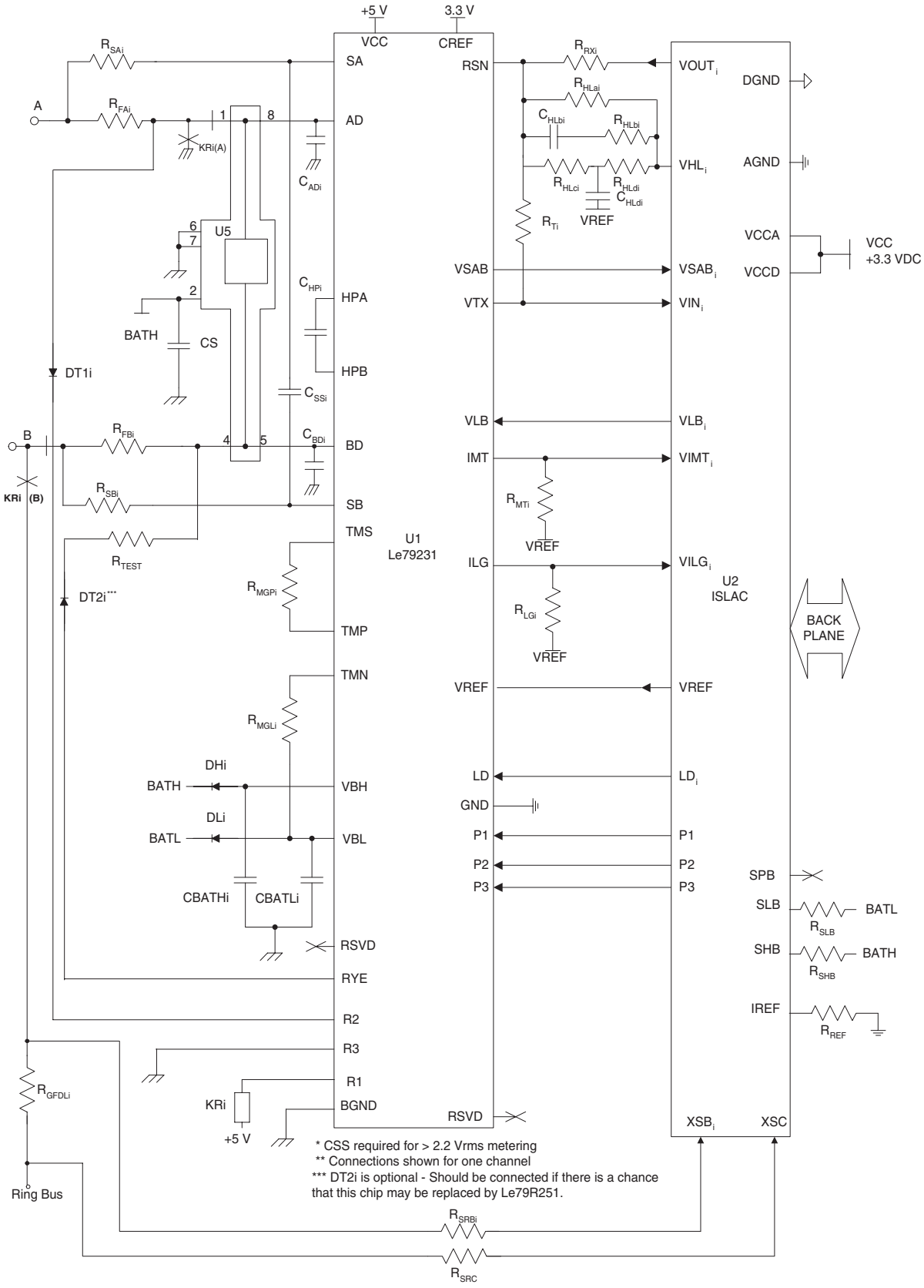
WAVEFORMS


187.5 µs
LD
P1,P2,P3
S
R
S
R
S
R
VCC
VREF
0V
LD
Write State Register
Lock Registers
Write Relay Register
Previous
Relay Data
P1,P2,P3
State Data
Relay Data
New State
Data
DETAIL A


VREF
LD
VREF
trSLD
tfSLD
Write State Register
Write Relay Register
tSLDPW
tSDXSU
tSDXHD
P1,P2,P3
tSDXD
Relay driver
response

APPLICATION CIRCUIT

External Ringing Line card Schematic



LINE CARD PARTS LIST

The following list defines the parts and part values required to meet target specification limits for channel i of the line card (i = 1, 2, 3, 4).

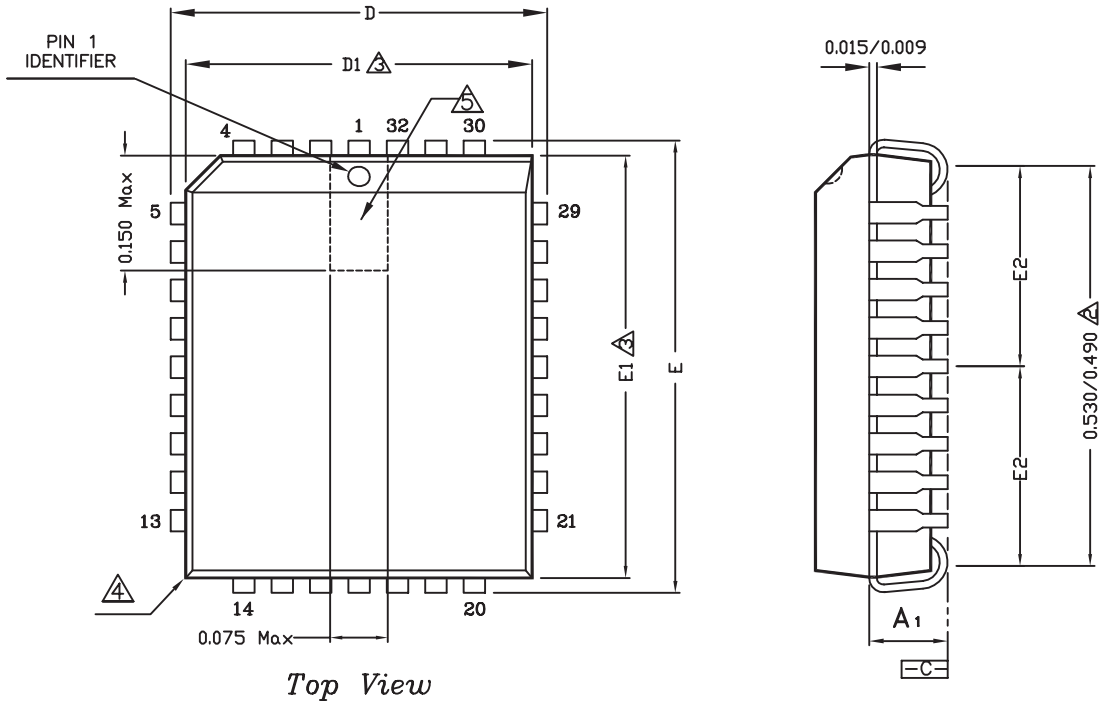
Item	Type	Value	Tol.	Rating	Comments
U1	Le79231				ISLIC device
U2	Le79Q224x				ISLAC device
U5	TISP61089			80 V	Transient Voltage Suppressor, Power Innovations
DH_i, DL_i, $DT1_i$, $DT2_i$ (see note 4)	Diode	100 mA		100 V	50 ns
R_{FAi}, R_{FBi}	Resistor	50 Ω	2%	2 W	Fusible PTC protection resistors
R_{SAi}, R_{SBi}	Resistor	200 kΩ	2%	1/4 W	Sense resistors
R_{Ti}	Resistor	80.6 kΩ	1%	1/10 W	
R_{RXi}	Resistor	100 kΩ	1%	1/10 W	
R_{REF}	Resistor	69.8 kΩ	1%	1/10 W	Current reference
R_{MGLi}, R_{MGPi}	Resistor	1 kΩ	5%	1 W	Thermal management resistors
R_{SHB}, R_{SLB}	Resistor	750 kΩ	1%	1/8 W	Battery Sense Resistors
R_{HLai}	Resistor	40.2 kΩ	1%	1/10 W	
R_{HLbi}	Resistor	4.32 kΩ	1%	1/10 W	
R_{HLci}	Resistor	2.87 kΩ	1%	1/10 W	
R_{HLdi}	Resistor	2.87 kΩ	1%	1/10 W	
C_{HLbi}	Capacitor	3.3 nF	10%	10 V	Not Polarized
C_{HLdi}	Capacitor	0.82 µF	10%	10 V	Ceramic
R_{MTi}	Resistor	3.01 kΩ	1%	1/8 W	Metallic Current Sense Resistors
R_{LGi}	Resistor	6.04 kΩ	1%	1/8 W	Longitudinal Current Sense Resistors
R_{TEST}	Resistor	2 kΩ	1%	1 W	Test board
C_{ADi}, C_{BDi} (see note 1)	Capacitor	22 nF	10%	100 V	Ceramic, not voltage sensitive
C_{BATHi}, C_{BATLi}	Capacitor	100 nF	20%	100 V	Ceramic
C_{HPi}	Capacitor	22 nF	20%	100 V	Ceramic
C_{Si} (see note 1)	Capacitor	100 nF	20%	100 V	Protector speed–up capacitor
C_{SSi} (see note 3)	Capacitor	56 pF	5%	100 V	Ceramic
R_{GFDi}	Resistor	510 Ω	2%	2 W	1.2 W typ
R_{SRBi}, R_{SRc}	Resistor	750 kΩ	2%	1/4 W	Matched to within 0.2% for initial tolerance and 0º to 70º C ambient temperature range (see note 2). 17 mW typ
KR_i	Relay	5 V Coil			DPDT

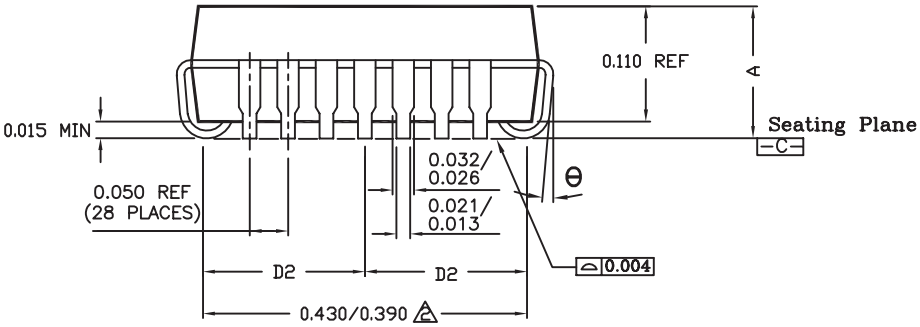
Note:

1. *Value can be adjusted to suit application.*
2. *Can be looser for relaxed ring-trip requirements.*
3. *Required for metering > 2.2 Vrms, otherwise may be omitted.*
4. *$DT2_i$ is optional - Should be put if there is a chance that this chip may be replaced by Le79R251.*

PHYSICAL DIMENSIONS

32-Pin PLCC



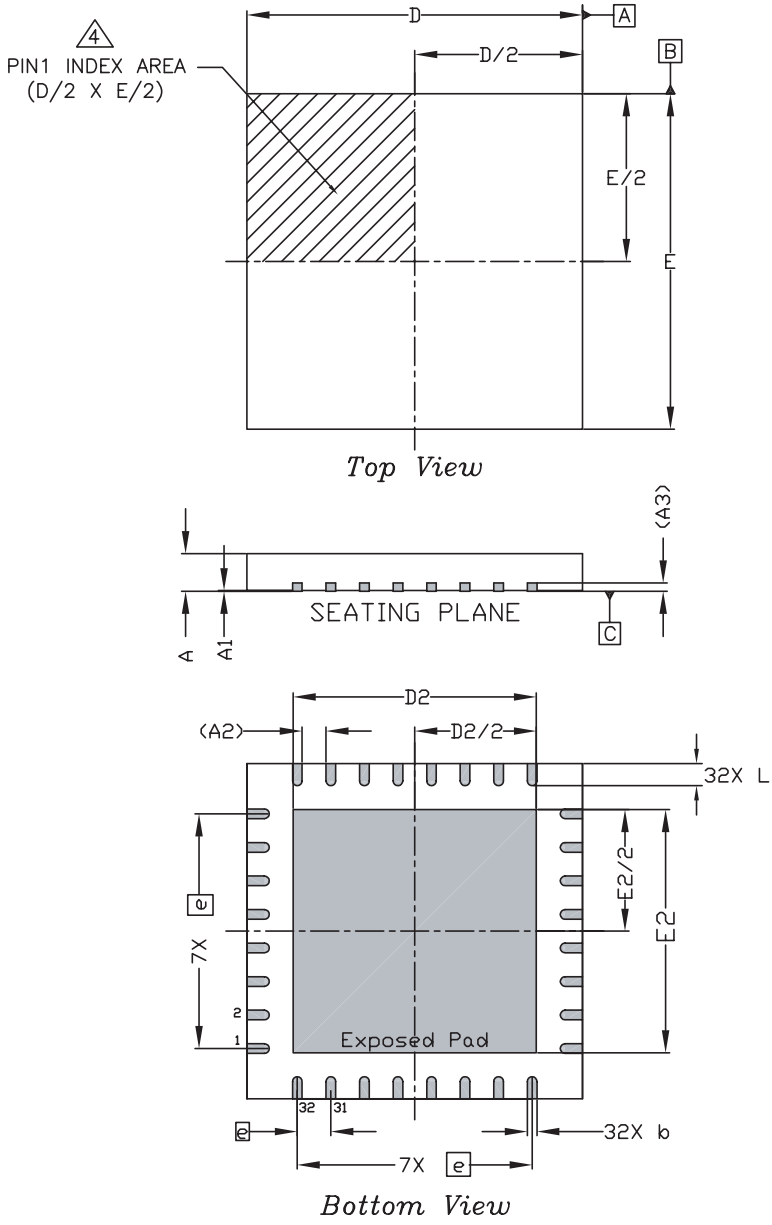


Symbol	Dimension in inch		
	Min	Nom	Max
A	0.125	—	0.140
A1	0.075	0.090	0.095
D	0.485	0.490	0.495
D1	0.447	0.450	0.453
D2	0.205 REF		
E	0.585	0.590	0.595
E1	0.547	0.550	0.553
E2	0.255 REF		
θ	0°	—	10°

NOTE :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14,5M–1994.
2. TO BE MEASURED AT SEATING PLANE C CONTACT POINT.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTURSION IS 0.010 IN PER SIDE. DIMENSIONS D, AND E, INCLUDE MOLD MISMATCH AND DETERMINED AT THE PARTING LINE; THAT IS D1 AND E1 ARE MEASURED AT THE EXTREME MATERIAL CONDITION AT THE UPPER OR LOWER PARTING LINE.
4. EXACT SHAPE OF THIS FEATURE IS OPTIONAL.
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
6. SUM OF DAM BAR PROTRUSIONS TO BE 0.007 MAX PER LEAD.
7. CONTROLLING DIMENSION : INCH.
8. REFERENCE DOCUMENT : JEDEC MS–016

32-Pin QFN



Symbol	Dimension in mm		
	Min	Nom	Max
A	0.80	0.90	1.00
A2		0.57 REF	
b	0.18	0.23	0.28
D		8.00 BSC	
D2	5.70	5.80	5.90
E		8.00 BSC	
E2	5.70	5.80	5.90
e		0.80 BSC	
L	0.43	0.53	0.63
N		32	
A1	0.00	0.02	0.05
A3		0.20 REF	

NOTES :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14,5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEP 95–1 SSP–012. DETAILS OF THE TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. COPLANARITY APPLIES TO EXPOSED PAD AS WELL AS THE TERMINALS.
6. REFERENCE DOCUMENT : JEDEC MO–220

REVISION SUMMARY

Revision A to Revision B

- Revision A was a condensed version of the data sheet. Revision B contains the full version.

Revision B to Revision C

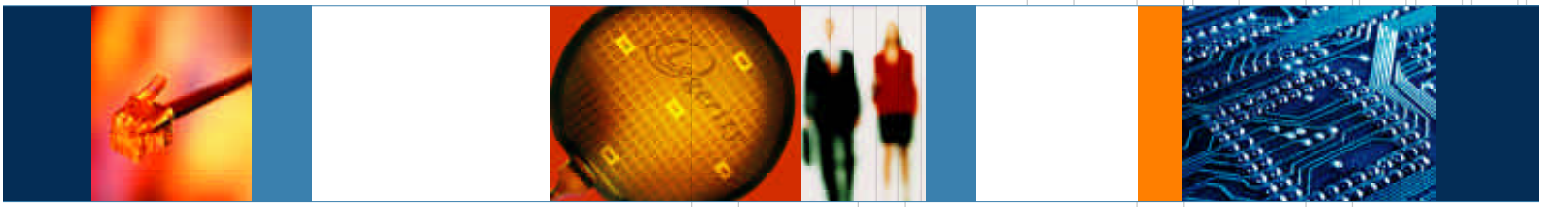
- Page 12, Linecard Parts List, Rows CHLbi and CHLdi: switched the numbers in the “Values” column.

Revision C to Revision D

- Applied new format.
- Global change: RTMG1 to RMGLi, and RTMG2 to RMGPi.
- Updated Device Internal Block Diagram.
- Updated pin description for LD pin.
- Modified text in "Electrical Operating Ranges" section.
- Modified text in "Environmental Operating Ranges" section.
- “Absolute Maximum Rating” for humidity changed from “tbd” to 5% - 95%.
- Under "Specifications", Power Dissipation table, changed the Power Supply Current On-Hook Disconnect value from 0.5 to 0.4.
- Made changes throughout the DC Specifications table.
- Updated “Target Specifications” for rows 10, 12, and 19.
- Updated “Transmission Specifications” for rows 5, 6, 7, 8, 10, 12 and 13.
- Renamed "Fault Indications" table to "Thermal Shutdown Fault Indications"; modified text.
- Modified text in "Operating Modes" section.
- Modified Thermal Management Equations for $I_L > 5$ mA
- Updated Waveforms graphic.
- Updated External Ringing Linecard Schematic.

Revision D to Revision E

- Added QFN package data to “Connection Diagram,” “Absolute Maximum Ratings,” and “Physical Dimensions.”
- Updated "Am" OPNs (Ordering Part Numbers) to "Le" throughout document
- The following changes were made to the "Ordering Information" section:
  - Removed chip graphic
  - Added entries for Le79231JC and Le79231QC
  - Added notes
- In "Features," added bullet for space savings feature
- Removed references to DISLAC documents in "Related Literature"
- Standardized notes in "Absolute Maximum Ratings" section
- In "Thermal Management Equations", IL > 5 mA, deleted the last sentence in the Description section
- Updated 32-Pin PLCC physical dimensions graphic
- In "Electrical Characteristics", Absolute Maximum Ratings table, added Theta JA data for both packages



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