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	SPECIFICATION	

DEVICE SPECIFICATION for

Passive Matrix COLOR LCD Module

(640×480 dots)

Model No.

LM10V33

□CUSTOMER'S APPROVAL

DATE

BY

PRESENTED

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LIQUID CRYSTAL DISPLAY GROUP

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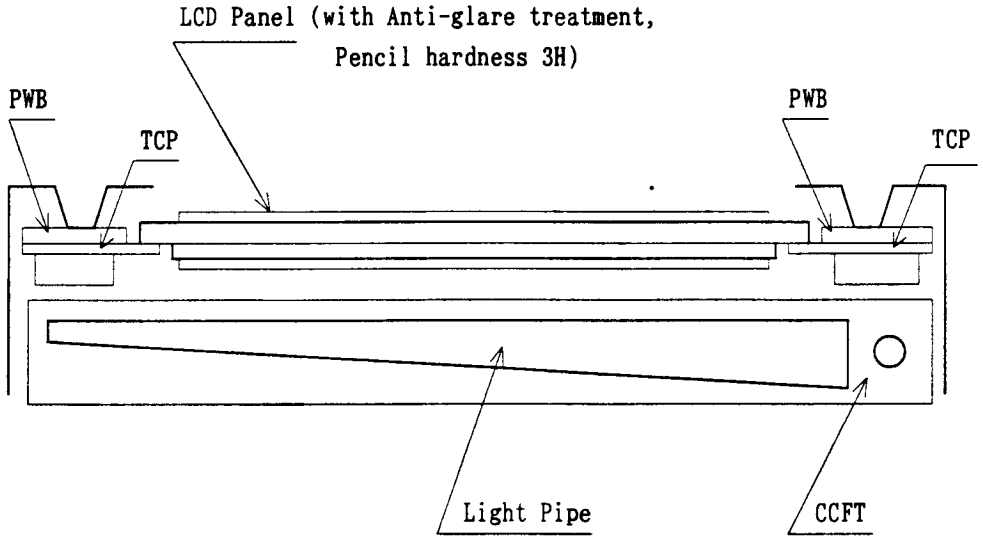
DATE	REF. PAGE PARAGRAPH DRAWING No.	REVISED No.	SUMMARY	CHECK & APPROVAL
FEB.28.1997	PAGE. 2	⚠1	Revised(Table No.1) BEZEL OPENING AREA 220.8±0.3×167.2±0.3 →215.2±0.3×162.4±0.3	Y. Inoue
MAR.28.1997	PAGE. 18	⚠2	Revised(5-1 Rating) Lamp life time 10 000Min →15 000Min. 25 000TYP.	Y. Inoue
JUL.03.1998	PAGE. 3	⚠3	Revised(4-2 Table No.3) Ambient temperature +40 ℃ →+50 ℃	Y. Inoue

1. Application

This data sheet is to introduce the specification of LM10V33, Passive Matrix type Color LCD Module.

2. Construction and Outline

Construction: 640×480 dots color display Module consisting of an LCD panel, PWB(printed wiring board) with electric components mounted onto, TCP(tape carrier package) to connect the LCD panel and PWB electrically, and plastic chassis with CCFT back light and bezel to fix them mechanically.
Signal ground(VSS) is connected with the metal bezel.
DC/DC converter is built in.



Outline : See Fig. 10
Connection : See Fig. 10 and Table 6

3. Mechanical Specifications

Table 1

	Parameter	Specifications	Unit
	Outline dimensions	264±0.5(W)×193.6±0.5(H)×8.5MAX(D)	mm
⚠1	BEZEL OPENING AREA	215.2±0.3(W)×162.4±0.3(H)	mm
	Display format	640(W)×480(H) full dots	—
	Dot size	0.09×RGB(W)×0.31(H)	mm
	Dot spacing	0.02	mm
	*1 Base color	Normally black *2	—
	Weight	Approx. 450	g

*1 Due to the characteristics of the LC material, the colors vary with environmental temperature.

*2 Negative-type display
Display data "H" : ON → transmission
Display data "L" : OFF → light isolation

4. Absolute Maximum Ratings

4-1 Electrical absolute maximum ratings

Table 2

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Supply voltage (Logic)	V_{DD}-V_{SS}	0	6.0	V	Ta=25 °C
Input voltage	V_{IN}	-0.3	V_{DD}	V	Ta=25 °C

4-2 Environmental Conditions

Table 3

Item	Tstg		Topr		Remark
	MIN.	MAX.	MIN.	MAX.	
⚠3 Ambient temperatuer	-25 ℃	+60 ℃	0 ℃	+50 ℃	Note 4)
Humidity	Note 1)		Note 1)		No condensation
Vibration	Note 2)		Note 2)		3 directions (X/Y/Z)
Shock	Note 3)		Note 3)		6 directions (±X±Y±Z)

Note 1) Ta≦40 ℃.....95 % RH Max

Ta>40 ℃.....Absolute humidity shall be less than Ta=40 ℃/95 % RH.

Note 2)

Table 4

Frequency	10 Hz～57 Hz	57 Hz～500 Hz
Vibration level	—	9.8 m/s²
Vibration width	0.075 mm	—
Interval	10 Hz～500 Hz～10 Hz/11.0 min	

2 hours for each direction of X/Y/Z (6 hours as total)

Note 3) Accerelation : 490 m/s²

Pulse width : 11 ms

3 times for each direction of ±X/±Y/±Z

⚠3 Note 4) As opto-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 ℃ and it becomes stable.

3. Electrical Specifications

3-1 Electrical characteristics

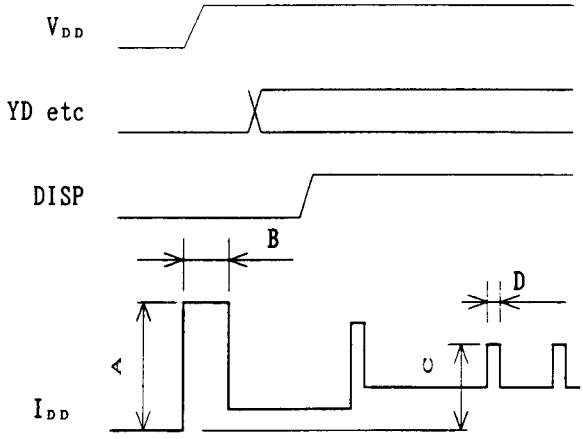
Table 4 Ta=25 °C, V_{DD}=5 V±10 %

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_{DD}-V_{SS}	Ta=0～40 °C	4.5	5.0	5.5	V
Contrast adjust voltage	Vcon -V_{SS}	Ta=0 °C	0.8	—	—	V
		Ta=25 °C	1.35	1.95	2.55	V
		Ta=40 °C	—	—	2.80	V
Input signal voltage	V_{IN}	"H" level	0.8V_{DD}	—	V_{DD}	V
		"L" level	0	—	0.2V_{DD}	V
Input leakage current	I_{ILL} (Logic)	"H" level	—	—	0.1	mA
		"L" level	-0.1	—	—	mA
	I_{ILV}	Vcont=2.8V	-1.0	—	1.0	mA
Supply current(Logic)	I_{DD}	Note 2)	—	210	320	mA
Power consumption	Pd	Note 2)	—	1050	1600	mW
Rush Current (Logic)	I_{DD}	Ta=25 °C, Note 1)-①	—	—	2 A×2 ms	
		Ta=25 °C, Note 1)-②	—	—	1 A×10 μs	

Note 1) Under the following conditions.; Logic voltage(V_{DD}) should be designed to supply following Inrush current.

①Immediately after the rise of V_{DD}.

②Under the situation that DISP signal is on and kept steady.



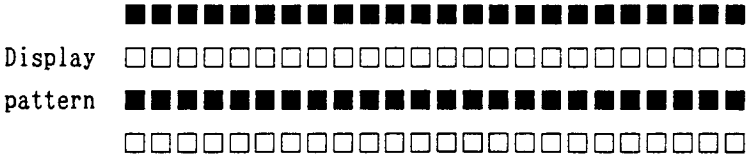
Measurement Curcuit: TMD-18-3 (Vdd Power Supply) (TAKASAGO)

A: 2 A MAX
B: 2 ms MAX
C: 1 A MAX
D: 10 μs MAX

Note 2) Under the following conditions.;

Vcon-V_{SS} : contrast max.(1.95 V TYP.)

V_{DD}-V_{SS}=5 V, Frame frequency=(120) Hz, Display pattern = black/white stripe pattern.



This value is direct current.

3-2 Interface signals

○L C D

Table 5

Pin No	Symbol	Description	Level
1	DL4	Display data signal (Lower)	H(ON), L(OFF)
2	V_{SS}	Ground potential	–
3	DL5	Display data signal (Lower)	H(ON), L(OFF)
4	YD	Scan start-up signal	"H"
5	DL6	Display data signal (Lower)	H(ON), L(OFF)
6	LP	Input data latch signal	"H"→"L"
7	DL7	Display data signal (Lower)	H(ON), L(OFF)
8	V_{SS}	Ground potential	–
9	V_{SS}	Ground potential	
10	XCK	Data input clock signal	"H"→"L"
11	DL0	Display data signal (Lower)	H(ON), L(OFF)
12	V_{CON}	Contrast adjust voltage	–
13	DL1	Display data signal (Lower)	H(ON), L(OFF)
14	V_{DD}	Power supply for logic and LCD (+5V)	–
15	V_{SS}	Ground potential	–
16	V_{DD}	Power supply for logic and LCD (+5V)	–
17	DL2	Display data signal (Lower)	H(ON), L(OFF)
18	DISP	Display control signal	H(ON), L(OFF)
19	DL3	Display data signal (Lower)	H(ON), L(OFF)
20	NC	–	–
21	V_{SS}	Ground potential	–
22	DU3	Display data signal (Upper)	H(ON), L(OFF)
23	DU4	Display data signal (Upper)	H(ON), L(OFF)
24	DU2	Display data signal (Upper)	H(ON), L(OFF)
25	DU5	Display data signal (Upper)	H(ON), L(OFF)
26	DU1	Display data signal (Upper)	H(ON), L(OFF)
27	V_{SS}	Ground potential	–
28	DU0	Display data signal (Upper)	H(ON), L(OFF)
29	DU6	Display data signal (Upper)	H(ON), L(OFF)
30	V_{SS}	Ground potential	–
31	DU7	Display data signal (Upper)	H(ON), L(OFF)

○C C F T

Pin No	Symbol	Description	Level
1	HV	High voltage lineal (from Inverter)	–
2	NC		–
3	GND	Ground line (from Inverter)	–

NOTE) Pin No. and its location are shown in Fig.5.

○L C D

Used connector:DF9B-31P-1V (HIROSE)

Mating connector:DF9B-31S-1V (HIROSE)

○C C F T

Used connector:BHR-03VS-1 (JST)

Mating connector:SM02(8.0)B-BHS (JST)

Except above connector shall be out of guaranty

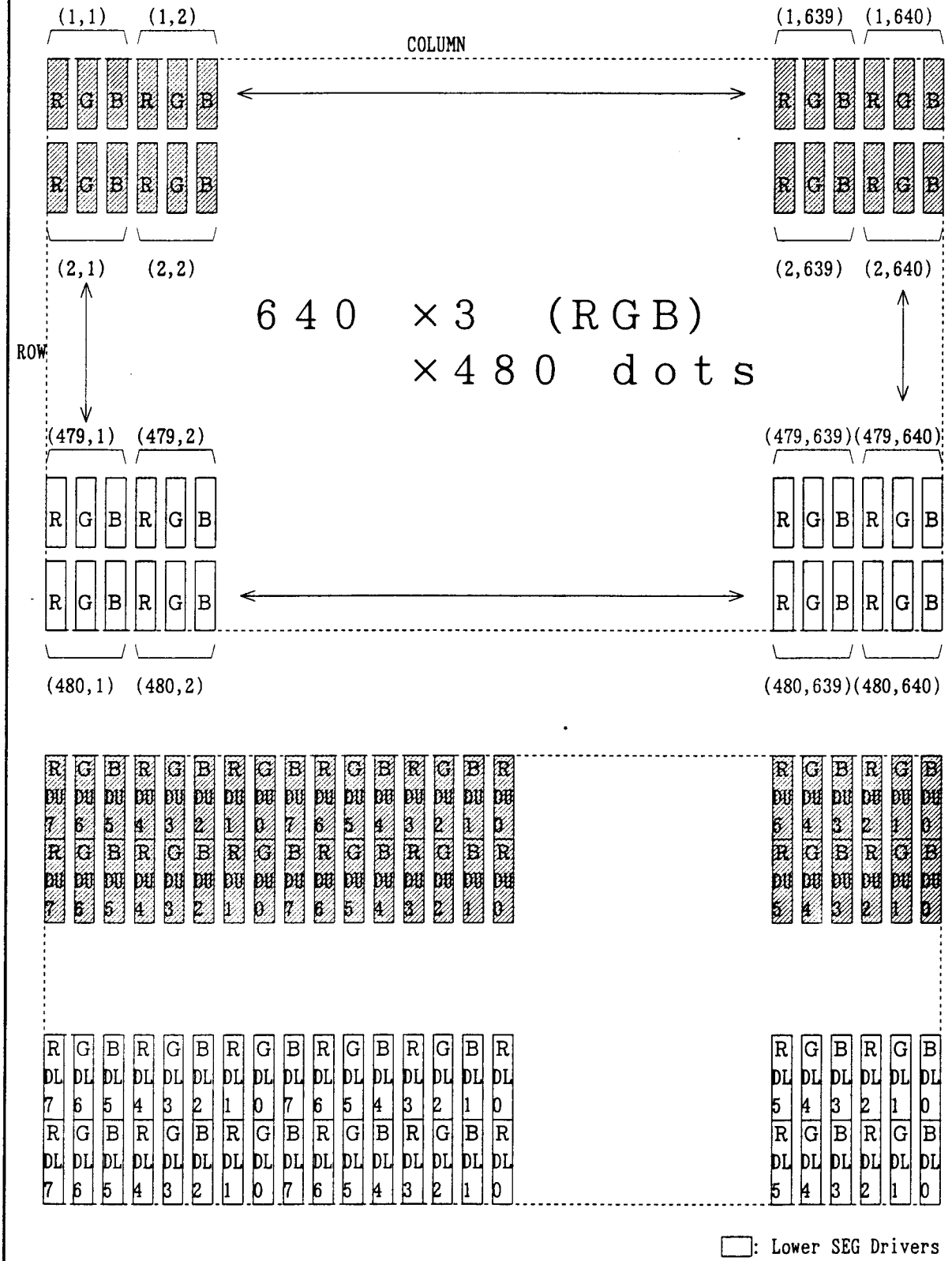


Fig.1 Dot chart of display area

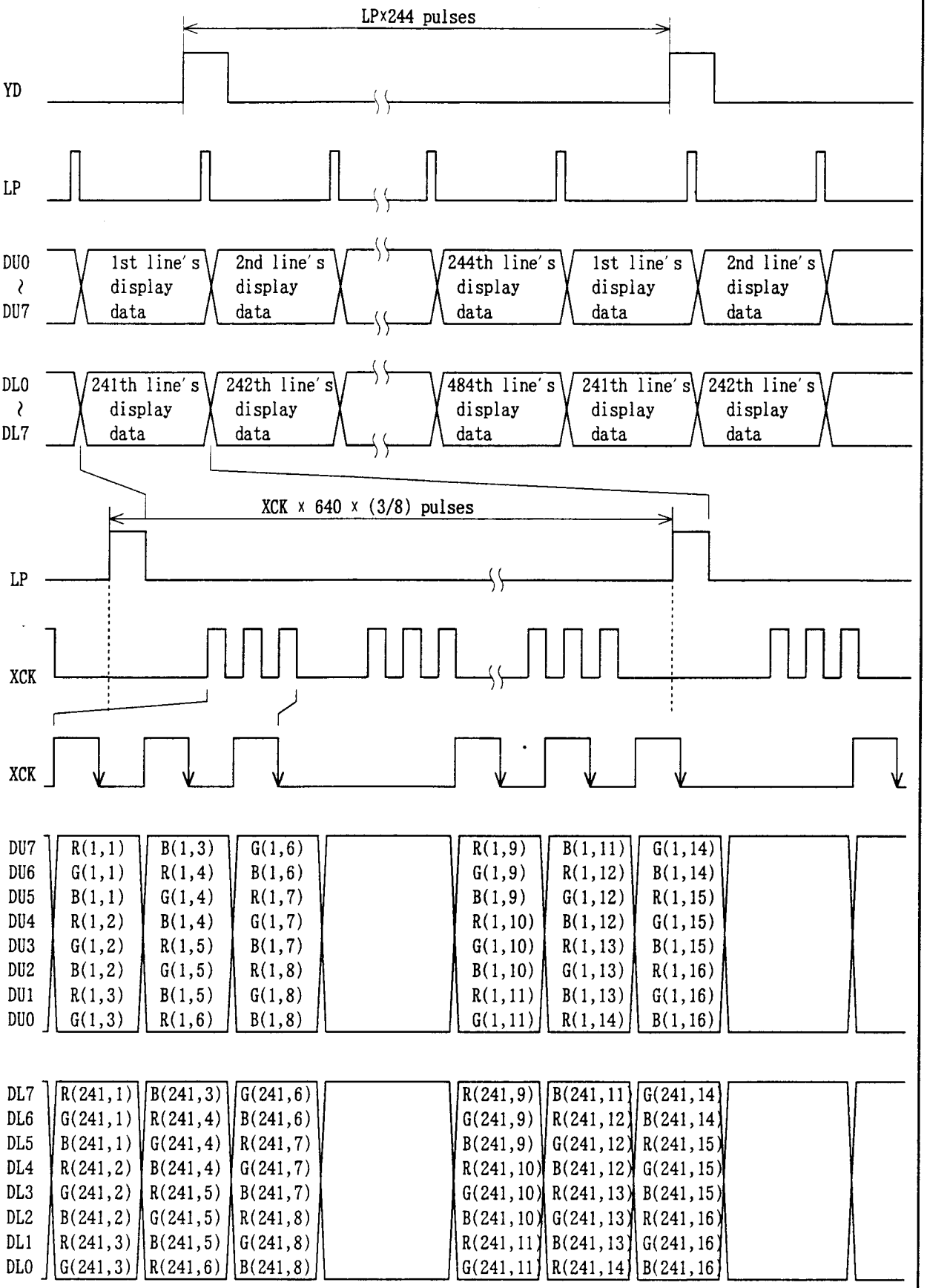


Fig.2 Data input timing chart

Table 6 Interface timing ratings

Item	Symbol	Rating MIN.	Rating TYP.	Rating MAX.	Unit
Frame cycle *1	tFRM	8.33		16.94	ms
YD signal "H" level set up time	tHYS	100			ns
"H" level hold time	tHYH	100			ns
"L" level set up time	tLYS	100			ns
"L" level hold time	tLYH	40			ns
LP signal "H" level pulse width	tWLPH	200			ns
XCK signal clock cycle	tCK	80			ns
"H" level clock width	tWCKH	30			ns
"L" level clock width	tWCKL	30			ns
Data set up time	tDS	5			ns
hold time	tDH	40			ns
LP↑ allowance time from XCK↓	tLS	200			ns
XCK↑ allowance time from LP↓	tLH	200			ns
Input signal rise/fall time	tr,tf			12	ns

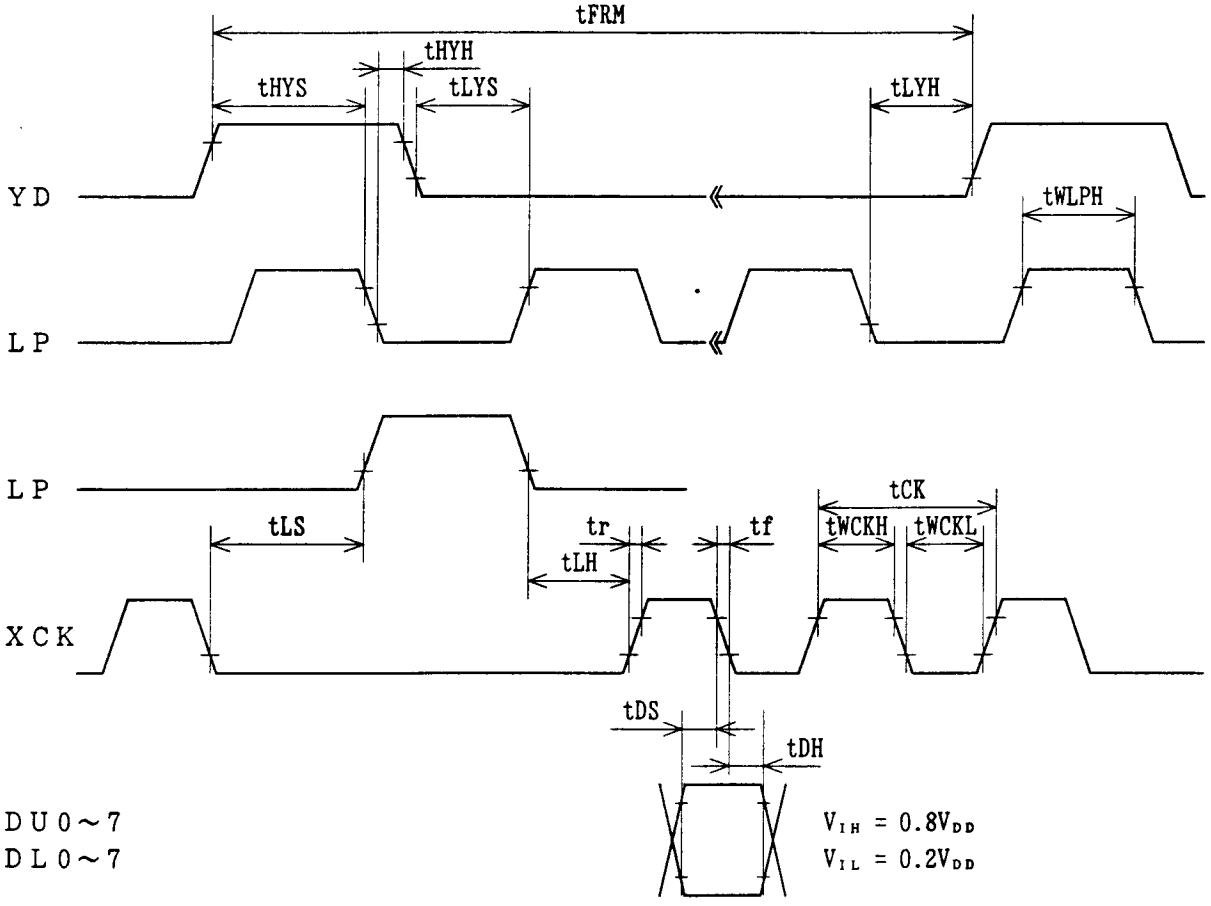


Fig.3 Interface timing chart

*1 LCD module functions at the minimum frame cycle of 8.33 ms(Maximum frame frequency of 120 Hz).
Owing to the characteristics of LCD module,"shadowing" will become more eminent as frame frequency goes up,while flicker will be reduced.

According to our experiments,frame cycle of 8.33 ms Min. or frame frequency of 120 Hz max. will demonstrate optimum display quality in terms of flicker and "shadowing". But since judgement of display quality is subjective and display quality such as "shadowing" is patturn dependent,it is recommended that decision of frame frequency, to which power consumption of the LCD module is proportional,be made based on your own through testing on the LCD module with every possible patterns displayed on it.

※ The intervals of one LP fall and the next must be always the same, and LPs must be input continuously.
The interval must be 70 μs Max.

6. module Driving Method

6.1 Circuit configuration

Fig.9 shows the block diagram of the module's circuitry.

6.2 Display Face Configuration

The display consists of 640x3 (R,G,B)x480 dots as shown in Fig.1.
The interface is single panel with double drive to be driven at 1/244 duty ratio.

6.3 Input Data and Control Signal

The LCD driver is 240 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits. Input data for each row (640x3 R,G,B) will be sequentially transferred in the form of 8 bit parallel data through shift registers from top left of the display together with clock signal(XCK) .

When input of one row (640 x 3,R,G,B dots) is completed, the data will be latched in the form of parallel data corresponding to the signal electrodes by the falling edge of latch signal (LP). Then, the corresponding drive signals will be transmitted to the 640 x 3 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal (YD) has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st row of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD. While the data of 1st row are being displayed, the data of 2nd row are entered. When data for 640x3 dots have been transferred, they will be latched by the falling edge of LP, switching the display to the 2nd row.

Such data input will be repeated up to the 244th row of each display segment, from upper row to lower rows, to complete one frame of display by time sharing method.

Simultaneously the same scanning sequence occur at the lower panel.
Then data input proceeds to the next display frame.

YD generates scan signal to drive horizontal electrodes.

Since DC voltage, if applied to LCD panel, causes chemical reaction in LC materials, causing deterioration of the materials, drive wave-form shall be inverted at every display frame to prevent the generation of such DC voltage. Control Signal M plays such a role.

Because of the characteristics of the CMOS driver LSI, the power consumption of the display module goes up with the clock frequency of XCK.
To minimize data transfer speed of XCK clock the LSI has the system of transferring 8 bit parallel data through the 8 lines of shift registers.
Thanks to this system the power consumption of the display module is minimized.

In this circuit configuration, 8 bit display data shall input to data input pins of DU0～7 and DL0～7.

Furthermore, the display module has bus line system for data input to minimize the power consumption with data input terminals of each driver LSI being activated only when relevant data input is fed.

Data input for column electrodes and chip select of driver LSI are made as follows:

The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI right next side is selected when data of 240 dot (30XCK) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face. This process is followed simultaneously both at the top and bottom column drivers LSI's.

Thus data input will be made through 8 bit bus line sequentially from the left end of the display face.

Since this display module contains no refresh RAM, it requires the above data and timing pulse inputs even for static display.

The timing chart of input signals are shown in Fig. 3 and Table 7.

7. Optical Characteristics

Ta = 25 °C, V_{DD} = 5.0 V, Vcon-V_{SS} = Vmax

Table 8

Following spec are based upon the electrical measuring conditions, on which the contrast of perpendicular direction ($\theta x = \theta y = 0°$) will be MAX.

Parameter		Symbol	Condition		MIN.	TYP.	MAX.	Unit	Remark
Viewing angle range		θx	Co>5.0	$\theta y = 0°$	-30	-	30	dgr.	Note1)
		θy		$\theta x = 0°$	-15	-	25	dgr.	
Contrast ratio		Co	$\theta x = \theta y = 0°$		15	30	-	—	Note2)
Response time	Rise	τr	$\theta x = \theta y = 0°$		-	220	300	ms	Note3)
	Decay	τd	$\theta x = \theta y = 0°$		-	80	100	ms	
module chromaticity	White	x	$\theta x = \theta y = 0°$		-	0.275	-	—	
		y	$\theta x = \theta y = 0°$		-	0.320	-	—	

Note 1) The viewing angle range is defined as shown Fig.4.

Note 2) Contrast ratio is defined as follows:

$$Co = \frac{\text{Luminance(brightness) all pixels "White" at Vmax}}{\text{Luminance(brightness) all pixels "dark " at Vmax}}$$

Vmax is defined in Fig.6.

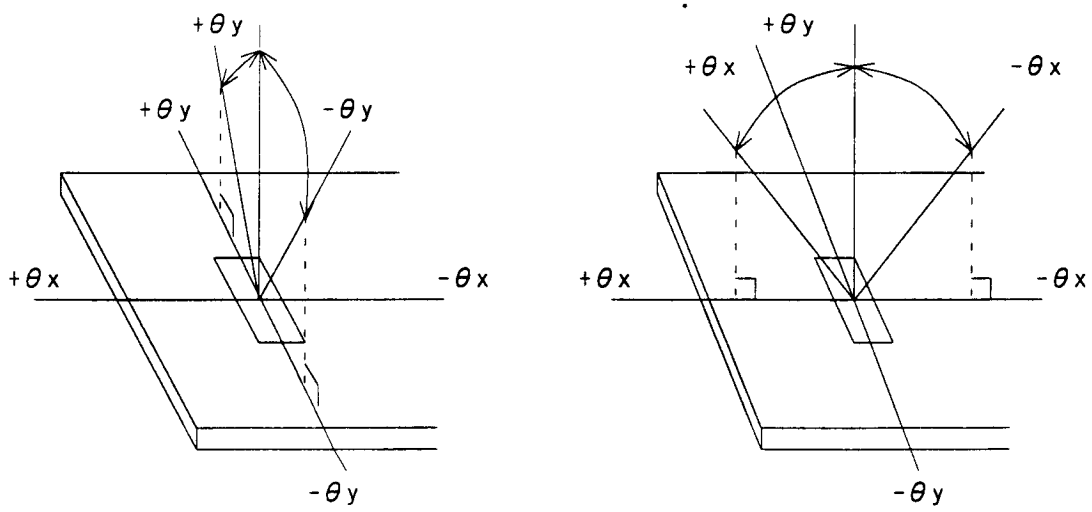
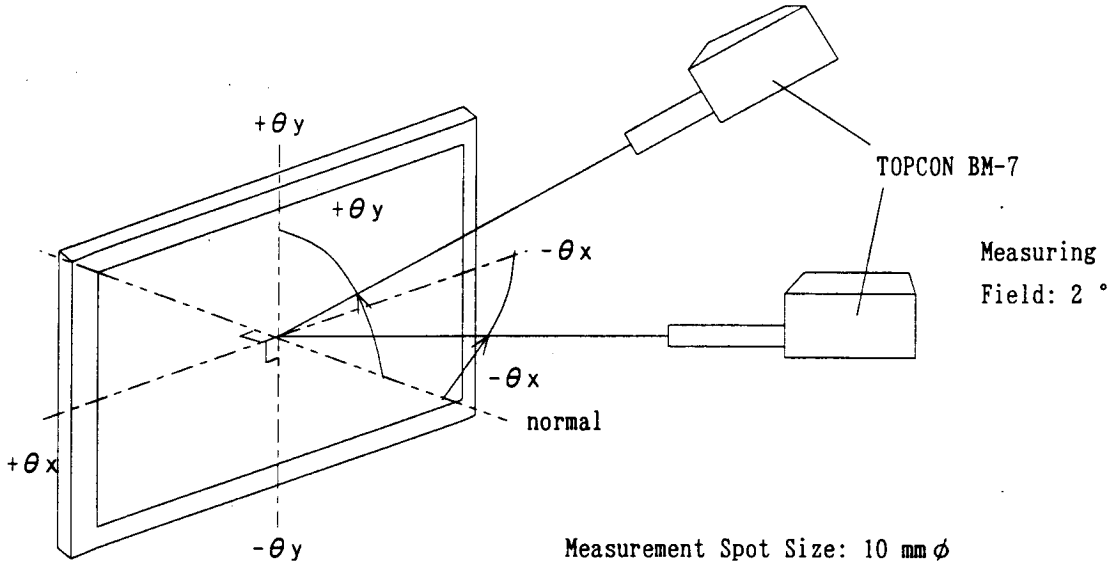


Fig.4 Definition of Viewing Angle

Note 3) The response characteristics of photo-detector output are measured as shown in Fig.7, assuming that input signals are applied so as to select and deselect the dots to be measured, in the optical characteristics test method shown in Fig.8.



Measurement Spot Size: 10 mmϕ

θx:Angle from "normal" to viewing surface roteted about the horizontal axis.

θy:Angle from "normal" to viewing surface roteted about the vertical axis.

Fig. 5 Optical Characteristics Test Method I

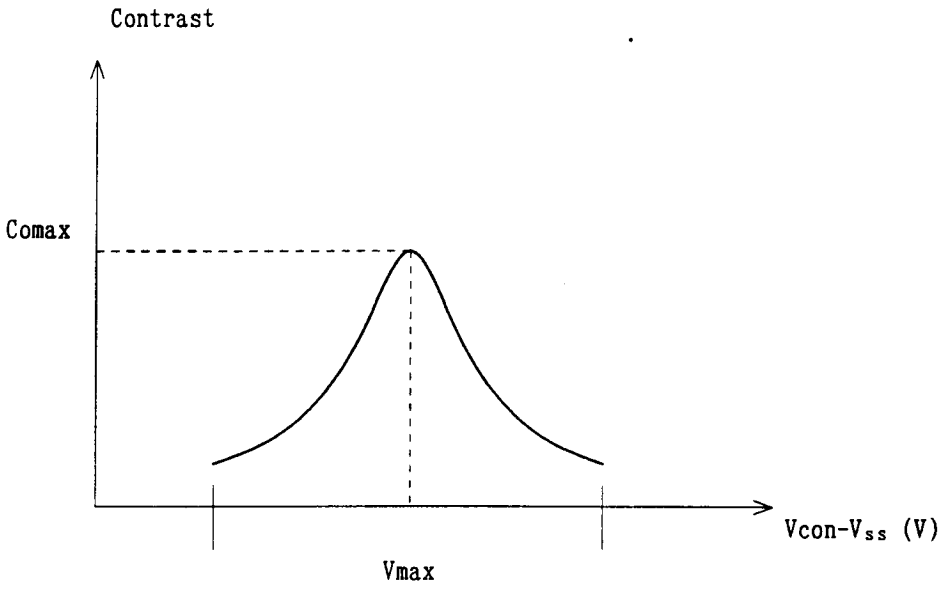


Fig. 6 Definition of V_{Max}

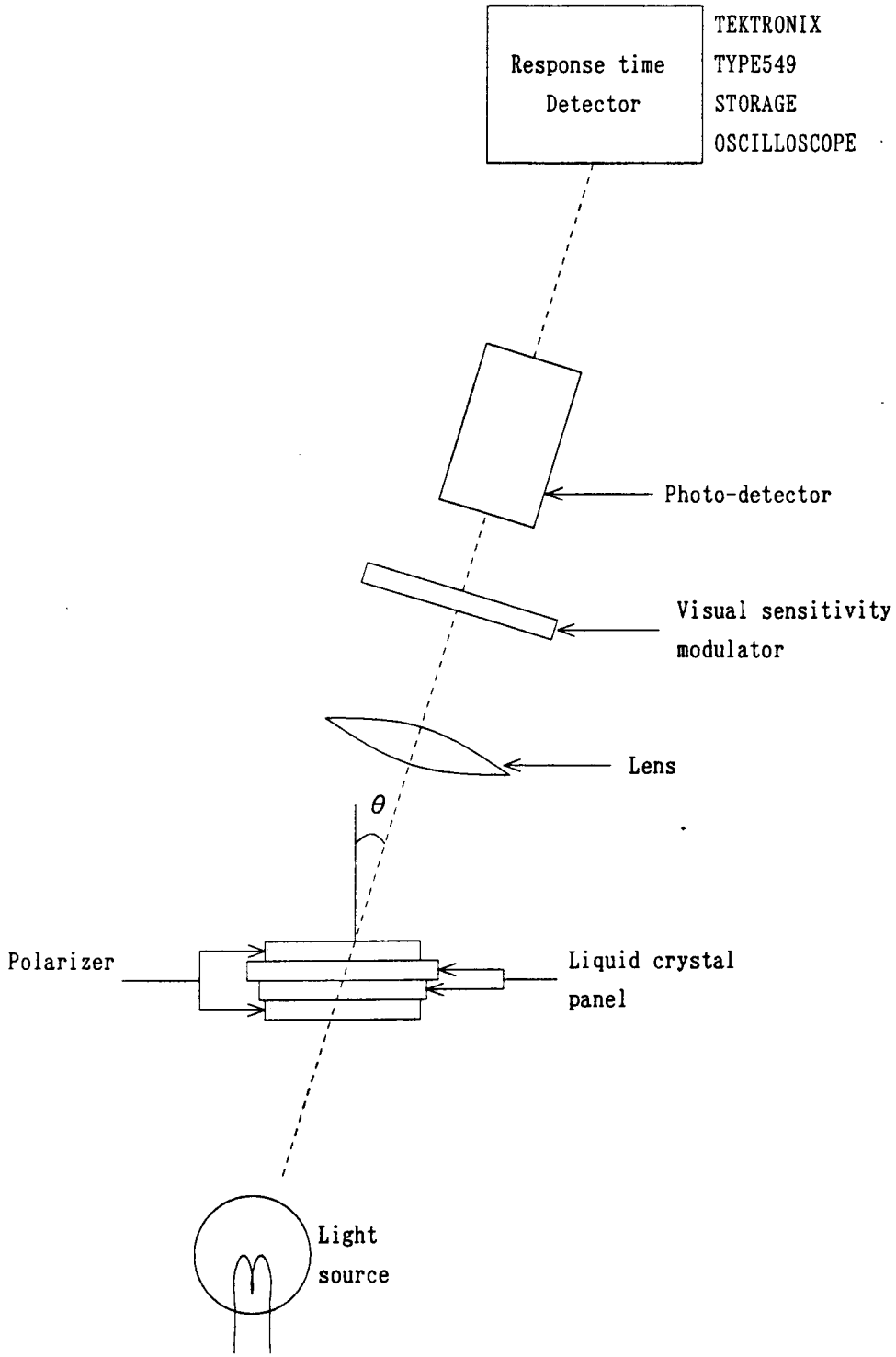
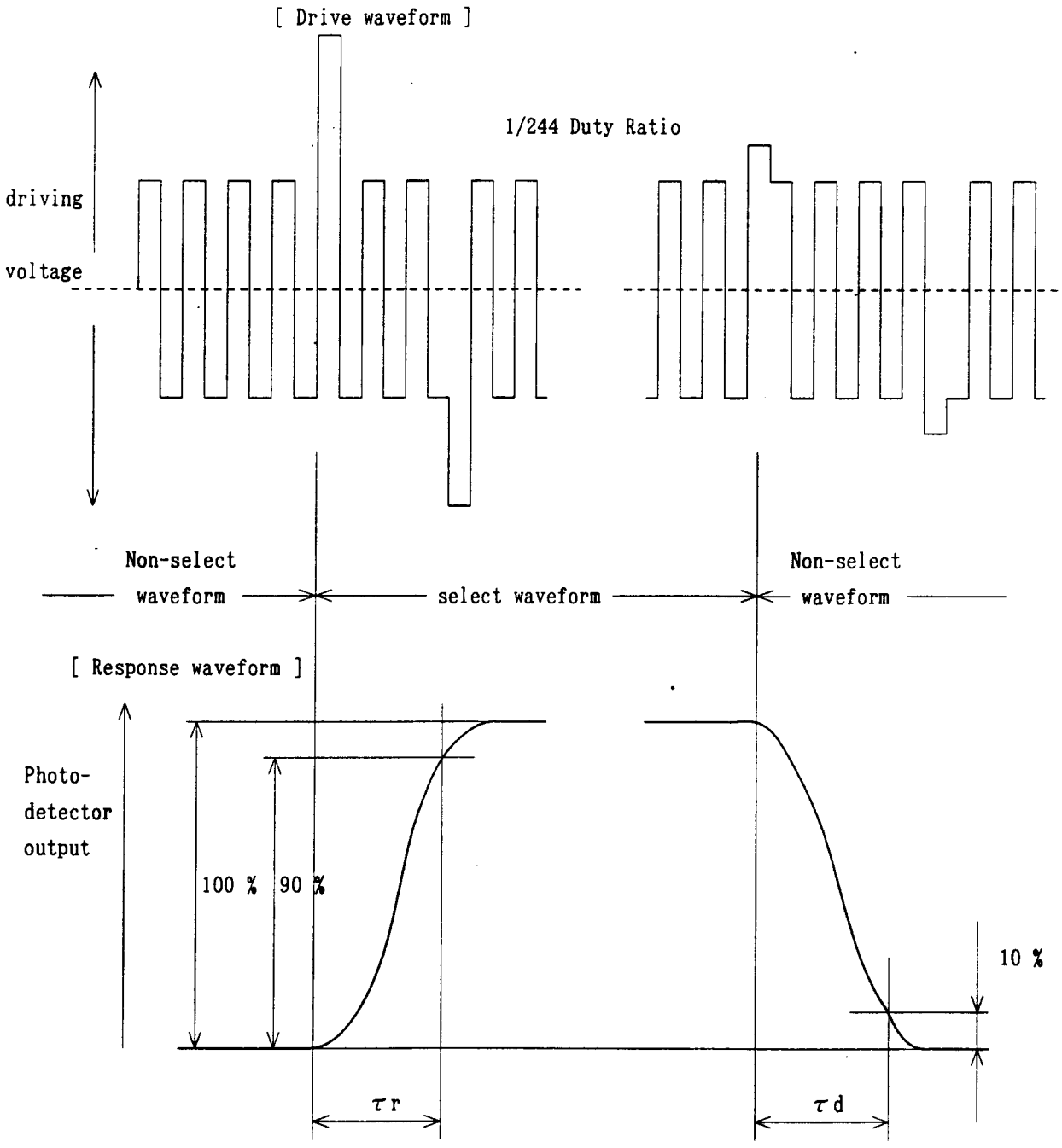


Fig.7 Optical Characteristics Test Method II



τr: Rise time

τd: Decay time

Fig.8 Definition of Response Time

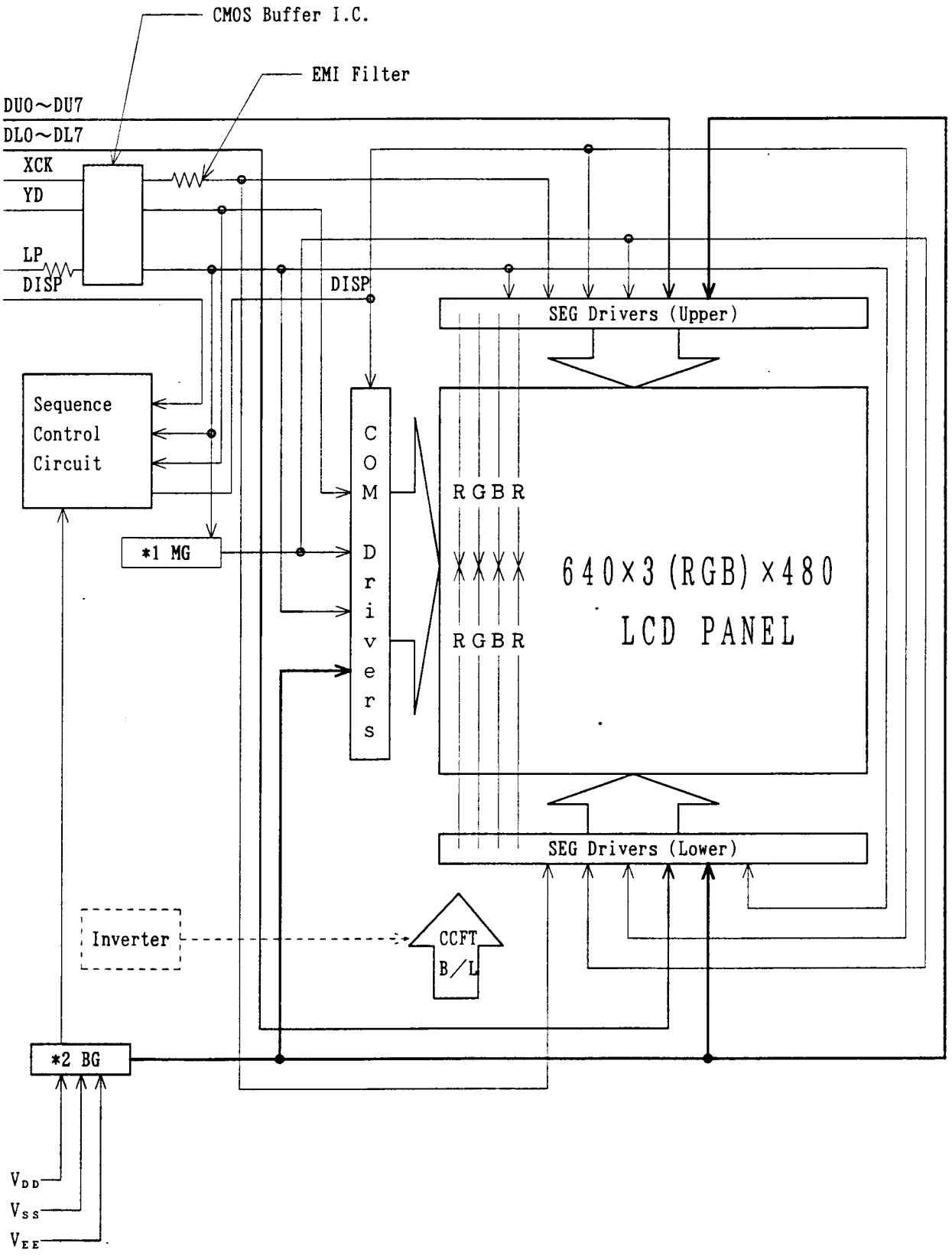


Fig.4 Circuit block diagram

*1 MG: M GENERATOR CIRCUIT

*2 BG: BIAS GENERATOR & PROTECTION CIRCUIT

8.Characteristics of Backlight

The ratings are given on condition that the following conditions are satisfied.

1) Rating (Note)

Parameter	Min	Typ	Max	Unit
Brightness	50	70	—	cd/m²

2) Measurement circuit: CXA-M10L (TDK) (at IL=5.5 mArms)

3) Measurement equipment: BM-7 (TOPCON Corporation)

4) Measurement conditions

4-1 Measurement circuit voltage: DC=10.6 V, at primary side

4-2 LCD: All digits WHITE, V_{DD}= 5 V,Vcon-Vss=Vmax,DU0～7="H"(WHITE),DL0～7="H"(WHITE)

4-3 Ambient temperature: 25 °C

Measurement shall be executed 30 minutes after turning on.

5) Used lamp: K-CE235T24E50BH (WEST ELECTRIC CO.,LTD.) : 1 pc

5-1 Rating

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp voltage	V_L	-	510	-	Vrms	—
Lamp current	I_L	-	5.5	-	mArms	(*1)
Lamp power consumption	P_L	-	2.8	-	W	(*2)
Lamp frequency	F_L	20	-	70	kHz	—
Kick-off voltage	V_S	-	-	760	Vrms	Ta=25 °C
		-	-	1 300	Vrms	Ta=0 °C(*3)
⚠2 Lamp life time	L_L	15 000	25 000	-	h	(*4)

Within no conductor closed. (CCFT only)

(*1) It is recommended that IL be not more than 5.5 mArms so that heat radiation of CCFT backlight may least affect the display quality.

(*2) Power consumption excluded inverter loss.

(*3) The circuit voltage(V_S) of the inverter should be designed to have some margin,because VS may be increased due to the leak current in case of the LCD module.

⚠2(*4) The Lamp life time(L_L) is 15 000 hours at 5.5 mArms.

5-2 Operating life

⚠2The operating life time is 15 000 hours or more at 5.5 mArms.

(Operating life with CXA-M10L or equivalent.)

The inverter should meet the following conditions to keep the specified life time of used lamp;

-Sine, symmetric waveform without spike in positive and negative.

-Output frequency range: 20 KHz～70 KHz

Make sure the operating conditions by executing the burn-in enough time.

The operating life time is defined as having ended when any of the following conditions occur; 25±1 ℃

-When the voltage required for initial discharge has reached 110 % of the initial value

-When the illuminence or quantity of light has decreased to 60 % of the initial value

(NOTE) Rating are defined as the average brightness inside the viewing area specified in Fig.11.

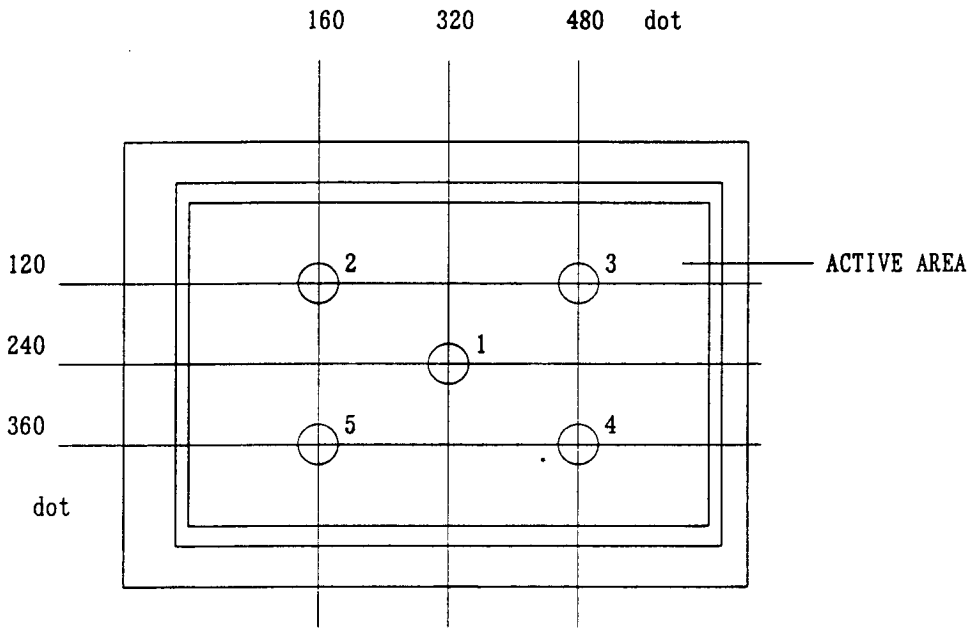


Fig.11 Measureing points (1~5)

9. Precautions

1) Industrial (Mechanical)design of the product in which this LCD module will be incorporated must be made that the viewing angle characteristics of the LCD may be optimized.

This module's viewing angle is illustrated in Fig.12.

θy MIN < viewing angle < θy MAX

(For the specific values of θymin. θymax. refer to the table 9.)

Please consider the optimum viewing conditions according to the purpose when installing the module.

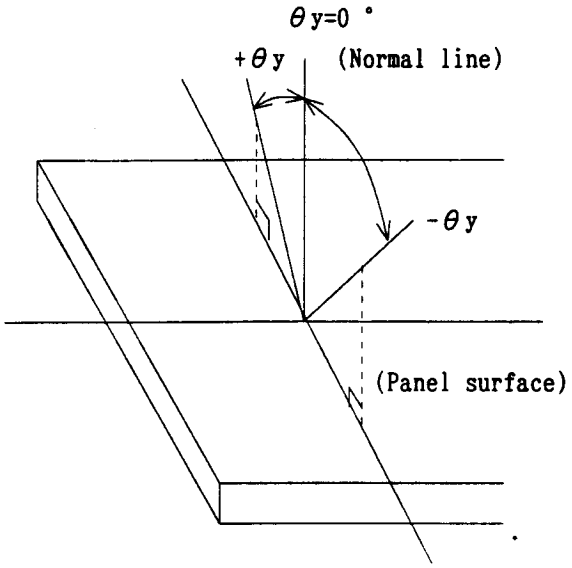


Fig.12 Dot matrix LCD viewing angle

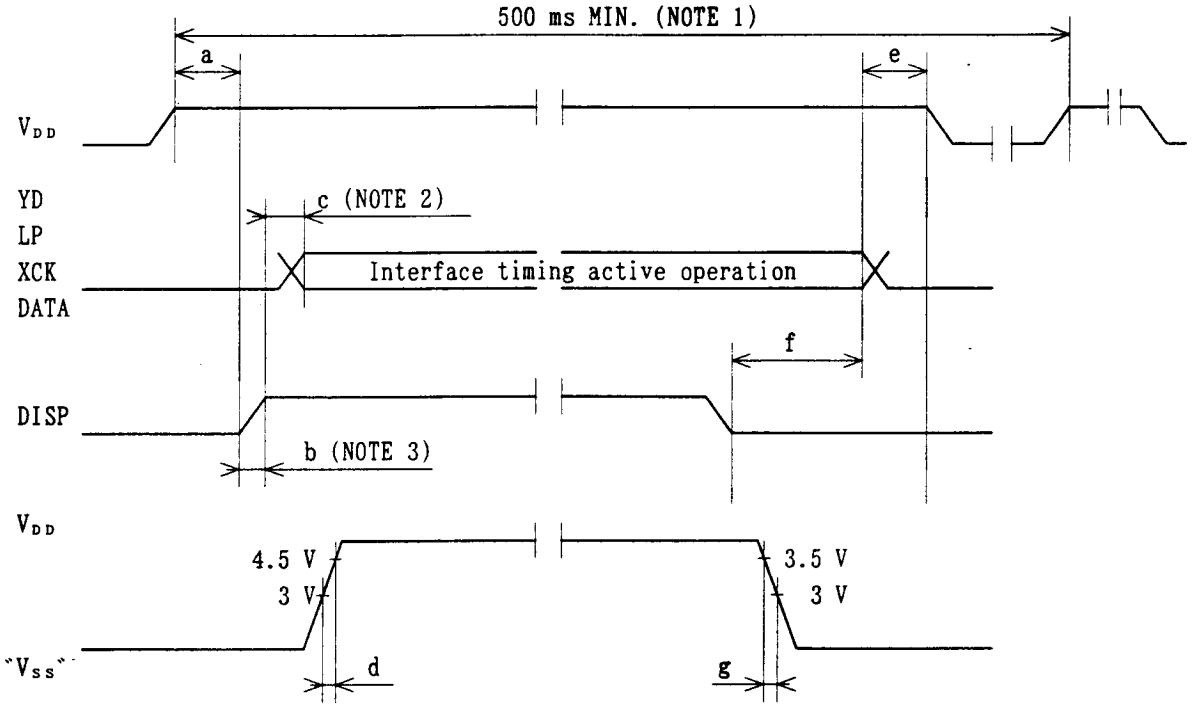
2) This module is installed using mounting holes metal PBC or bezel.

When installing the module, pay attention and handle carefully not to allow any undue stress such as twist or bend.

A transparent acrylic resin board or other type of protective panel should be attached to the front of the module to protect the polarizer, LCD cells,etc.

3) Since the front polarizer is easily damaged. Please pay attention not to scratch on its face.
4) If the surface of the LCD cells needs to be cleaned, wipe it swiftly with cotton or other soft cloth. If still not completely clear, blow on its and wipe.
5) Water droplets, etc, must be wiped off immediately since they may cause color changes, staining, etc, if remained for a long time.
6) Since LCD is made of glass plates, dropping the module or banging it against hard objects may cause cracking or fragmentation.
7) CMOS LSIs are equipped in this module, so care must be taken to avoid the electro static charge, by earthing human body, etc. Take the following measures, to protect the module from the electric discharge via mounting tabs from the main system the electrified with static electricity.
   (1) Earth the metallic case of the main system (contact of the module and main system).
   (2) Insulate the module and main system by attaching insulating washers made of bakelite or nylon,etc.
8) The module should be driven according to the specified ratings to avoid malfunction of parmanent damage. DC voltage drive leads to rapid deterioration of LC, so ensure that the drive is alternating waveform by continuous application of the signal M. Especially the power ON/OFF sequence shown on next page is strongly recommended to avoid latch-up of drive LSIs and application of DC voltage to LCD panel.
9) Since leakage current, which may be caused by routing of CCFT cables,etc., may affect the brightness of the display, the inverter has to be designed taking the leakage current into consideration. Thorough evaluation of the LCD module/inverter built into its host equipment shall be conducted, therefore, to ensure the specified brightness.
10) Avoid to expose the module to the direct sun-light, strong ultraviolet light, etc. for a long time.
11) If stored at temperatures below specified storage temperature, the LC may freeze and be deteriorated. If storage temperature exceed the specified rating. the molecular orientation of the LC may change to that of a liquid, and they may not revert to their original state. As for as possible always store at normal room temperature.
12) Disassembling the LCD module can cause permanent damege and should be strictly avoided.

Supplt voltage sequence condition



POWER ON		
SYMBOL	Allowable value	
a	0 ms MIN.	1 s MAX.
b	—	100 ns MAX.
c	50 ms MIN.	—
d	—	25 ms MAX.

POWER OFF		
SYMBOL	Allowable value	
e	0 ms MIN.	1 s MAX.
f	0 ms MIN.	1 s MAX.
g	1 ms MIN.	—

(NOTE 1) Power ON/OFF cycle time. All signals and power line shall be in accordance with above sequence in case of power ON/OFF.

(NOTE 2) In this period, YD and LP shall be "L" level.

(NOTE 3) Except V_{DD}=DISP.

9. Applicable inspection standard

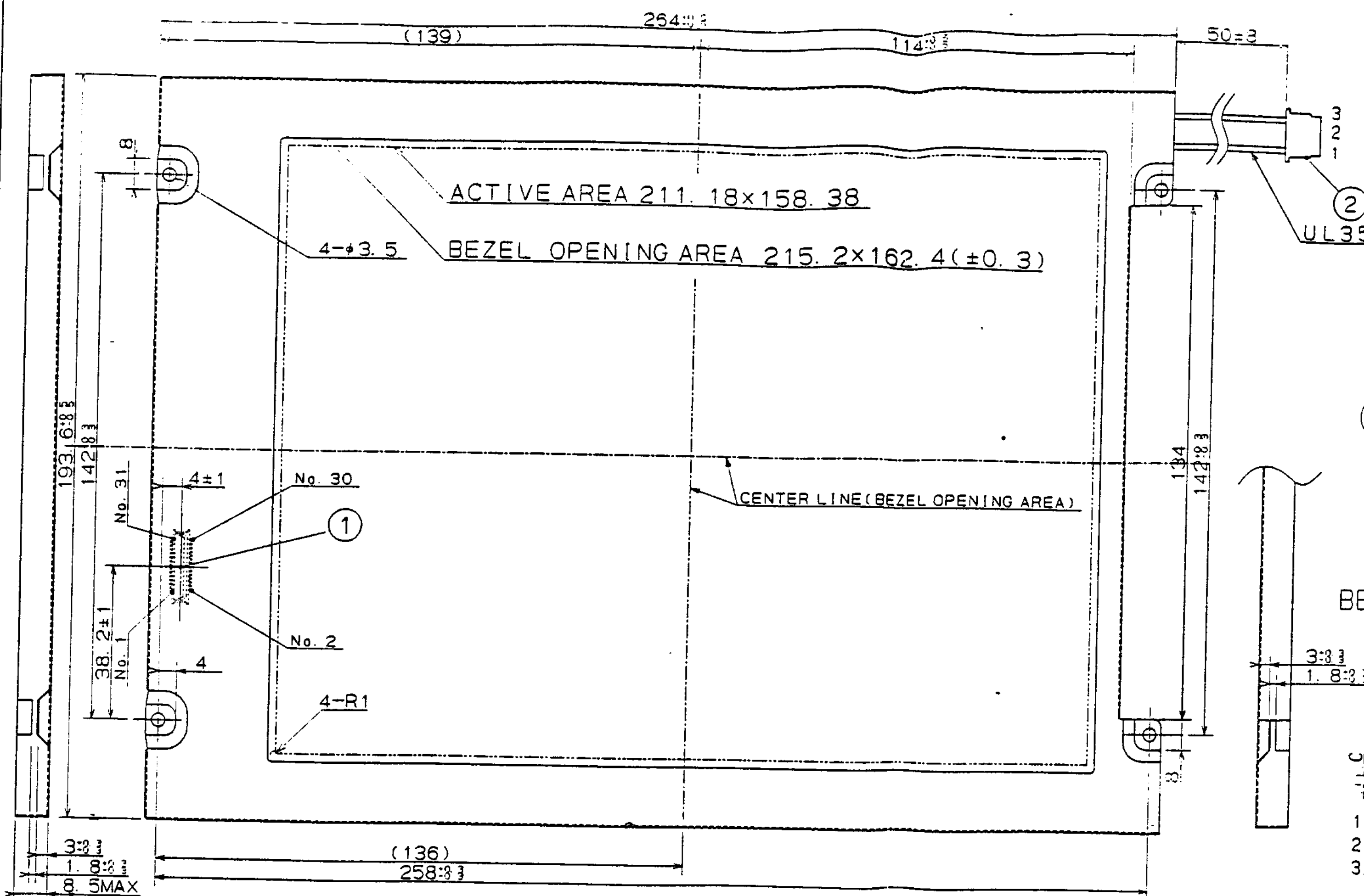
The LCD module shall meet the following inspection standard

:S-U-014

10. This specification describes display quality in case of no gray scale. Since display quality can be affected by gray scale methods, display quality shall be carefully evaluated for the usability of the LCD MODULE in case gray scale is displayed on the LCD MODULE.

WARNING

DON'T USE ANY MATERIALS WHICH EMIT FOLLOWING GAS FROM EPOXY RESIN (AMINES' HARDENER) AND SILICONE ADHESIVE AGENT (DEALCOHOL OR DEOXYM) TO PREVENT CHANGE POLORIZER COLOR OWING TO GAS.



Excluded the allowance of deformation

(1) INTERFACE CONNECTOR

DF9B-31P-1V(HIROSE)

<PIN LAYOUT>

PIN#	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	DL4	VSS	DL5	Y0	DL6	LP	DL7	VSS	VSS	XCK	DL0	VCON	DL1	VDD	VSS
	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	VDD	DL2	DISP	DL3	NC	VSS	DU3	DU4	DU2	DU5	DU1	VSS	DU0	DU6	VSS	DU7

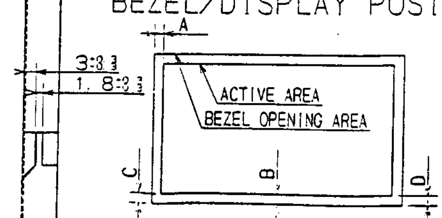
(2) CCFT CONNECTOR

BHR-03VS-1(JST)

<PIN LAYOUT>

PIN#	1	2	3
	HV	NC	GND

BEZEL/DISPLAY POSITION



1) TOLERANCE X-DIRECTION A:2. 0±0. 8
2) TOLERANCE Y-DIRECTION B:2. 0±0. 8
3) OBLIQUITY OF DISPLAY AREA |C-D|<0. 8

指示なき寸法公差は UNSPECIFIED TOL. TO BE ±0.5

出図	設計通知 DRAWING INFO No	通知書 INFORMATION 書による	
新設 NEW	変更 CHANGE	差換 REPLACE	図面

機種 MODEL	LM10V33
名称 NAME	LCD MODULE OUTLINE DIMENSIONS
記号 SYMBOL	640xRGBx480 P0. 33
部品コード PARTS CODE	
作成日付 DATE	1996 · 11 · 21 ·
図番 DRAWING No.	0D10V33080 1 1

年月日 DATE / 改定記事 REVISE / 認番 No / 担当 PREPA / 材質 MATERIAL / 厚さ THICKNESS / 仕上 FINISH / 尺度 SCALE

設計 DESIGN / 製図 TRACE / 検図 CHECK / 検認 CHECK / 承認 APPROVE

城山 / 小羽田

SHARP CORPORATION

シャープ株式会社 液晶事業本部（事本）

発行部門 デューティー開発センター第2技術部

CSTN, low cost, low cost display, 10.4 inch, wide operating temperature, LM10V33