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Photon Vision Systems

High Performance Linear CMOS Image Sensors
LIS-XXXX Family
LIS-128, LIS-512, LIS-1024

The Photon Vision Systems LIS series is a family of high performance linear image sensors designed for a wide variety of applications as a superior CCD replacement, including:

Edge Detection
Contact Imaging
Bar Code Reading
Encoding and Positioning
Text Recognition

Description

The LIS-XXXX family of Linear Image Sensors consists of an array of low dark current photo-diode pixels with performance exceeding most Charge-Coupled Devices (CCD's). The device has multiple read out modes, including Dynamic Pixel Reset™ or DPR, Frame Reset, and non-destructive. In DPR mode, each pixel is reset as it is read, guaranteeing each pixel integrates for the same amount of time, making the LIS series ideal for continuous illumination as well as strobed applications. Other reset modes are also provided to give exceptional control over exposure time and pixel read out. A key feature when compared with traditional CCD technology is that the device can be read and reread Non-Destructively, allowing the user to maximize signal to noise and dynamic range. The Sensor also operates over an extended power supply range of 2.8-5.0 VDC.

Operation is simplified by on-chip logic. The only external signals required are a clock with a frequency equal to the desired pixel read rate, a reset mode selection, and an external reset to initiate read-out when running asynchronously.

The LIS-XXXX series is supplied in 8-pin PHOTO-DIP™ package, or 16-pin LCC package.

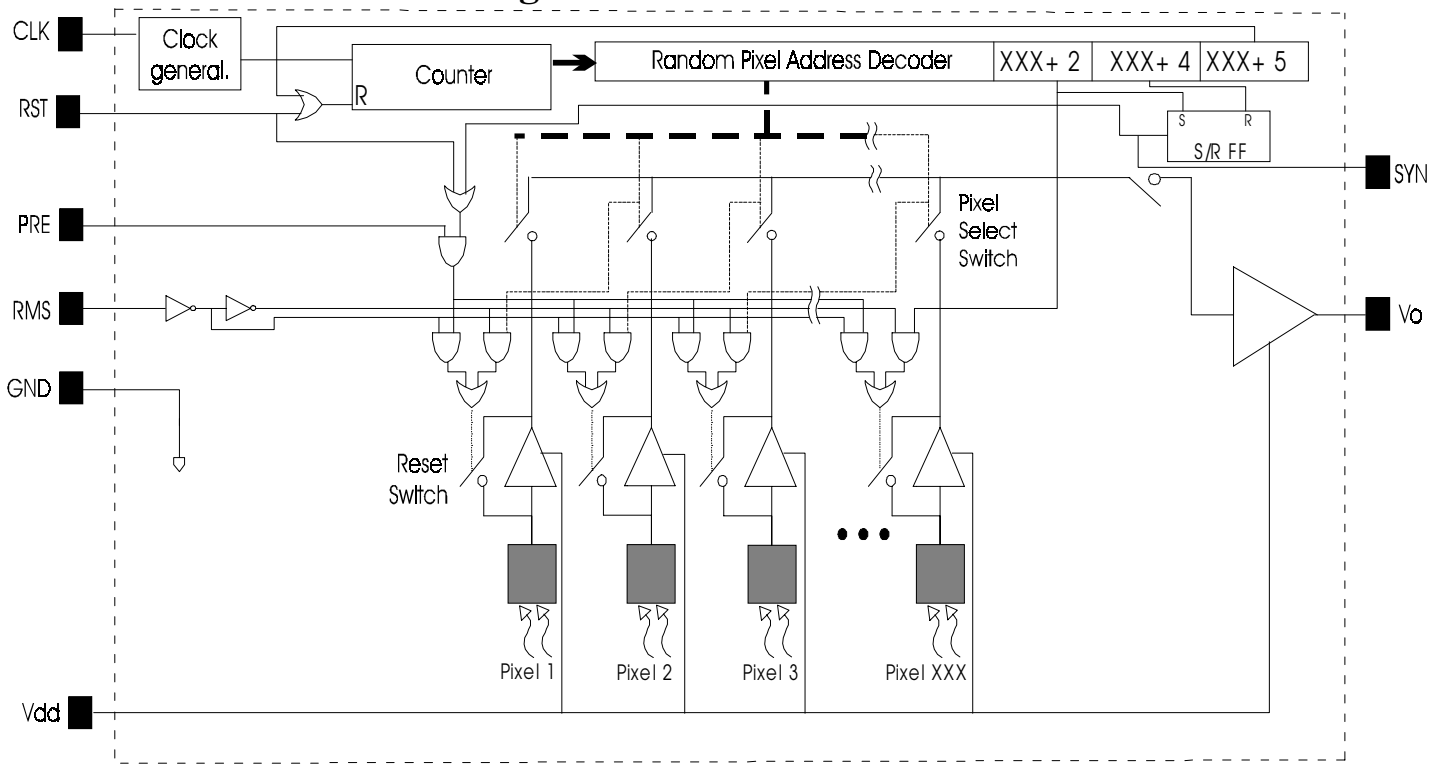
Key Features

- Low Cost
- Single Supply Operation
- Multiple read out modes
- High Signal to Noise
- Non-Destructive read capable
- 1.0 kHz to 20.0 MHz Operation
- Very Low Dark Current
- Completely integrated Timing and Control
- Replaces CCD systems, not just the sensor

MODEL	ARRAY SIZE	PIXEL SIZE h x w(pitch)
LIS-128	1 x 128	125u X 62.5u
LIS-512	1 x 512	125u X 15.6u
LIS-1024	1 x 1024	125u X 7.8u

Array length is 7.988 mm for all devices.
See Mechanical Dimension for Die layout.

Functional Block Diagram



Electrical Characteristics/Operating Conditions

Parameter	Min	Typical	Max	Units
Supply Voltage (see note 5)	2.50	5.0	5.25	V
Supply Current (see note 1)	8	18	50	mA
Input High Logic Level	VDD –0.6V			V
Input Low Logic Level			0.6	V
Clock Frequency/Pixel Read Rate (see note 3)	1.0	1000	20,000	kHz
External Load	330		10k	Ohms
Output Voltage at Saturation (see note 5)	2.8	3.3	4.0	V
Output Voltage at Dark	0.64	0.74	0.84	V
Pixel Non-Uniformity Dark		±0.5		%
Linearity (see note2)		1.0		%
Output due to Dark Current (see note 4)	2	19	38	mV/s
Relative Humidity	0		90	%
Operating Temperature	0	25	50	°C

Parameter	LIS-128	LIS-512	LIS-1024	UNITS
Sensitivity (note 7)	0.039	0.16	0.32	µv/e-
Full Well	6.5	1.6	0.8	Me-
Signal/Noise (RMS) (see note 6)	>93	>87	>84	db

Notes
1. Including Load Resistor
2. Pixel average from 5% - 75% Saturation
3. Specs. given at pixel read rates of 2.5 MHz for LIS-128, 1 MHz for LIS-512, and 1 Mhz for LIS-1024. At greater read rates, MTF and S/N begin to degrade.
4. At 24 °C.
5. At Supply voltages less than Saturation Voltage, Vo is clipped by supply, no load applied.
6. Temporal rms noise @ 1 Mhz erc and 500khz video band width filter applied, values are typical and may vary. Higher S/N ratios are obtainable with lower erc and bandwidths.
7. Unloaded video, values are typical and may vary.

Absolute maximum ratings, T_A = 25°C unless otherwise noted, see Note 1, below. †

Supply voltage range, V_{DD}---------- 0 V to 5.25 V
Digital input current range, I ---------- –20 mA to 20 mA
Operating case temperature range, T_C (see Note 2)---------- –10°C to 70°
Operating free-air temperature range, T_A ---------- 0°C to 50°C
Storage temperature range ---------- –20°C to 85°C
Humidity range, Rh ---------- 0-100%, non-condensing
Lead temperature 1.5 mm (0.06 inch) from case for 10 seconds----- 255°C

† Exceeding the ranges specified under "absolute maximum ratings" can damage the device. The values given are for stress ratings only. Operation of the device at conditions other than those indicated under "recommended operating conditions" is not implied. Exposing the device to absolute maximum rated conditions for extended periods may affect device reliability and performance.
NOTES: 1. Voltage values are with respect to the device GND terminal.
2. Case temperature is defined as the surface temperature of the package measured directly over the integrated circuit.

SIGNAL DESCRIPTION & PACKAGE PINOUT

Signal	I/O type	Definition	8 Pin DIP	16 Lead LCC
GND	-----	Ground Reference.	1	1
CLK	Input	Clock	2	3
PRE	Input	Pixel Reset Enable	3	5
RMS	Input	Reset Mode Select	4	7
RST	Input	External Reset/Start pixel read	5	10
VO	Output	Video Output	6	12
SYN	Output	Synch Output	7	14
Vdd	Input	Supply Voltage	8	16

OPERATION AND TIMING

The device offers multiple modes of operation including:

- Dynamic Pixel Reset™ (DPR) Mode, where each pixel is reset after reading,
- Sequential Read Non-Destructive Mode, where each pixel is allowed to integrate even after reading,
- Frame Mode with Destructive Read, where all pixels are reset all at once
- Frame Mode with Non-Destructive Read, where all pixels were originally reset at once and allowed to integrate after reading.

Example timing diagrams are given below. The user selects which mode of operation by selecting logic levels for the PRE (Pixel Reset Enable) pin and the RMS (Reset Mode Select) pin. The device requires a clock frequency equal to the desired pixel read rate. In frame mode, a read cycle is initiated by pulsing the RST pin. See the truth table below for all modes of operation.

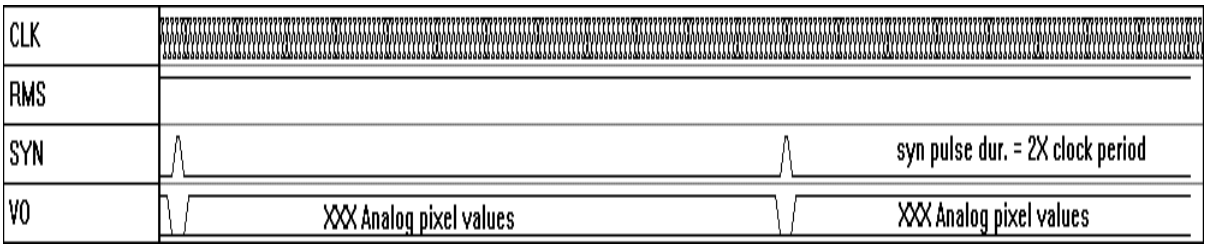
In all modes, the end of each frame is identified with a pulse being output on the SYN pin. This SYN pulse will begin on the rising edge of the XXX+2 clock cycle for that frame, XXX being the number of pixels in the device. The SYN pulse goes low on the rising edge of the XXX+4 clock. In sequential read mode, the internal counter is reset on the rising edge of the XXX+5 clock.

NOTES TO TIMING DIAGRAMS

1. Clock duty cycle should be 50%.
2. XXX Clock cycles for the number of pixels to read, starting at the first pixel.
3. t int represents integration time.
4. RST pulse always resets internal counter, thus next pixel output is the first pixel.

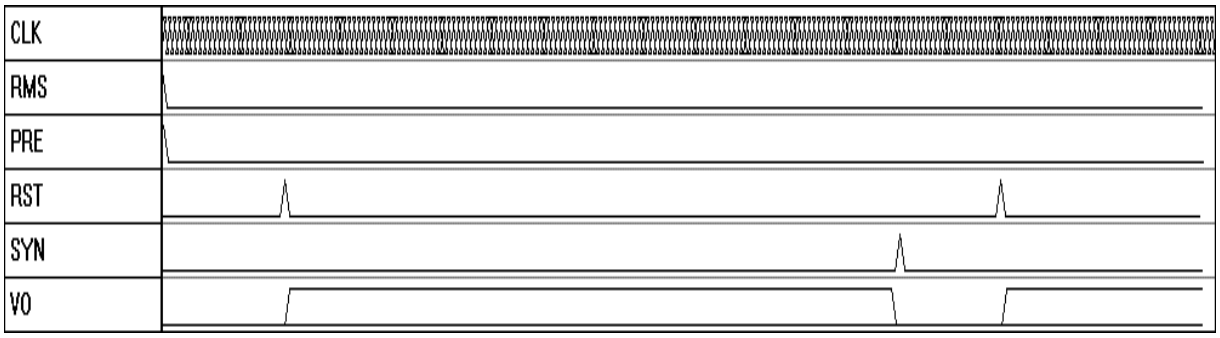
DYNAMIC PIXEL RESET (DPR) MODE.

In this mode, pixels are reset as they are sequentially read. This assures identical integration time for each pixel. Clock must run for XXX+5 clock cycles for internal counter to reset if relying on the internal logic, or the user can reset externally. See Reset Mode Truth Table below for more details. Clock can continue or go low after the XXX+5 cycle. The pixel integration time in this mode is equal to the clock period times 4 + number of pixels in the device. The device will operate well at speeds to 12 MHz, at speeds faster than this, DPR™ mode of operation is not recommended, but instead choose one of the frame modes. Note that the last pixel in DPR™ mode is invalid, unless it reset by switching modes at the end of the frame.



Note: Sequential read continues as long as clock runs. To disable internal pixel reset (DPR) for continuous integration (Sequential Read Non-Destructive Mode), connect the RMS pin to ground. With DPR disabled, pulsing the RST pin will reset the pixels.

FRAME MODE - NON-DESTRUCTIVE READ



In this mode, the RST pulse resets the internal counter, and the video out is set to read the first pixel. Because the PRE line is held low, the pixels are not reset, and the image is preserved.

FRAME MODE - DESTRUCTIVE READ.

The timing for Frame Mode - Non Destructive read applies, except that taking the PRE line high will cause the pixels to be reset when the RST pin goes high. This mode is ideal for Strobe applications.

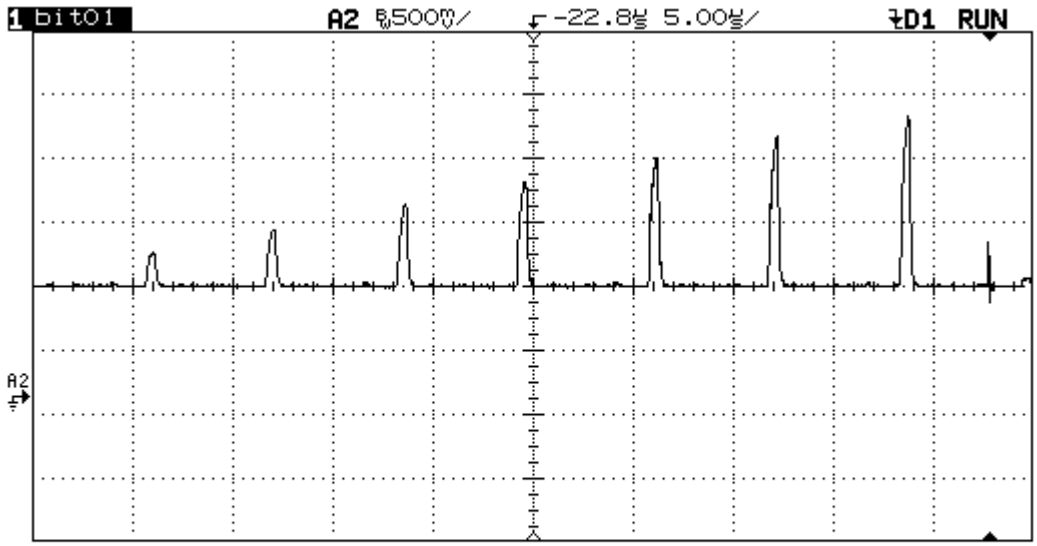
RESET MODE TRUTH TABLE:

The following truth table summarizes the various reset modes, and readout modes.

MODE	RST	RMS	PRE	PIXEL RESET OR INTEGRATING	COUNTER RESET OR NORMAL	NOTES
0	0	0	0	INTEGRATING	NORMAL	Frame mode, continuous integration.
1	0	0	1	ALL PIX. RESET	NORMAL	Frame mode, all pixels reset.
2	0	1	X	DPR RESET	NORMAL	DPR mode, previous pixel reset
3	1	0	0	INTEGRATING	RESET	External reset, frame mode, continuous integration
4	1	0	1	ALL PIX. RESET	RESET	External reset, frame mode, all pixels reset
5	1	1	X	DPR RESET	RESET	External reset, DPR mode, previous pixel reset

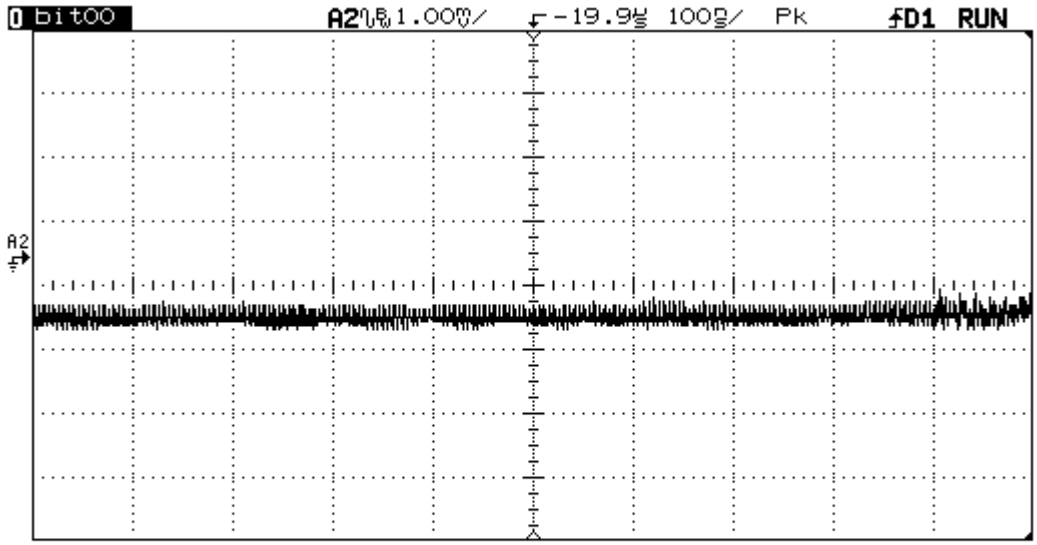
0 = Logic 0, 1 = Logic 1, X = Don't Care

Example Output Traces.

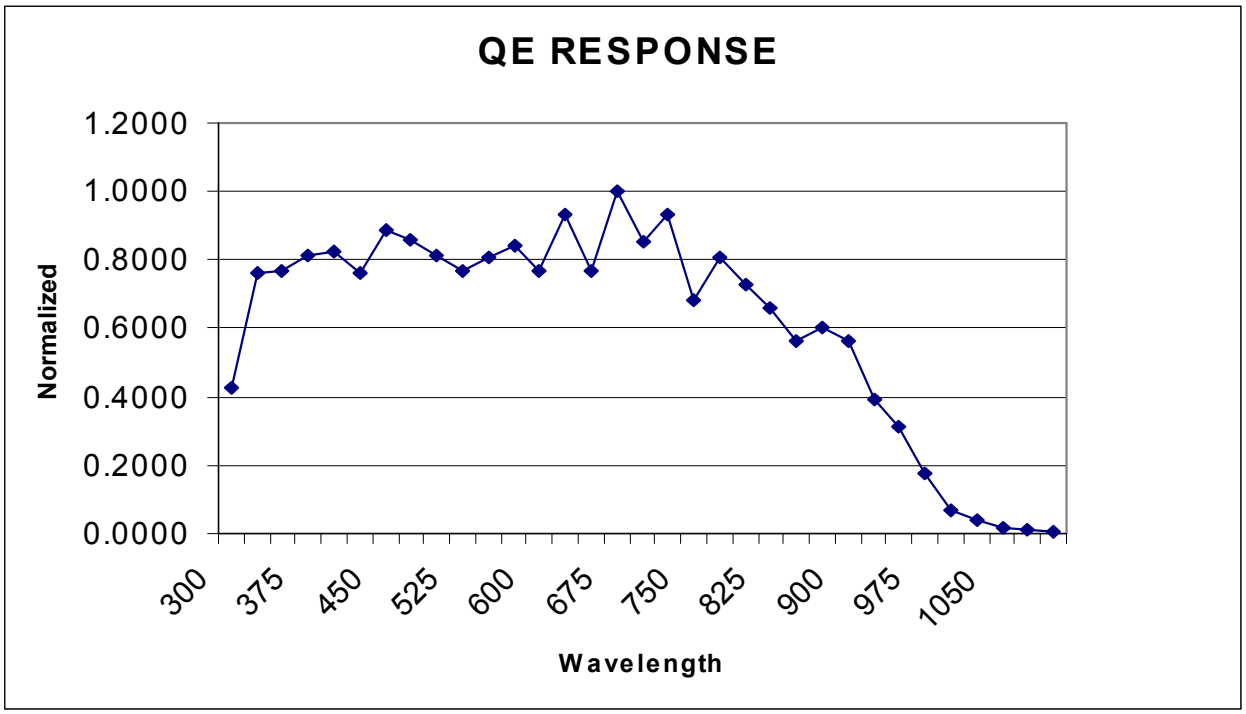


LIS-128 running at 40Mhz pixel read rate or 148,000 frames/sec.
Illustrates non destructive read for seven frames.

Test Set-up – A dim spot light illuminating about 25. pixels of LIS-128 , while disabling pixel reset for non-destructive read.



LIS-128 analog scope trace with scope probe AC coupled. Output showing peak to peak noise levels of 400 µV at full dark. Illustrates peak signal to RMS noise (S/N) well in excess of 90db.



Note: Data below 350nm not measured, but device is sensitive to 200 nm. Shown for un-encapsulated device.

MECHANICAL DIMENSIONS

For 8 pin dip package see drawing: 40066

For LCC package see drawing: 40068

See pages 8 & 9 for optical position information

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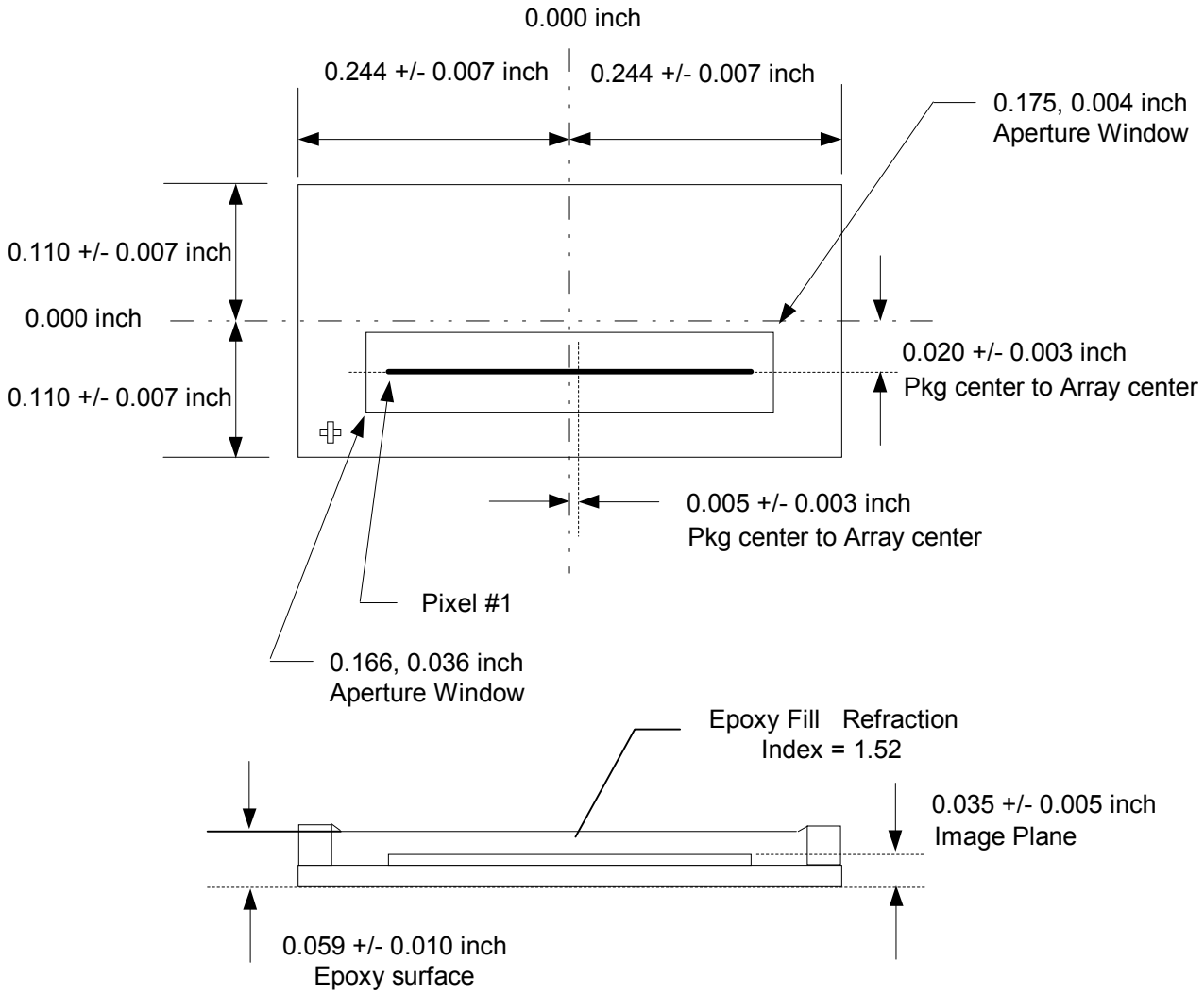
Optical Design guide
LIS-xxxx in 16 Pad LCC



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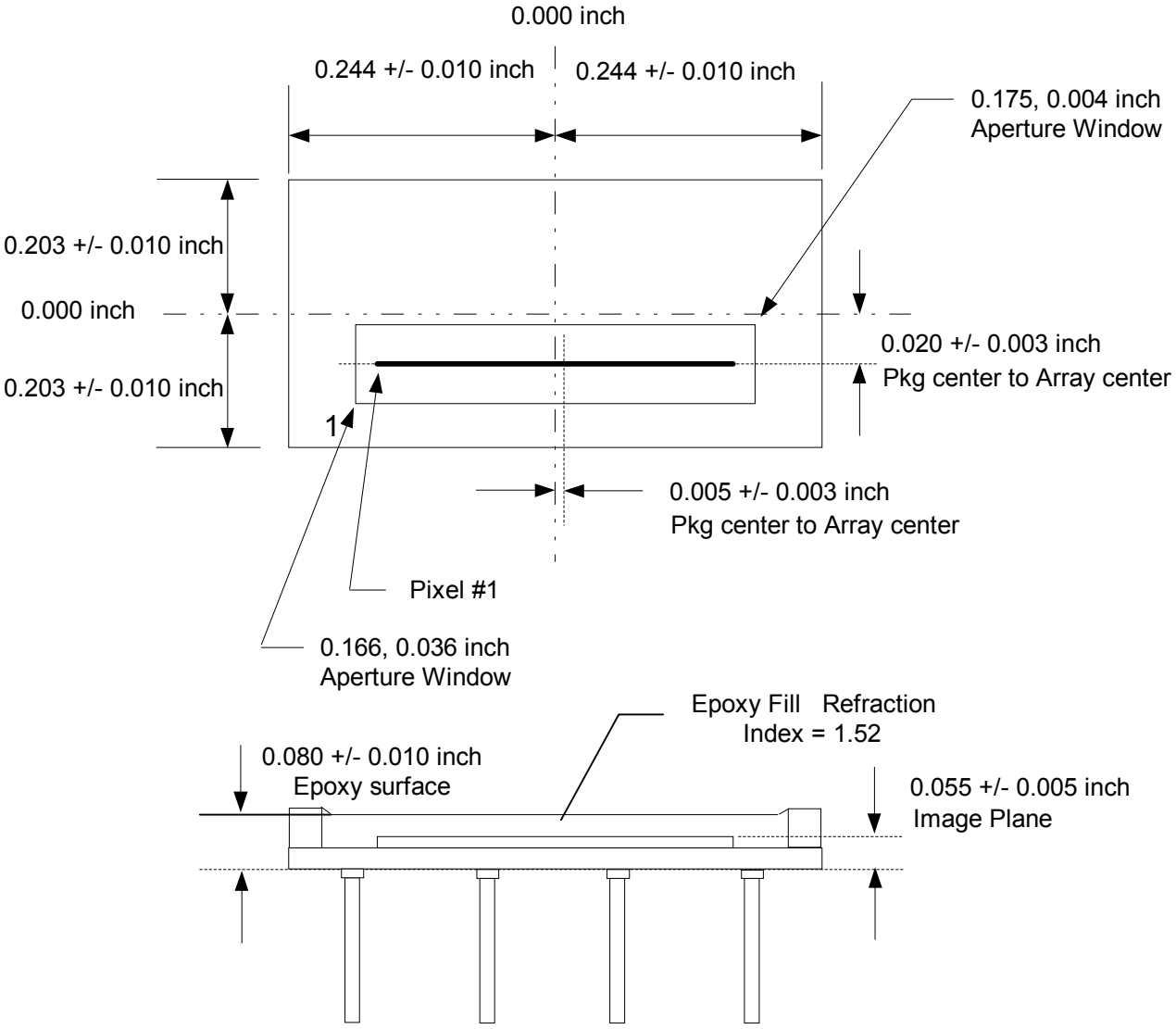
Optical Design guide
LIS-xxxx in 8 Pin DIP



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This imager may be covered under the following patent: 6,084,229