CMOS IC

LC58F7416

4-Bit Single Chip Microcontroller

UnderDevelopment

LC58F7416

CMOS LSI

LCD Driver　RAM 512 × 4-bit

Flash ROM (on-board rewrite possible) 16K × 16-bit

4-bit single chip microcontroller

Overview

The LC58F7416 microcontroller has a CPU (enables functions with the low-voltage) as a core and is the CMOS 4-bit microcontrollers with 512 × 4-bit RAM, 16K × 16-bit Flash ROM, stack-only RAM(8 levels), 8-bit AD × 4 ch, 8-bit timer × 2 channels (one used as an event counter), 8-bit synchronous serial interface,the alarm signal generation circuit, remote control carrier generation circuit, LCD controller and driver, and powerful stand-by function (power-saving function) all mounted as one chip.

Usage

- Functions for handy materials with LCD function (suitable for applications of low-power battery consumption)
- Portable CD, timer, health control and management machine control and LCD display
- Remote controllers for the CD, VTR, tuners.

SANYO Electric Co.,Ltd. Semiconductor Company
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Features

1. ROM

   • LC58 F 7416A (16384 ×16-bit)

   (sharing 2K worth space of 14K-16K ROM space with the self-rewrite possible ROM)

2. RAM

   • LC58F7416 (512 × 4-bit)

3. Instruction Cycle Time

   Instructions (excluding TABLE-Reference instruction) execute their transactions with one cycle.

Cycle Time	Power Voltage	System Clock Oscillation	Oscillation Frequency
1 μs	4.5-5.5V	CF (Ceramic) Oscillation	4MHz
4 μs	4.5-5.5V	CF (Ceramic) Oscillation	1MHz
10 μs	4.5-5.5V	CF (Ceramic) Oscillation	400kHz
122 μs	3.0-5.5V	X'tal (crystal) Oscillation	32.768kHz

4. Ports

   INPUT-Only Pin

   • Port S (4 pins)

   • INT pin (1 pin)

   IN/OUT pin

   • Port K (4 pins) Output type is fixed at CMOS

   • Port M (4 pins) Output type can be programmed at CMOS or Pch with every port.
   (M4 pin is set as the signal input pin when Timer 2 is in the event counter mode)

   • Port SO (4 pins) Output type can be programmed at CMOS or Nch with every port.
   (Pins for SO1, SO2, SO3 are shared with the serial interface.2-pin serial possible)

   • Port P (4 pins) Output type can be programmed at CMOS or Pch with every port.

   OUTPUT-Only Pin

   • Port N (4 pins) N3 pin is shared with the remote control carrier outputs.
   N4 is shared with the alarm output too.

   LCD Driver pin

   • Common pin (4 pins)

   • Segment Pin (23 pins)

   Every segment pin has the segment memory used only to store the output data. The output format can be changed from the LCD driver output format to the general output formats (CMOS, Pch, Nch) by program.

5. Various LCD driving types

LCD Drive Type	Number of segment drivable	Required common pins
1/3 bias, 1/4 duty	92 Segments	COM1 - COM4
1/3 bias, 1/3 duty	69 Segments	COM1 - COM3
1/2 bias, 1/4 duty	92 Segments	COM1 - COM4
1/2 bias, 1/3 duty	69 Segments	COM1 - COM3
DUPLEX	46 Segments	COM1 , COM2
STATIC	23 Segments	COM1

6. Timers

Timer 1

- 6-bit prescaler + 8-bit programmable reload timer (prescaler shared with Timer 1, Timer2, serial interface)
- Can be programmed to generate the remote controller carrier signal

Timer 2

- 6-bit prescaler + 8-bit programmable timer (prescaler shared with Timer 1, Timer2, serial interface)
- Used as an event counter

Base Timer (when 32.768kHz X'tal Oscillation is selected)

- Flexible for the application as two types can be chosen from the 2 types of the basic signal (125ms/500ms or 250ms/1000ms) with the combination of the program.

7. Stand-by Functions

HALT mode

- This halts an instruction. The oscillation circuit, timer, LCD controller and driver, serial interface continue their operations. This also deletes unnecessary loops. The low-power consumption is achieved with utilizing this HALT mode.
- Release conditions for this mode can be set by program. The followings are the functions that can be used for releasing this HALT mode.
    a) INT pin signal change (1 source)
    b) Timer 1 (1 source)
    c) Timer 2 (1 source)
    d) Base Timer (1 source)
    e) Serial interface or SO4 pin signal change (either one)
    f) Signal changes at Port S and K which are defined with SSW instruction (8 sources)
    g) Reset signal

HOLD mode

- Stand-by mode where oscillation circuit stops completely.
- Release conditions for this mode can be set by program. The followings are the functions that can be used
    a) INT pin signal change (1 source)
    b) Timer 2 event counter mode (1 source)
    c) Serial interface or SO4 pin signal change (either one)
    d) Signal changes at Port S and K which are defined with SSW instruction (8 sources)

e) Reset signal

8. Interrupt Functions (5 sources with 4 vector addresses)
   a) INT pin signal change (1 source)
   b) Timer 1 (1 source)
   c) Timer 2 (1 source)
   d) Serial interface or SO4 pin signal change (either one)

9. Watchdog Timer
   16-bit counter type. This can be reset at two different points so that it can be flexible for application use.
   Watchdog timer operation time example
   For the X'tal oscillation (32.768kHz, 1 or 2 oscillations) : 2000ms (Max)
   For the CF oscillation (1MHz, 1 oscillation) : 65.536ms (Max)

10. Sub-routine Stack
    This has 8-level RAM for the use of stack. Therefore, the data RAM is not wasted when escaping to the program counter.

11. Number of instructions
    Useful instructions of 130 types (the accumulator manipulation, transfer between the register memory, arithmetic calculation, flag manipulation, IN/OUT port manipulation, conditional branch instructions etc) are available.

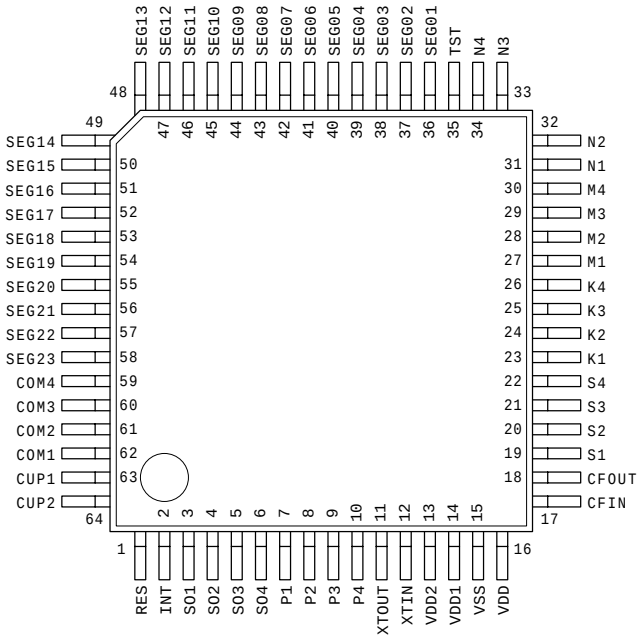
12. Oscillation Circuits (3 types)
    a) 1 oscillation One from the CF oscillation, RC oscillation or X'tal oscillation
    b) 2 oscillations CF oscillation + X'tal oscillation or RC oscillation +X'tal oscillation
    CF (Ceramic) Oscillation Circuit
    - System Clock for the FAST mode
    - 400 kHz - 4MHz

    RC (Resistance, capacitor) Oscillation Circuit
    - System clock for FAST mode
    - 400kHz - 800kHz
    - 2-pin oscillation

    X'tal (Crystal) Oscillation Circuit
    - System clock for SLOW mode
    - 32.768kHz, 65.536kHz

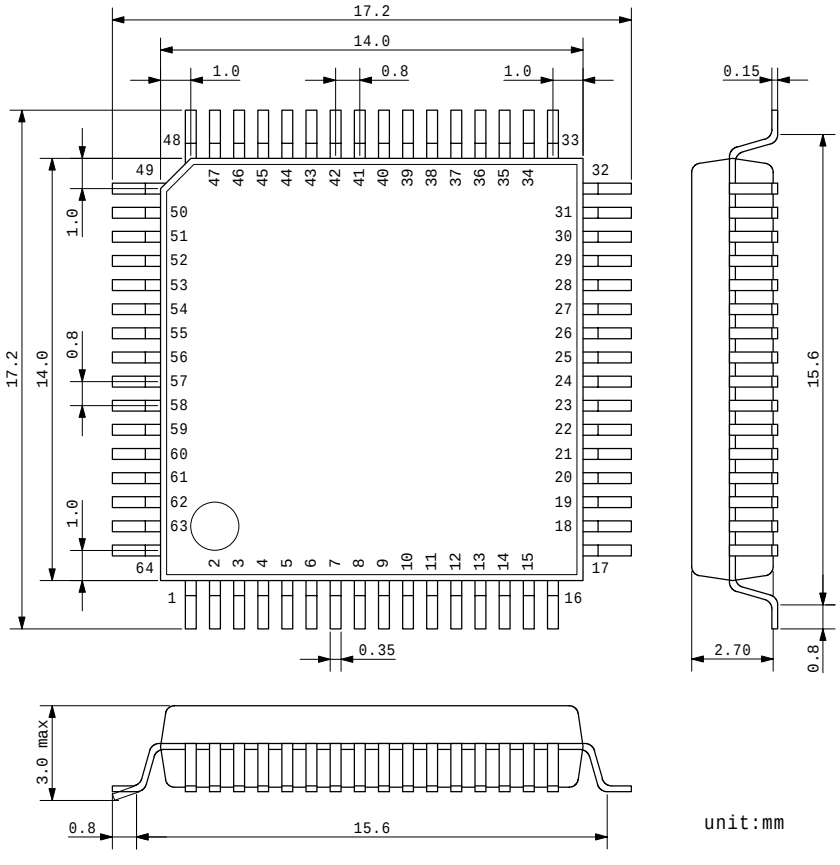
13. Shipment
    - QIP64E (Flat-package)

14. Pin assignment

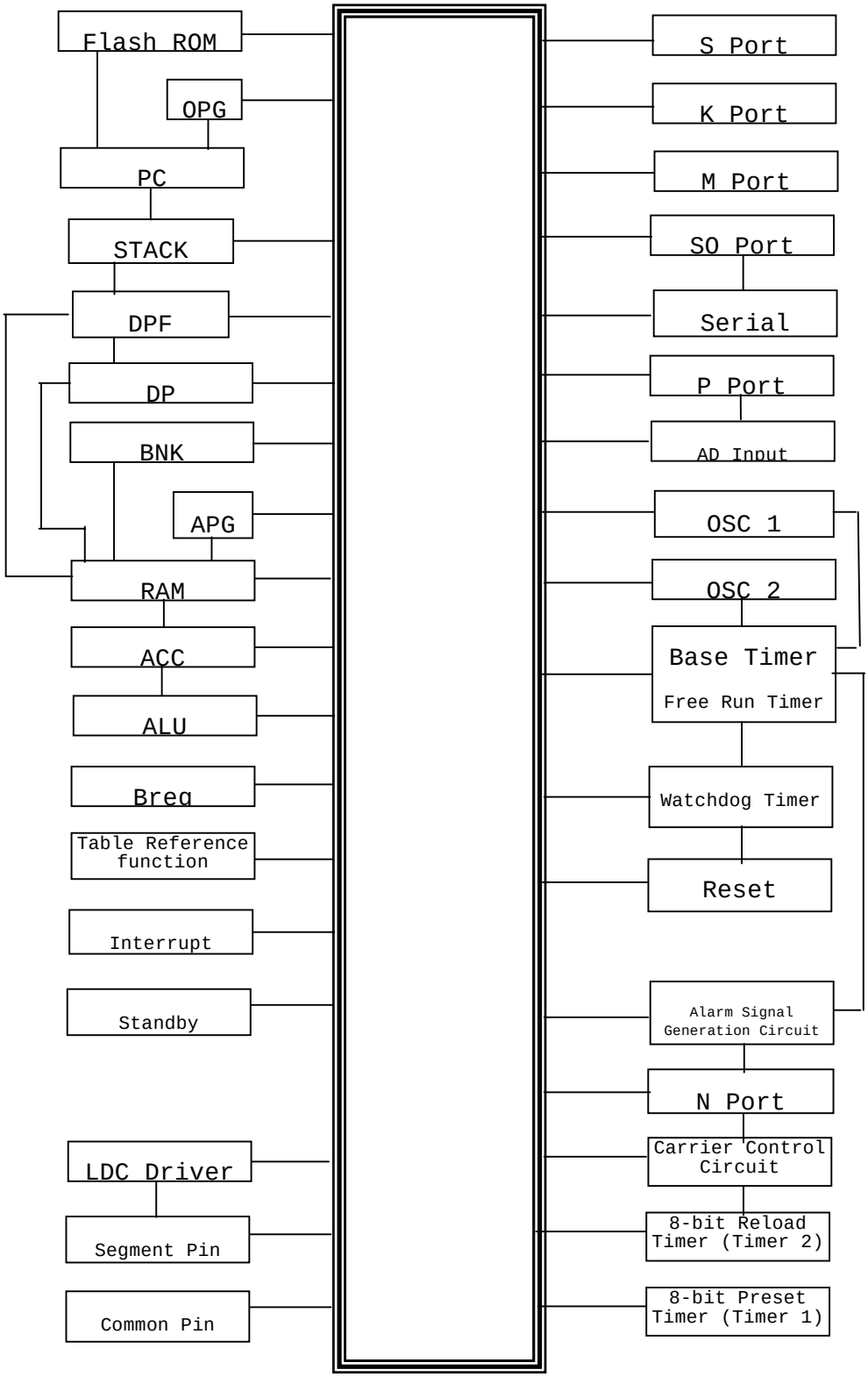


- Pin No.35 (TST) must be connected to VSS.
- For the soldered chip, contact to your nearest SANYO sales department.

15. External form (refer to the delivery specification form for details)



System Clock Diagram



Overview of the Mask Option

The user can select mask option as it is available for adjusting the hardware functions of the microcontroller to the application type.

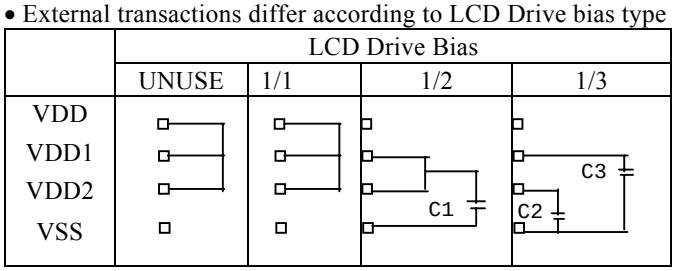
Options for the Oscillation Circuit

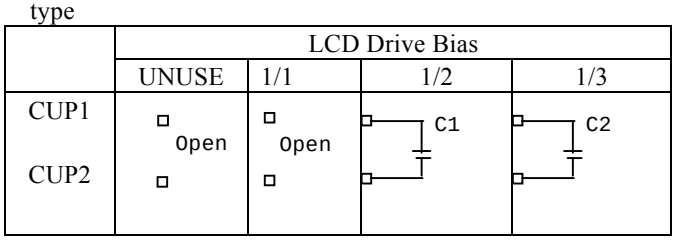
- OSC1 SELECT Selects OSC1 oscillation type that corresponds to the application.
  1:EXT 2:RC 3:CF 4:NONUSED
- OSC1 PRE-DIV Selects OSC1 system clock type.
  1:OSC1/1 2:OSC1/2
- OSC1 WAIT TIME SELECT Selects OSC1 reset release time.
  1:1/4K 2:1/8K 3:1/16K 4:1/42K 5:1/65K
- OSC2 SELECT Selects OSC2 oscillation type that corresponds to the application.
  1:32KNz 2:65KHz 3:NONUSED
- OSC2 CdRd SELECT Selects OSC2 oscillation type.
  1:USE 2:NONUSE

Other Options

- RESISTOR SOURCE LEVEL Selects pull-up/pull-down type
  1:PULL DOWN 2:PULL UP
- RES PORT RESISTOR SELECT Selects RESET pin type.
  1:OPEN 2:PULL DOWN 3:PULL UP (Note:"Pull-up" and "OPEN" are only available for LC58F74XX)
- RES PORT LEVEL Selects the supply level of RESET operation.
  1:L-LEVEL 2:H-LEVEL ("L-LEVEL" is only available for LC58F74XX)
- N PORT INITIAL LEVEL Selects the initialized state of N port.
  1:L-Level 2:H-Level
- OUTPUT N1 Port Selects N1 port as the output format.
  1:N-CH 2:CMOS
- OUTPUT N2 Port Selects N2 port as the output format.
  1:N-CH 2:CMOS
- OUTPUT N3 Port Selects N3 port as the output format.
  1:N-CH 2:CMOS
- OUTPUT N4 Port Selects N4 port as the output format.
  1:N-CH 2:CMOS

Pin Functions

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>State when reset</th></tr>
<tr><td>VSS</td><td></td><td>(-) pin of power-on</td><td></td></tr>
<tr><td>VDD</td><td></td><td>(+) pin of power-on</td><td></td></tr>
<tr><td>VDD1
VDD2</td><td></td><td>• LCD Drive Power Pin
• External transactions differ according to LCD Drive bias type
 

C1,C2,C3=0.1μ F (typ)</td><td></td></tr>
<tr><td>CUP1
CUP2</td><td></td><td>• LCD Drive Pin
• External transactions differ according to every LCD Drive bias type
 

C1,C2 =0.1μ F (typ)</td><td></td></tr>
<tr><td>CFIN
CFOUT</td><td>IN
OUT</td><td>• OSC1 (FAST Mode) Oscillation Pin
CF type : 400kHz - 4MHz
RC type : 400kHz - 800kHz
EXT type:200kHz - 4MHz</td><td></td></tr>
<tr><td>XTIN
XTOUT</td><td>IN
OUT</td><td>• OSC2 (SLOW Mode) Oscillation Pin
X’tal : 32kHz, 65kHz</td><td></td></tr>
<tr><td>INT</td><td>IN</td><td>• 1 bit input pin
• External interrupt input pin
• Program determines the input type and the interrupt level (Pull-up, pull-down, open)
(Rising edge, falling edge)
• “Level-hold function” that prevent floating is available</td><td>• Interrupt acceptance disabled</td></tr>
<tr><td>S1
S2
S3
S4</td><td>IN
IN
IN
IN</td><td>• 4-bit input port
• Pull-up or pull-down (controlled by program for each port) is imbedded.
• Input signal change detect circuit by one bit unit.
• “Level-hold function” that prevent floating is available</td><td>• Pull-up or pull-down resistance : ON (OFF after reset release)</td></tr>
<tr><td>K1
K2
K3
K4</td><td>IN/OUT
IN/OUT
IN/OUT
IN/OUT</td><td>• 4-bit input port
• Pull-up or pull-down (controlled by program for each port) is imbedded.
• Input signal change detect circuit by port.
• Output format : CMOS
• “Level-hold function” that prevent floating is available</td><td>• Input mode
• Pull-up or pull-down resistance : ON (OFF after reset release)
• Output Latch data :HIGH</td></tr>
</table>

Pin Name	I/O	Function	State when reset
SO1 SO2 SO3 SO4	IN/OUT IN/OUT IN/OUT IN/OUT	• 4-bit input port (shared with serial interface) SO1:Serial input pin SO2:Serial output pin SO3:Serial clock pin • parallel serial transfer possible • SO4 pin is in HALT mode when the serial function is not used and can be applied as a release source or an interrupt source. • Pull-up or pull-down (controlled by program for each port) is imbedded. • Output format can be controlled for each port by program (CMOS/Nch) • "Level-hold function" that prevent floating is available	• Input mode • Pull-up or pull-down resistance : ON (OFF after reset release) • 4-bit parallel mode • Output Latch data :HIGH
M1 M2 M3 M4	IN/OUT IN/OUT IN/OUT IN/OUT	• 4-bit input/output port • Pull-up or pull-down (controlled by program for each port) is imbedded. • Output format can be controlled for each port by program (CMOS/Pch) • M4 pin changes to be as a clock input pin when operating Timer 2 as an event counter mode. • "Level-hold function" that prevent floating is available	• Input mode • Pull-up or pull-down resistance : ON (OFF after reset release) • Output Latch data :HIGH
P1 P2 P3 P4	IN/OUT IN/OUT IN/OUT IN/OUT	• 4-bit input/output port • Pull-up or pull-down (controlled by program for each port) is imbedded. • Output format can be controlled for each port by program (CMOS/Pch) • "Level-hold function" that prevent floating is available	• Input mode • Pull-up or pull-down resistance : ON (OFF after reset release) • Output Latch data :HIGH
N1 N2 N3 N4	OUT OUT OUT OUT	• 4-bit output port • Output format can be controlled for each port by program (CMOS/Nch) • Mid-withstand pressure when in Nch open drain format • N3 pin is an output pin for remote control carrier signal. • N4 pin is an output pin for alarm pulse signal.	•Output level is determined with an option.
SEG01 to SEG23	OUT OUT	• LCD panel segment drive pin • Can be applied for 6 types of drive formats. • Used as a general output pin (CMOS, Pch, Nch) by program • Can be combined with LCD drive pin and general purpose output pin	
COM1 COM2 COM3 COM4	OUT OUT OUT OUT	• LCD panel common electrode drive pin • Uses from COM1 to COM4 according to LCD drive duty type • LCD drive frequency (frame frequency) is determined by program.	
RES	IN	• Input pin for the microcontroller reset Reset signal of over 200 μs must be supplied.	
TST	IN	• Test pin • Must be connected to the VSS pin level ("-" side of the power)	

Absolute Maximum Rate / VSS = 0V, Ta = 25 °C

Item	Sign	Condition / Pin	Min.	Typ.	Max.	Unit
Max.Power Voltage	VDD		-0.3		+7.0	V
	VDD1		-0.3		VDD	V
	VDD2		-0.3		VDD	V
Max.Input Voltage	VI(1)	Admitted at specified circuit XTIN,CFIN	Admitted up to the generated voltage			
	VI(2)	S1-4,K1-4,P1-4,SO1-4,RES,INT,TST (K,P,M,SO ports are in input mode)	-0.3		VDD +0.3	V
Max.Output Voltage	VO(1)	Admitted at specified circuit XTOUT,CFOUT	Admitted up to the generated voltage			
	VO(2)	K1-4,P1-4,SO1-4,N1-4,CUP1,CUP2,SEG1-23,COM1-4 (K,P,M,SO ports are in output mode)	-0.3		VDD +0.3	V
	VO(3)	Open drain type N1 - 4 (Nch)	-0.3		+16	V
Output Pin Current	IO(1)	N1 - 4 for each pin	0		+10	mA
	IO(2)		-10		0	mA
	IO(3)	K1-4, P1-4, M1-4, SO-4 for each pin	0		+5	mA
	IO(4)		-5		0	mA
	∑IO(1)	Total current at pins (K1-4,P1-4,M1-4,SO1-4,N1-4,SEG1-23)			40	mA
	∑ IO(2)		-40			mA
Admitted power consumption	PD(max)	QIP - 64E Flat Package			300	mW
Operation peripheral temperature	Topg		-30		+70	°C
Saving peripheral temperature	Tstg		-55		+125	°C

Admissible Operation Range / VSS = OV, Ta = -30 to + 70°C

Item	Sign	Condition / Pin	Min.	Typ.	Max.	Unit
Power Voltage	VDD	LCD with no spec:VDD1=VDD2=VDD STATIC spec: VDD1=VDD2=VDD 1/2Bias spec:VDD1=VDD2=1/2VDD 1/3Bias spec:VDD1=2×1/3VDD VDD2=1/3VDD	3.0 3.0 3.0 3.0		5.5 5.5 5.5 5.5	V V V
Hold Power Voltage	VHD	RAM. Register hold voltage (*1)	2.0		VDD	V
Input “H” Voltage	VIH1	S1-4, K1-4,P1-4, M1-4, SO1-4 INT(K,P,M,SO ports are in input mode)	0.7VDD		VDD	V
	VIH2	RES pin	0.75VDD		VDD	V
	VIH3	CFIN pin	0.75VDD		VDD	V
Input “L” Voltage	VIL1	S1-4, K1-4,P1-4,M1-4,SO1-4 INT(K,P,M,SO ports are in input mode)	0		0.3VDD	V
	VIL2	RES pin	0		0.25VDD	V
	VIL3	CFIN pin	0		0.25VDD	V
Frequency no.1	fopg1	VDD=3.0V-5.5V , 32KHz XTIN/XTOUT,X’tal oscillation	32		33	kHz
Frequency no.2	fopg2	VDD=3.0V-5.5V, 38KHz XTIN/XTOUT,X’tal oscillation	37		39	kHz
Frequency no.3	fopg3	VDD=3.0V-5.5V , 65KHz XTIN/XTOUT,X’tal oscillation	60		70	kHz
Frequency no.4	fopg4	VDD=4.5V-5.5V ,CFIN/CFOUT,CF spec	390		810	kHz
Frequency no.5	fopg5	VDD=4.5V-5.5V CFIN/CFOUT CF spec	390		1200	kHz
Frequency no.6	fopg6	VDD=4.5V-5.5V CFIN/CFOUT CF spec	390		4200	kHz
Frequency no.7	fopg7	VDD=4.5V-5.5V CFIN/CFOUT RC spec	190		800	kHz
Frequency no.8	fopg8	VDD=4.5V-5.5V CFIN/CFOUT EXT spec	DC		4000	kHz
Frequency no.9	fopg9	VDD=4.5V-5.5V SO1/SO3 pin (with serial) Input signal/Rising and falling edge of the clock waveform ≤ 10 μs			200	kHz

(*1) When all the internal circuits stop with the total stop of the CF/RC oscillation and X’tal oscillation.

Electrical Features / VDD=3.0-4.5V, VSS=OV, Ta=-30 to +70°C

Item	Sign	Condition / Pin	Min.	Typ.	Max.	Unit
Input Resistance	RIN1A	VIN=0.2VDD, "L"Level Hold Tr (*1)	35	200	800	kΩ
	RIN1B	VIN=VDD, Pull-down resistance (*1)	15	80	300	kΩ
	RIN1C	VIN=0.8VDD, "H" Level hold Tr (*1)	35	200	800	kΩ
	RIN1D	VIN=VSS, Pull-up resistance (*1)	15	80	300	kΩ
	RIN2A	VIN=0.2VDD, INT "L" Level hold Tr	35	200	800	kΩ
	RIN2B	VIN=VDD, INT pull-down resistance	150	800	3000	kΩ
	RIN2C	VIN=0.8VDD, INT "H" Level hold Tr	35	200	800	kΩ
	RIN2D	VIN=VSS, INT pull-up resistance	150	800	3000	kΩ
	RIN5	VIN=VDD, TST pin pull-down resistance	20	50	300	kΩ
Output "H" Voltage	VOH(1)	IOH=--1.0mA N1-4	VDD-0.5			V
Output "L" Voltage	VOL(1)	IOL=2.0mA			0.5	V
	VOH(2)	IOH=-500µA K1-4,P1-4,M1-4,SO1-4	VDD-0.5			V
	VOL(2)	IOL=500µA(K,P,M,SO ports are in output mode)			0.5	V
Output OFF LEAK Current	|IOFF|	VOH=10.5V N1-4 (Open spec)			1.0	µA
Segment Port Output impedance • with CMOS output port						
Output "H" Voltage	VOH(3)	IOH= -300µA	VDD-0.5			V
Output "L" Voltage	VOL(3)	IOH= 300µA,			0.5	V
Segment Port Output impedance • with Pch open drain output port						
Output "H" Voltage	VOH(3)	IOH= -300µA	VDD-0.5			V
Output Off-leak voltage	|IOFF|	VOL=VSS			1.0	µA
Segment Port Output impedance • with Nch open drain output port						
Output "L" Voltage	VOL(3)	IOH= 300µA			0.5	V
Output Offleak voltage	|IOFF|	VOH=VDD			1.0	µA
Segment Port Output impedance • Static						
Output "H" Voltage	VOH(4)	IOH= -20µA, Seg 1-23	VDD-0.2			V
Output "L" Voltage	VOL(4)	IOL= 20µA			0.2	V
Output "H" Voltage	VOH(5)	IOH= -100µA, COM1	VDD-0.2			V
Output "L" Voltage	VOL(5)	IOL= 100µA,			0.2	V
Segment Port Output impedance • 1/2 bias						
Output "H" Voltage	VOH(4)	IOH= -20µA, Seg 1-23	VDD-0.2			V
Output "L" Voltage	VOL(4)	IOL= 20µA			0.2	V
Output "H" Voltage	VOH(5)	IOH= -100µA, COM1-4	VDD-0.2			V
Output "M" Voltage	VOM	IOL= -100µA,	VDD/2 -0.2		VDD/2 +0.2	V
		IOL= 100µA,				
Output "L" Voltage	VOL(5)	IOL= 100µA,			0.2	V
Segment Port Output impedance • 1/3 bias						
Output "H" Voltage	VOH(4)	IOH= -20µA, Seg 1-23	VDD-0.2			V
Output "M" Voltage	VOM1-1	IOL= -20µA	2VDD/3 -0.2		2VDD/3 +0.2	V
	VOM1-2	IOL= 20µA	VDD/3 -0.2		VDD/3 +0.2	V
Output "L" Voltage	VOL(4)	IOL= 20µA			0.2	V
Output "H" Voltage	VOH(6)	IOH= -100µA, COM1-4	VDD-0.2			V
Output "M" Voltage	VOM2-1	IOH= -100µA	2VDD/3 -0.2		2VDD/3 +0.2	V
	VOM2-2	IOL= 100µA,	VDD/3 -0.2		VDD/3 +0.2	V
Output "L" Voltage	VOL(6)	IOL= 100µA,			0.2	V

(*1) 20 pins of S1-4, K1-4, P1-4, M1-4, SO1-4.

Electrical Features / VDD=3.0-4.5V, VSS=OV, Ta=-30 to +70°C

Item	Sign	Condition / Pin	Min.	Typ.	Max.	Unit
Power Leak Current	ILEK(1)	VDD=3.0V,Ta=25°C		0.2	1.0	µA
Power Leak Current	ILEK(2)	VDD=3.0V,Ta=50°C		1.0	5.0	µA
Input Leak Current	IOFF	VDD=3.0V, S1-4,K1-4,P1-4,M1-4,SO1-4				
		VIN=VDD,(K,P,M,SO are in input mode)			1.0	µA
		VIN=VSS, INT,RES (INT,RES are open spec)	-1.0			µA
Output Voltage 1	VDD1-(1)	VDD=3.0V,C1=C2=0.1µF VDD1=VDD2,1/2 Bias, fopg=32.768KHz	1.3	1.5	1.7	V
Power current 1	|IDD|1-1	VDD=3.0V, Ta=25°C		7	15	µA
	|IDD|1-2	VDD=3.0V, Ta=50°C			20	µA
		X'tal oscillation spec, Crystal 32KHz (with Cd,Rd)				
		Cg=11pF,CI=31KΩ, at HALT,LCD=1/3 Bias				
Power current 2	|IDD|2-1	VDD=3.0V, Ta=25°C		25	35	µA
	|IDD|2-2	VDD=3.0V, Ta=50°C			40	µA
		X'tal oscillation spec, Crystal 32KHz (with Cd,Rd)				
		Cg=11pF,CI=31KΩ,with sequential ROM, LCD=1/3 Bias				
Power current 3	|IDD|3-1	VDD=3.0V, Ta=25°C		300	400	µA
	|IDD|3-2	VDD=3.0V, Ta=50°C			400	µA
		CF oscillation spec, CF4MHz				
		Ccg=Ccd=33pF,at HALT, LCD=1/3 Bias				
Power current 4	|IDD|4-1	VDD=3.0V, Ta=25°C		1000	1100	µA
	|IDD|4-2	VDD=3.0V, Ta=50°C			1100	µA
		CF oscillation spec, CF4MHz				
		Ccg=Ccd=33pF,with sequential ROM, LCD=1/3 Bias				
Oscillation hold voltage	|VHOLD|	With 32kHz X'tal	3.0		5.5	V
Oscillation start time	|TSTT|	VDD=3.0V, XCg=11pF,XCI≤31kΩ			5	s
Oscillation stable grade	△ f	VDD=2.95-3.05V			3	ppm
Oscillation hold voltage	|VHOLD|	With 65kHz X'tal	3.0		5.5	V
Oscillation start time	|TSTT|	VDD=3.0V, XCg=12pF,XCI≤31kΩ			5	s
Oscillation hold voltage	|VHOLD|	With 4MHz CF	4.5		5.5	V
Oscillation start time	|TSTT|	VDD=4.5V, Ccg=Ccd=33pF			30	ms
Oscillation correcting capacity	Cd	VDD=3.0V, XTOUT pin (built-in)		20		pF

Electrical Features / VDD=4.5-5.5V, VSS=OV, Ta=-30 to +70°C

Item	Sign	Condition / Pin	Min.	Typ.	Max.	Unit
Input Resistance	RIN1A	VIN=0.2VDD, "L" level hold Tr (*1)	30	120	500	kΩ
	RIN1B	VIN=VDD, pull-down resistance (*)	10	50	200	kΩ
	RIN1C	VIN=0.8VDD, "H" level hold Tr (*1)	30	120	500	kΩ
	RIN1D	VIN=VSS, pull-up resistance (*1)	10	50	200	kΩ
	RIN2A	VIN=0.2VDD,INT "L" level hold Tr	30	120	500	kΩ
	RIN2B	VIN=VDD,INT pull-down	100	500	2000	kΩ
	RIN2C	VIN=0.8VDD, INT "H" level hold Tr	30	120	500	kΩ
	RIN2D	VIN=VSS, INT pull-up resistance	100	500	2000	kΩ
	RIN5	VIN=VDD,TST pin pull-down resistance	20	50	300	kΩ
Output "H" voltage	VOH(1)	IOH=-5.0mA, N1-4	VDD-0.5			V
Output "L" voltage	VOL(1)	IOL=5.0mA			0.5	V
	VOH(2)	IOH=-1.0mA, K1-4,P1-4,M1-4,SO1-4	VDD-0.5			V
	VOL(2)	IOL=2.0mA(K,P,M,SO ports are in output mode)			0.5	V
Output OFF LEAK Current	|IOFF|	VOH=10.5V N1-4 (Open spec)			1.0	µA
Segment Port Output impedance • with CMOS output port						
Output "H" Voltage	VOH(3)	IOH= -500µA	VDD-0.5			V
Output "L" Voltage	VOL(3)	IOH= 500µA,			0.5	V
Segment Port Output impedance • with Pch open drain output port						
Output "H" Voltage	VOH(3)	IOH= -500µA	VDD-0.5			V
Output Offleak voltage	|IOFF|	VOL=VSS			1.0	µA
Segment Port Output impedance • with Nch open drain output port						
Output "L" Voltage	VOL(3)	IOH= 500µA			0.5	V
Output Offleak voltage	|IOFF|	VOH=VDD			1.0	µA
Segment Port Output impedance • Static						
Output "H" Voltage	VOH(4)	IOH= -40µA, Seg 1-23	VDD-0.2			V
Output "L" Voltage	VOL(4)	IOL= 40µA			0.2	V
Output "H" Voltage	VOH(5)	IOH= -400µA, COM1	VDD-0.2			V
Output "L" Voltage	VOL(5)	IOL= 400µA,			0.2	V
Segment Port Output impedance • 1/2 bias						
Output "H" Voltage	VOH(4)	IOH= -40µA, Seg 1-23	VDD-0.2			V
Output "L" Voltage	VOL(4)	IOL= 40µA			0.2	V
Output "H" Voltage	VOH(5)	IOH= -400µA, COM1-4	VDD-0.2			V
Output "M" Voltage	VOM	IOL= -400µA,	VDD/2		VDD/2	V
		IOL= 400µA,	-0.2		+0.2	
Output "L" Voltage	VOL(5)	IOL= 400µA			0.2	V
Segment Port Output impedance • 1/3 bias						
Output "H" Voltage	VOH(4)	IOH= -40µA, Seg 1-23	VDD-0.2			V
Output "M" Voltage	VOM1-1	IOH= -40µA	2VDD/3		2VDD/3	V
			-0.2		+0.2	
	VOM1-2	IOL= 40µA,	VDD/3		VDD/3	V
			-0.2		+0.2	
Output "L" Voltage	VOL(4)	IOL= 40µA			0.2	V
Output "H" Voltage	VOH(6)	IOH= -400µA, COM1-4	VDD-0.2			V
Output "M" Voltage	VOM2-1	IOL= -400µA,	2VDD/3		2VDD/3	V
			-0.2		+0.2	
	VOM2-2	IOL= 400µA,	VDD/3		VDD/3	V
			-0.2		+0.2	
Output "L" Voltage	VOL(6)	IOL= 400µA			0.2	V

(*1) 20 pins of S1-4, K1-4, P1-4, M1-4,SO1-4.

Electrical Features / VDD=4.5-5.5V, VSS=OV, Ta=-30 to +70°C

Item	Sign	Condition / Pin	Min.	Typ.	Max.	Unit
Power Leak Current	ILEK(1)	VDD=5.0V,Ta=25°C		0.2	1.0	µA
Power Leak Current	ILEK(2)	VDD=5.5V,Ta=50°C		1.0	5.0	µA
Input Leak Current	IOFF	VDD=5.5V,S1-4,K1-4,P1-4,M1-4,SO1-4				
		VIN=VDD,(K,P,M,SO are in input mode)			1.0	µA
		VIN=VSS, INT,RES (INT,RES are open spec)	-1.0			µA
Output Voltage 1	VDD1-(2)	VDD=3.0V,C1=C2=0.1µF VDD1=VDD2,1/2 Bias, fopg=32.768KHz	2.4	2.5	2.6	V
Output Voltage 2	VDD1-(3)	VDD=5.0V,C1=C2=0.1µF,1/3 Bias, fopg=32.768KHz	1.4	1.67	1.8	V
	VDD1-(3)		3.1	3.33	3.5	V
Power current 1	|IDD|1-1	VDD=5.0V, Ta=25°C		45	60	µA
	|IDD|1-2	VDD=5.0V, Ta=50°C			65	µA
		X'tal oscillation spec, Crystal 32KHz (with Cd,Rd)				
		Cg=11pF,CI=31KΩ, at HALT,LCD=1/3 Bias				
Power current 2	|IDD|2-1	VDD=5.0V, Ta=25°C		80	90	µA
	|IDD|2-2	VDD=5.0V, Ta=50°C			90	µA
		X'tal oscillation spec, Crystal 32KHz (with Cd,Rd)				
		Cg=11pF,CI=31KΩ,with sequential ROM, LCD=1/3 Bias				
Power current 3	|IDD|3-1	VDD=5.0V, Ta=25°C		900	1000	µA
	|IDD|3-2	VDD=5.0V, Ta=50°C			1100	µA
		CF oscillation spec, CF4MHz				
		Ccg=Ccd=33pF,at HALT, LCD=1/3 Bias				
Power current 4	|IDD|4-1	VDD=5.0V, Ta=25°C		3000	4000	µA
	|IDD|4-2	VDD=5.0V, Ta=50°C			4000	µA
		CF oscillation spec, CF4MHz				
		Ccg=Ccd=33pF,with sequential ROM, LCD=1/3 Bias				
Oscillation correcting capacity	Cd	VDD=5.0V, XTOUT pin (built-in)		20		pF

AD Conversion Features / VSS = OV, Ta=-30 to +70°C

Item	Sign	Condition / Pin	Min.	Typ.	Max.	Unit
Resolution	N	VDD=3.072V, Ta=25°C		8		bit
Absolute precision	ET	VDD=3.072V, Ta=25°C			±1.5	LSB
Analog input Voltage range	VAIN		VSS		VDD	V