SANYO Preliminary	8-BIT SINGLE CHIP MICROCOMPUTER LC867148A/40A/32A/28A/24A/20A/16A/12A/08A

LC867148A
On-chip 48K-byte ROM and On-chip 1152-byte RAM 8-bit single chip microcomputer

LC867140A
On-chip 40K-byte ROM and On-chip 1152-byte RAM 8-bit single chip microcomputer

LC867132A
On-chip 32K-byte ROM and On-chip 768-byte RAM 8-bit single chip microcomputer

LC867128A
On-chip 28K-byte ROM and On-chip 768-byte RAM 8-bit single chip microcomputer

LC867124A
On-chip 24K-byte ROM and On-chip 768-byte RAM 8-bit single chip microcomputer

LC867120A
On-chip 20K-byte ROM and On-chip 640-byte RAM 8-bit single chip microcomputer

LC867116A
On-chip 16K-byte ROM and On-chip 640-byte RAM 8-bit single chip microcomputer

LC867112A
On-chip 12K-byte ROM and On-chip 512-byte RAM 8-bit single chip microcomputer

LC867108A
On-chip 08K-byte ROM and On-chip 512-byte RAM 8-bit single chip microcomputer

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Overview

The LC867148A/40A/32A/28A/24A/20A/16A/12A/08A microcomputers are 8-bit single chip microcomputers with the following on-chip functional blocks :

- CPU : Operable at a minimum bus cycle time of 0.5µs (microsecond)
- On-chip ROM maximum capacity : 48K bytes
- On-chip RAM capacity : 1152 bytes (LC867148A/40A)
  768 bytes (LC867132A/28A/24A)
  640 bytes (LC867120A/16A)
  512 bytes (LC867112A/08A)
- LCD controller/driver
- Two 16-bit timers (or four 8-bit timers)
- 12-channel × 8-bit AD converter
- 4-channel × 8-bit DA converter (R-2R)
- Two 8-bit synchronous serial-interface circuits
- 13-source 10-vectored interrupt system

All of the above functions are fabricated on a single chip.

Features

(1) Read Only Memory (ROM)

: LC867148A	49152 × 8 bits
: LC867140A	40960 × 8 bits
: LC867132A	32768 × 8 bits
: LC867128A	28672 × 8 bits
: LC867124A	24576 × 8 bits
: LC867120A	20480 × 8 bits
: LC867116A	16384 × 8 bits
: LC867112A	12288 × 8 bits
: LC867108A	8192 × 8 bits

(2) Random Access Memory (RAM)

: LC867148A/40A	1152 × 8 bits
: LC867132A/28A/24A	768 × 8 bits
: LC867120A/16A	640 × 8 bits
: LC867112A/08A	512 × 8 bits

(3) Bus Cycle Time / Instruction Cycle Time

The LC867148A/40A/32A/28A/24A/20A/16A/12A/08A are constructed to read ROM twice within one instruction cycle. It has 1.7 times more performance capability within the same instruction cycle compared to our 4-bit microcomputers (LC66000 series).

Bus cycle time indicates the speed to read ROM.

Bus cycle time	Cycle time	Clock divider	System clock oscillation	Oscillation Frequency	Voltage
0.5µs	1.0µs	1/1	Ceramic resonator oscillation	6MHz	4.5 - 6.0V
2.0µs	4.0µs	1/2	Ceramic resonator oscillation	3MHz	2.5 - 6.0V
7.5µs	15.0µs	1/2	RC resonator oscillation	800kHZ	2.5 - 6.0V
183µs	366µs	1/2	Crystal oscillation	32.768kHz	2.5 - 6.0V

(4) Ports
- Input / output ports : 50 terminals (normal ports P0, P1, PA, PB, PC, PD, P9)
  - P0 Input/output port programmable in nibble units : 1 port (8 terminals)
    (When the N-channel open drain output is selected, the data in a bit can be inputted.)
  - P1 Input/output port programmable in a bit : 1 port (8 terminals)
  - PA, PB, PC, PD (can be used for LCD)
    Input/output port programmable in two bits : 4 ports (30 terminals)
  - P9 (can be used for DA output)
    Input/output port programmable in a bit : 1 port (4 terminals)
- Input ports : 21 terminals (P7, P8, PL)
- LCD control port : 34 terminals
  Segment output port : 30 terminals
  Common output port : 4 terminals

(5) LCD controller / driver
- Selectable seven kinds of display mode (a combination of static 1/2, 1/3, 1/4 duty and 1/2, 1/3 bits)
- The segment and common output ports can be switched to a general input/output port.

(6) AD converter
- 12-channel × 8-bit AD converter

(7) DA converter
- 4-channel × 8-bit DA converter

(8) Serial-interface
- One channel × 16-bit serial-interface circuits (8-bit transmission available by program)
- LSB first/MSB first function available
- Internal 8-bit baud-rate generator in common with two serial-interface circuits

(9) Timers
- Timer0
  16-bit timer / counter
  2-bit prescaler + 8-bit programmable prescaler
  Mode 0 : Two 8-bit timers with programmable prescaler
  Mode 1 : 8-bit timer with programmable prescaler + 8-bit counter
  Mode 2 : 16-bit timer with programmable prescaler
  Mode 3 : 16-bit counter
  The resolution of Timer is tCYC. (tCYC : cycle time)
- Timer1
  16-bit timer / PWM
  Mode 0 : Two 8-bit timers
  Mode 1 : 8-bit timer + 8-bit PWM
  Mode 2 : 16-bit timer
  Mode 3 : Variable-bit PWM (9-16 bits)
  In Mode 0 and Mode 1, the resolution of Timer and PWM is tCYC.
  In Mode 2 and Mode 3, the resolution of Timer and PWM selectable ; tCYC or 1/2tCYC by program
- Base timer
  Every 500ms overflow system for a clock application (using 32.768kHz crystal oscillation for Base timer clock)
  Every 976µs, 3.9ms, 15.6ms, 62.5ms overflow system (using 32.768kHz crystal oscillation for Base timer clock)
  The Base timer clock selectable ; 32.768kHz crystal oscillation, System clock, and programmable prescaler output of Timer 0

(10) Buzzer output
- The Buzzer sound frequency selectable ; 4KHz, 2KHz (using 32.768kHz crystal oscillation for Base timer clock)

(11) Remote control receiver circuit (Shares with the P73/INT3/T0IN terminal)
- Noise rejection function
- Switch polarity function

(12) Watchdog timer
- The watchdog timer is taken on RC outside
- Watchdog timer operation selectable : interrupt system, system reset

(13) Interrupts system
- 13-source 10-vectored interrupts :
  1. External interrupt INT0 (include watchdog timer)
  2. External interrupt INT1
  3. External interrupt INT2, timer / counter T0L (Lower 8-bit)
  4. External interrupt INT3, base timer
  5. Timer / counter T0H (Upper 8-bit)
  6. Timer T1L, Timer T1H
  7. Serial interface SIO0
  8. Serial interface SIO1
  9. AD converter
  10. Port 0
- Built-in interrupt priority control register
  Microcomputer allows 3 levels of interrupt; low level, high level, and highest level of multiplex interrupt. It can specify a low level or a high level interrupt priority from INT2/T0L through port 0 (i.e. the above interrupt number from three through ten). It can also specify a low level or the highest level interrupt priority to INT0 and INT1.

(14) Real-time service operation
The Real-time service (RTS) functions the 4-byte data-transfer between the special function registers at acknowledging the interrupt request.
The RTS starts within 1 instruction cycle-time and completes within 5 instruction cycle-times after occurring the interrupt request.

(15) Sub-routine stack levels
- 128 levels (Max.) : stack area included in RAM area

(16) Multiplication and division
- 16-bit × 8-bit (7 instruction cycle times)
- 16-bit ÷ 8-bit (7 instruction cycle times)

(17) Three oscillation circuits
- On-chip RC oscillation circuit using for the system clock
- On-chip CF oscillation circuit using for the system clock
- On-chip crystal oscillation circuit using for the system clock and for time-base clock

(18) Standby function

- HALT mode function

  The HALT mode is used to reduce the power dissipation. In this operation mode, the program execution is stopped. This operation mode can be released by the interrupt request signals or the system reset request signal.

- HOLD mode function

  The HOLD mode is used to freeze all the oscillations ;
  RC (internal), CF and Crystal oscillations. This mode can be released by the following operations.

  • Reset terminal ($\overline{\text{RES}}$) set to low level.
  • Input a assigned level to P70/INT0 or P71/INT1 terminal
  • Input a Port0 interrupt condition

(19) Factory shipment

• QFP80E delivery form

(20) Development support tools

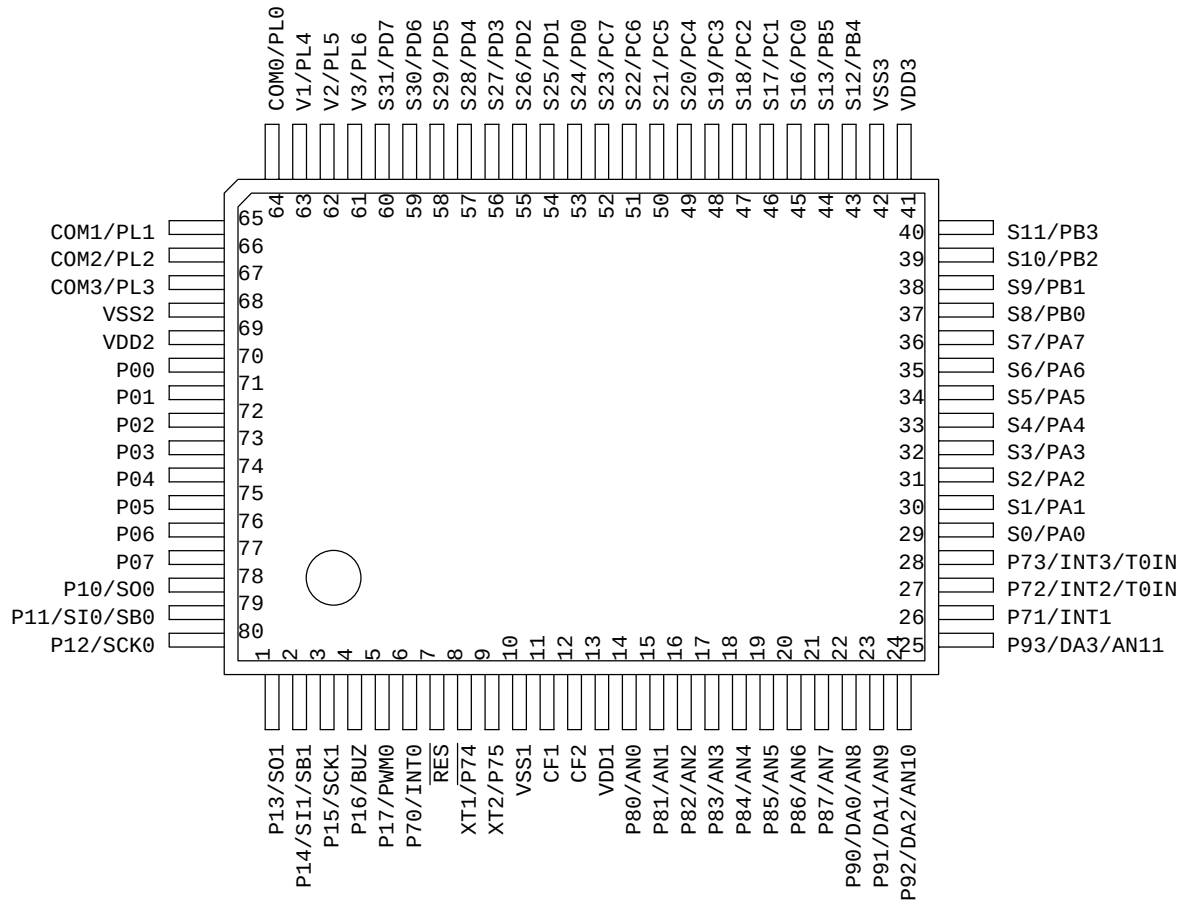
- Evaluation (EVA) chip : LC866096
- EPROM version : LC86E7148
- One time version : LC86P7148
- Emulator : EVA86000 + ECB867000 (Evaluation chip board) + POD867100 (Pod)

• Notes for use

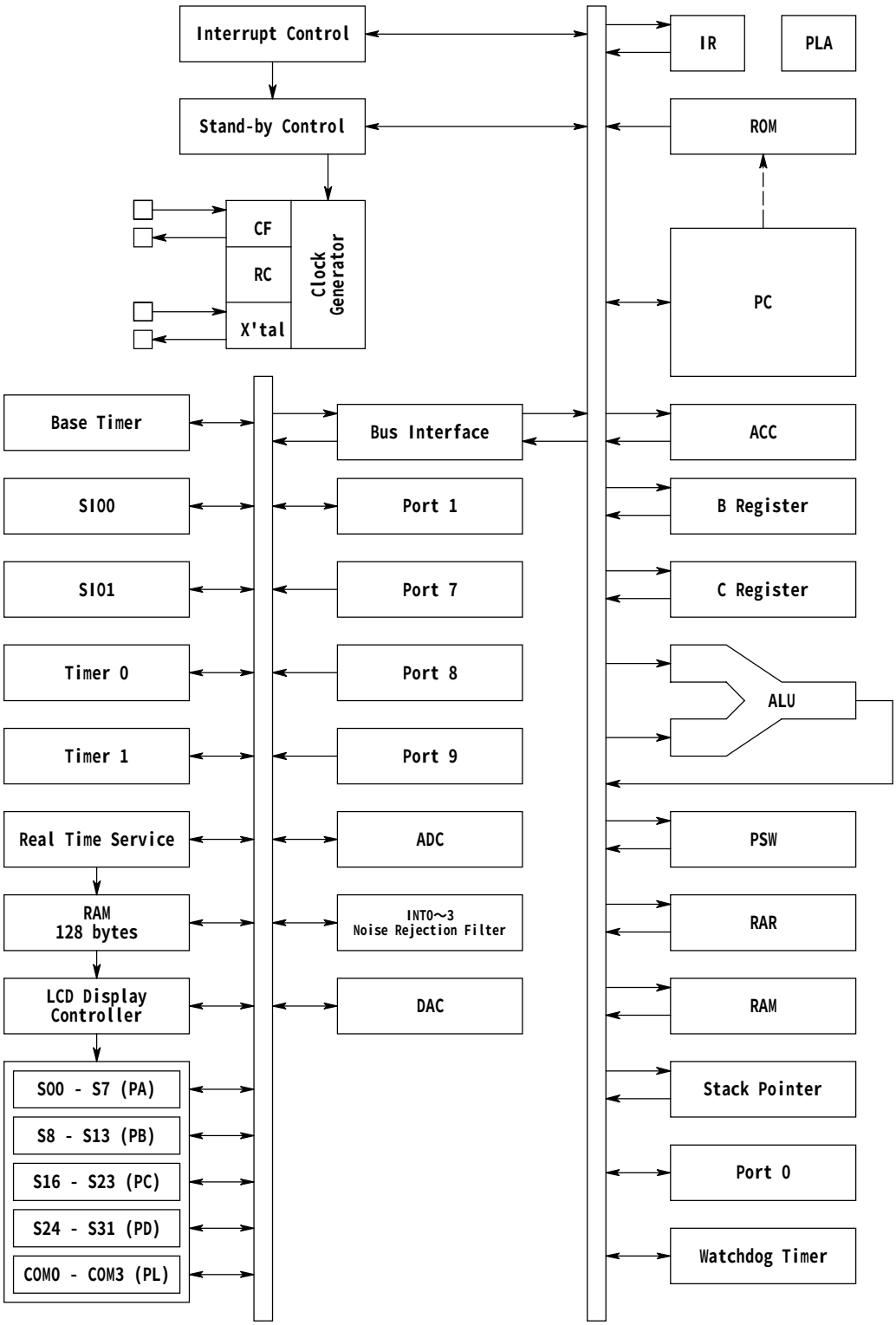
Follow the under table

Frequency range of the system clock	Voltage range	Clock Divider	Note
15kHz to 30kHz	4.5V to 6.0V	1/1	Can not use 1/2 divider
30kHz to 6MHz		1/1, 1/2	
15kHz to 30kHz	2.5V to 6.0V	1/1	Can not use 1/2 divider
30kHz to 1.5MHz		1/1, 1/2	
1.5MHz to 3MHz		1/2	Can not use 1/1 divider
Internal RC oscillation	4.5V to 6.0V	1/1, 1/2	
	2.5V to 6.0V	1/2	Can not use 1/1 divider

Pin Assignment



System Block Diagram



Pin Description

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function description</th><th>Option</th></tr>
<tr><td>VSS1</td><td>-</td><td>Power pin (–)</td><td>-</td></tr>
<tr><td>VSS2</td><td>-</td><td>Power pin (–)</td><td>-</td></tr>
<tr><td>VSS3</td><td>-</td><td>Power pin (–)</td><td>-</td></tr>
<tr><td>VDD1</td><td>-</td><td>Power pin (+)</td><td>-</td></tr>
<tr><td>VDD2</td><td>-</td><td>Power pin (+)</td><td>-</td></tr>
<tr><td>VDD3</td><td>-</td><td>Power pin (+)</td><td>-</td></tr>
<tr><td>PORT0
P00 - P07</td><td>I/O</td><td>• 8-bit input/output port
Input/output in nibble units
• Input for port 0 interrupt
• Input for HOLD release</td><td>• Pull-up resistor :
Provided/Not provided
(specified in nibble units)
• Output form (P00 – P07) :
CMOS/N-channel open drain
(specified in a bit)</td></tr>
<tr><td>PORT1
P10 - P17</td><td>I/O</td><td>• 8-bit input/output port
Input/output can be specified in bit unit
• Other pin functions
P10 SIO0 data output
P11 SIO0 data input/bus input/output
P12 SIO0 clock input/output
P13 SIO1 data output
P14 SIO1 data input/bus input/output
P15 SIO1 clock input/output
P16 Buzzer output
P17 Timer1 output (PWM output)</td><td>• Output form :
CMOS/N-channel open drain
(specified in a bit)</td></tr>
<tr><td>PORT7

P70

P71 - P73

$\overline{P74}$ - P75</td><td>

I/O

I

I</td><td>• 6-bit input port
• Other pin functions
P70 : INT0 input/HOLD release input/
N-channel Tr. output for watchdog timer
P71 : INT1 input/HOLD release input
P72 : INT2 input/timer 0 event input
P73 : INT3 input with noise filter/timer 0
event input
• Interrupt received form, vector address
<table>
<tr><th></th><th>rising</th><th>falling</th><th>rising & falling</th><th>high level</th><th>low level</th><th>vector</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr>
</table>
$\overline{P74}$: XT1 terminal for crystal oscillation
P75 : XT2 terminal for crystal oscillation</td><td>Pull-up resistor :
Provided/Not provided
(specified in a bit)
(P70, P71, P72, P73)
* $\overline{P74}$, P75 don’t have the pull-up resistor option.</td></tr>
<tr><td>Port8
P80 – P87</td><td>I</td><td>• 8-bit input port
• Other function
AD input port (8 port pins)</td><td>-</td></tr>
<tr><td>PORT9
P90 - P93</td><td>I/O</td><td>• 4-bit input/output port
• Other function
DA output port (4 port pins)
AD input port (4 port pins)</td><td>-</td></tr>
</table>

Pin name	I/O	Function description	Option
PORT A (S0/PA0 – S7/PA7)	I/O	• Segment output terminal for LCD display • Can be used as a general input/output port	-
PORT B (S8/PB0 – S13/PB5)	I/O	• Segment output terminal for LCD display • Can be used as a general input/output port	-
PORT C (S16/PC0 – S23/PC7)	I/O	• Segment output terminal for LCD display • Can be used as a general input/output port	-
PORT D (S24/PD0 – S31/PD7)	I/O	• Segment output terminal for LCD display • Can be used as a general input/output port	-
PORT L (COM0/PL0 – COM3/PL3)	I/O	• Common output terminal for LCD display • Can be used as a general input port	-
V1/PL4 – V3/PL6	I	• Bias power terminal for LCD drive • Can be used as a general input port	-
$\overline{\text{RES}}$	I	Reset pin	-
XT1/ $\overline{\text{P74}}$	I	• Input pin for 32.768kHz crystal oscillation In case of non use, connect to VDD. • Other function A general input port $\overline{\text{P74}}$	-
XT2/P75	O (I)	• Output pin for 32.768kHz crystal oscillation In case of non use, should be left unconnected • Other function A general input port P75	-
CF1	I	Input pin for ceramic resonator oscillation	-
CF2	O	Output pin for ceramic resonator oscillation	-

* All of port options can be specified in bit unit except the pull-up resistor of port 0.

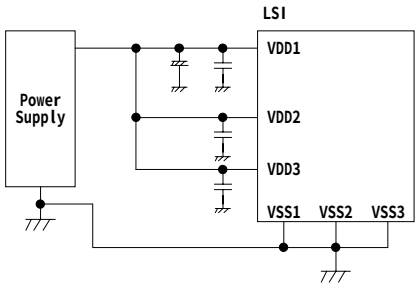
* A state of pins at reset

Pin name	I/O mode	A state of pull-up resistor specified at pull-up option
Port 0	Input	Fixed pull-up resistor OFF
Port 1	Input	Programmable pull-up resistor OFF
Port 3	Input	Programmable pull-up resistor OFF
Ports 70, 71, 72, 73	Input	Fixed pull-up resistor OFF
XT1/ $\overline{\text{P74}}$, XT2/P75	Input	General input port as $\overline{\text{P74}}$, P75 (If using as the crystal oscillation, the specified register must be set.)

Pin name	I/O mode
Ports A, B, C, D	Output OFF

[Notes] • The VDD1, VDD2 and VDD3 terminals must be shorted electrically each other.
• The VSS1, VSS2 and VSS3 terminals must be shorted electrically each other.

* Connect like the following figure to reduce noise into a VDD terminals.



1. Absolute maximum ratings / Ta=25°C, VSS=VSS1=VSS2=VSS3=0V

Parameter		Symbol	Pins	Conditions	Limits				
					VDD[V]	min.	typ.	max.	unit
Supply voltage		VDDMAX	VDD1, VDD2 VDD3	VDD1=VDD2= VDD3		-0.3		+7.0	V
LCD display voltage		VLCD	V1/PL6, V2/PL5 V3/PL4	VDD1=VDD2= VDD3		-0.3		VDD	
Input voltage		VI	•Ports 71, 72, 73 •Ports $\overline{74}$, 75 •Port 8, Port L • $\overline{RES}$			-0.3		VDD+0.3	
Input/output voltage		VIO	•Port 0, 1 •Port 9 •Ports A, B, C, D			-0.3		VDD+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1	•CMOS output •At each pins		-4			mA
		IOPH(2)	Ports A, B, C, D			-4			
		IOPH(3)	Port 9			-4			
	Total output current	ΣIOAH(1)	Ports 0, 1	Total all pins		-30			
		ΣIOAH(2)	Ports A, B	Total all pins		-20			
		ΣIOAH(3)	Ports C, D	Total all pins		-20			
		ΣIOAH(4)	Port 9	Total all pins		-20			
Low level output current	Peak output current	IOPL(1)	Ports 0, 1	At each pins				20	
		IOPL(2)	Ports A, B, C, D	At each pins				20	
		IOPL(3)	Port 9	At each pins				20	
		IOPL(4)	Port 70	At each pins				15	
	Total output current	ΣIOAL(1)	Ports 0, 1	Total all pins				40	
		ΣIOAL(2)	Ports A, B	Total all pins				30	
		ΣIOAL(3)	Ports C, D	Total all pins				30	
		ΣIOAL(4)	Port 9	Total all pins				15	
		vIOAL(5)	Port 70	Total all pins				10	
Maximum power dissipation		Pdmax	QFP80E	Ta=-30 to+70°C				515	mW
Operating temperature range		Topr				-30		+70	°C
Storage temperature range		Tstg				-65		+150	

2. Recommended operating range / Ta=-30°C to +70°C, VSS=VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
Operating supply voltage range	VDD(1)	VDD1=VDD2 =VDD3	0.98µs ≤ tCYC ≤ 400µs		4.5		6.0	V
	VDD(2)		3.9µs ≤ tCYC ≤ 400µs		2.5		6.0	
Hold voltage	VHD	VDD1=VDD2 =VDD3	RAMs and the registers hold voltage at HOLD mode.		2.0		6.0	
Input high voltage	VIH(1)	Port 0	Output disable	2.5-6.0	0.4VDD +0.9		VDD	
	VIH(2)	•Ports 1, 9 •Ports A, B, C, D •Ports 72, 73 (Schmitt)	Output disable	2.5-6.0	0.75VDD		VDD	
	VIH(3)	•Port 70 Port input/interrupt •Port 71 • $\overline{RES}$ (Schmitt)	Output N-channel Tr. OFF	2.5-6.0	0.75VDD		VDD	
	VIH(4)	Port 70 Watchdog timer	Output N-channel Tr. OFF	2.5-6.0	0.9VDD		VDD	
	VIH(5)	•Port 8 •Ports $\overline{74}$,75	Using as port	2.5-6.0	0.75VDD		VDD	
Input low voltage	VIL(1)	Port 0	Output disable	2.5-6.0	VSS		0.2VDD	
	VIL(2)	•Ports 1, 9 •Ports A, B, C, D •Ports 72, 73 (Schmitt)	Output disable	2.5-6.0	VSS		0.25VDD	
	VIL(3)	•Port 70 Port input/interrupt •Port 71 • $\overline{RES}$ (Schmitt)	Output N-channel Tr. OFF	2.5-6.0	VSS		0.25VDD	
	VIL(4)	Port 70 Watchdog timer	Output N-channel Tr. OFF	2.5-6.0	VSS		0.8VDD -1.0	
	VIL(5)	•Port 8 •Ports $\overline{74}$,75	Using as port	2.5-6.0	VSS		0.25VDD	
Operation cycle time	tCYC			4.5-6.0	0.98		400	µs
				2.5-6.0	3.9		400	

Parameter	Symbol	Pins	Conditions	VDD[V]	Limits min.	typ.	max.	unit
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 1	4.5-6.0				MHz
	FmCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 1	2.5-6.0	2.94	3	3.06	
	FmRC		RC oscillation	2.5-6.0	0.3	0.8	3.0	
	FsXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 2	2.5-6.0		32.768		kHz
Oscillation stabilizing time period (Note 1)	tmsCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 3	4.5-6.0				ms
	tmsCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 3	4.5-6.0				
				2.5-6.0				
	tssXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 3	4.5-6.0				s
				2.5-6.0				

(Note 1) The oscillation constant is shown on table 1 and table 2.

3. Electrical characteristics / Ta=-30°C to +70°C, VSS=VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[V]	min.	typ.	max.	unit
Input high current	IIH(1)	•Port 1 •Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr. OFF. VIN=VDD (including the off-leak current of the output Tr.)	2.5-6.0			1	µA
	IIH(2)	•Port 7 without pull-up MOS Tr. •Port 8	VIN=VDD	2.5-6.0			1	
	IIH(3)	Port 9	VIN=VDD	2.5-6.0			1	
	IIH(4)	Ports A, B, C, D, L	VIN=VDD	2.5-6.0			1	
	IIH(5)	$\overline{RES}$	VIN=VDD	2.5-6.0			1	
	IIH(6)	Ports $\overline{74}$,75	Using as port VIN=VDD	2.5-6.0			1	
Input low current	IIL(1)	•Port 1 •Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr. OFF. VIN=VSS (including the off-leak current of the output Tr.)	2.5-6.0	-1			
	IIL(2)	•Port 7 without pull-up MOS Tr. •Port 8	VIN=VSS	2.5-6.0	-1			
	IIL(3)	Port 9	VIN=VSS	2.5-6.0	-1			
	IIL(4)	Ports A, B, C, D, L	VIN=VSS	2.5-6.0	-1			
	IIL(5)	$\overline{RES}$	VIN=VSS	2.5-6.0	-1			
	IIL(6)	Ports $\overline{74}$,75	Using as port VIN=VSS	2.5-6.0	-1			
Output high voltage	VOH(1)	Ports 0,1 of CMOS output	IOH=-1.0mA	4.5-6.0	VDD-1			V
	VOH(2)		IOH=-0.1mA	2.5-6.0	VDD-0.5			
	VOH(3)	•Port 9 of CMOS output •Ports A, B, C, D of CMOS output	IOH=-1.0mA	4.5-6.0	VDD-1			
	VOH(4)		IOH=-0.1mA	2.5-6.0	VDD-0.5			
Output low voltage	VOL(1)	Ports 0, 1	IOL=10mA	4.5-6.0			1.5	
	VOL(2)		IOL=1.6mA	4.5-6.0			0.4	
	VOL(3)		•IOL=1mA •The current of any unmeasurement pin is not over 1 mA.	2.5-6.0			0.4	
	VOL(4)	Port 70	IOL=1mA	4.5-6.0			0.4	
	VOL(5)		IOL=0.5mA	2.5-6.0			0.4	
	VOL(6)	Port 9	IOL=6mA	4.5-6.0			1.5	
	VOL(7)		IOL=1.2mA	4.5-6.0			0.4	
	VOL(8)	Port 9	•IOL=1mA •The current of any unmeasurement pin is not over 1 mA.	2.5-6.0			0.4	
	VOL(9)	Ports A, B, C, D of CMOS output	IOL=8mA	4.5-6.0			1.5	
	VOL(10)		IOL=1.6mA	4.5-6.0			0.4	
	VOL(11)		•IOL=1mA •The current of any unmeasurement pin is not over 1 mA.	2.5-6.0			0.4	

Continue.

Parameter	Symbol	Pins	Conditions	VDD[V]	Limits min.	typ.	max.	unit
LCD output regulation	VODLS	S0 to S13, S16 to S31	•Deference voltage to ideal value •VLCD, 2/3VLCD, 1/3VLCD	4.5-6.0	0		±0.2	V
				2.5-6.0	0		±0.2	
	VODLC	COM0 to COM3	•Deference voltage to ideal value •VLCD, 2/3VLCD, 1/2VLCD, 1/3VLCD	4.5-6.0	0		±0.2	
				2.5-6.0	0		±0.2	
LCD ladder resistor	PLCD(1)		Resistance at a ladder resistor	4.5-6.0		60		kΩ
				2.5-6.0		60		
	PLCD(2)		•Resistance at a ladder resistor •1/2R mode	4.5-6.0		30		
				2.5-6.0		30		
Pull-up MOS Tr. resistor	Rpu	•Ports 0, 1 •Ports A, B, C, D •Ports 70, 71, 72, 73	VOH=0.9VDD	4.5-6.0	15	40	70	
				2.5-4.5	25	70	150	
Hysteresis voltage	VHIS	•Ports 0, 1 •Ports 70, 71, 72, 73 • $\overline{\text{RES}}$	Output disable	2.5-6.0		0.1VDD		V
Pin capacitance	CP	All pins	•f=1MHz •Unmeasurement terminals for the input are set to VSS level. •Ta=25°C	2.5-6.0		10		pF

4. Serial input/output characteristics / Ta=-30°C to +70°C, VSS=VSS1=VSS2=VSS3=0V

Parameter			Symbol	Pins	Conditions	VDD[V]	Limits min.	typ.	max.	unit
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0, SCK1	Refer to figure 5.	2.5-6.0	2			tCYC
		Low Level pulse width	tCKL(1)				1			
		High Level pulse width	tCKH(1)				1			
	Output clock	Cycle	tCKCY(2)	SCK0, SCK1	•Use pull-up resistor (1kΩ) when open drain output. •Refer to figure 5.	2.5-6.0	2			
		Low Level pulse width	tCKL(2)					1/2 tCKCY		
		High Level pulse width	tCKH(2)					1/2 tCKCY		
Serial input	Data set up time		tICK	•SI0,SI1 •SB0,SB1	•Data set-up to SCK0, 1 •Data hold from SCK0, 1 •Refer to figure 5.	4.5-6.0	0.1			µs
						2.5-6.0	0.4			
	Data hold time		tCKI			4.5-6.0	0.1			
						2.5-6.0	0.4			
Serial output	Output delay time (Serial clock is external clock)		tCKO(1)	•SO0, SO1 •SB0, SB1	•Use pull-up resistor (1kΩ) when open drain output. •Data hold from SCK0, 1 •Refer to figure 5.	4.5-6.0			7/12tCYC +0.2	
						2.5-6.0			7/12tCYC +1	
	Output delay time (Serial clock is internal clock)		tCKO(2)			4.5-6.0			1/3tCYC +0.2	
						2.5-6.0			1/3tCYC +1	

5. Pulse input conditions / Ta=-30°C to +70°C, VSS=VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[V]	min.	typ.	max.	unit
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN	•Interrupt acceptable •Timer0-countable	2.5-6.0	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock is selected to 1/1.)	•Interrupt acceptable •Timer0-countable	2.5-6.0	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock is selected to 1/16.)	•Interrupt acceptable •Timer0-countable	2.5-6.0	32			
	tPIH(4) tPIL(4)	INT3/T0IN (The noise rejection clock is selected to 1/64.)	•Interrupt acceptable •Timer0-countable	2.5-6.0	128			
	tPIL(5)	$\overline{\text{RES}}$	Reset acceptable	2.5-6.0	200			µs

6. AD converter characteristics / Ta=-30°C to + 70°C, VSS=VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[V]	min.	typ.	max.	unit
Resolution	NAD			4.5-6.0		8		bit
Absolute precision (Note 2)	ETAD			4.5-6.0			±1.5	LSB
Conversion time	tCAD		AD conversion time = 16 × tCYC (ADCR2=0) (Note 3)	4.5-6.0	15.68 (tCYC= 0.98µs)		65.28 (tCYC= 4.08µs)	µs
			AD conversion time = 32 × tCYC (ADCR2=1) (Note 3)		31.36 (tCYC= 0.98vs)		130.56 (tCYC= 4.08µs)	
Analog input voltage range	VAIN	AN0 - AN11		4.5-6.0	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5-6.0			1	µA
	IAINL		VAIN=VSS	4.5-6.0	-1			

(Note 2) Absolute precision excepts quantizing error (±1/2 LSB).

(Note 3) The conversion time means the time from executing the AD conversion instruction to setting the complete digital conversion value to the register.

7. DA converter characteristics / Ta=-30°C to + 70°C, VSS=VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
Resolution	NDA			4.5-6.0		8		bit
Total error			8 bit mode	4.5-6.0			1.0	%
			9 bit mode				0.8	
			9.5 bit mode				0.7	
Settling time	tSAD		(Note 4)	4.5-6.0			0.5	μs
Analog output voltage range	VAOUT	DA0 to DA3	8 bit mode	4.5-6.0	VSS		VDD	V
			9 bit mode (1)		VSS		1/2VDD	
			9 bit mode (2)		1/2VDD		VDD	
			9.5 bit mode		1/3VDD		2/3VDD	
Output resistor	RODA		(Note 5)	4.5-6.0		4		kΩ

(Note 4) Settling time means the time from executing the DA conversion instruction to generating the analog voltage output corresponding to the digital data on the specific port.

(Note 5) DA data = 80H

8. Current dissipation characteristics / Ta=-30°C to +70°C, VSS=VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
Current dissipation during basic operation (Note 6)	IDDOP(1)	VDD1= VDD2= VDD3	•FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/1 divided	4.5-6.0		10	20	mA
	IDDOP(2)		•FmCF=3MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/2 divided	4.5-6.0		3	11	
	IDDOP(3)			2.5-4.5		1.5	6	
	IDDOP(4)		•FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation •1/2 divided	4.5-6.0		0.7	2.3	
	IDDOP(5)			2.5-4.5		0.4	1.6	
	IDDOP(6)		•FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : crystal oscillation •Internal RC oscillation stops •1/2 divided	4.5-6.0		35	130	µA
	IDDOP(7)			2.5-4.5		15	70	

Continue.

Parameter	Symbol	Pins	Conditions	VDD[V]	Limits min.	typ.	max.	unit
Current dissipation in HALT mode (Note 6)	IDDHALT(1)	VDD1= VDD2= VDD3	•HALT mode •FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/1 divided	4.5-6.0		5	11	mA
	IDDHALT(2)		•HALT mode	4.5-6.0		2.2	9	
	IDDHALT(3)		•FmCF=3MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/2 divided	2.5-4.5		0.8	5	
	IDDHALT(4)		•HALT mode	4.5-6.0		400	1100	µA
	IDDHALT(5)		FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation •1/2 divided	2.5-4.5		200	700	
	IDDHALT(6)		•HALT mode	4.5-6.0		25	100	
	IDDHALT(7)		FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : crystal oscillation •Internal RC oscillation stops •1/2 divided	2.5-4.5		8	55	
Current dissipation in HOLD mode (Note 6)	IDDHOLD(1)	VDD1= VDD2= VDD3	HOLD mode	4.5-6.0		0.05	30	
	IDDHOLD(2)			2.5-4.5		0.02	20	

(Note 6) The currents of the output transistors and the pull-up MOS transistors are ignored.

Table 1. Ceramic resonator oscillation recommended constant (main clock)

Oscillation type	Maker	Oscillator	C1	C2
8MHz ceramic resonator oscillation				
7MHz ceramic resonator oscillation				
6MHz ceramic resonator oscillation				
3MHz ceramic resonator oscillation				

* Both C1 and C2 must use K rank (±10%) and SL characteristics.

Table 2. Crystal oscillation guaranteed constant (sub clock)

Oscillation type	Maker	Oscillator	C3	C4
32.768kHz crystal oscillation				

* Both C3 and C4 must use J rank (±5%) and CH characteristics.
(It is about the application which is not in need of high precision. Use K rank (±10%) and SL characteristics.)

(Notes) •Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
•If you use other oscillators herein, we provide no guarantee for the characteristics.

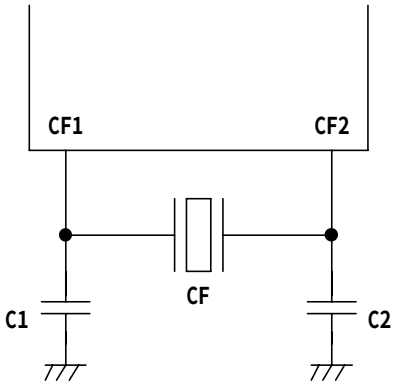


Figure 1 Ceramic oscillation circuit

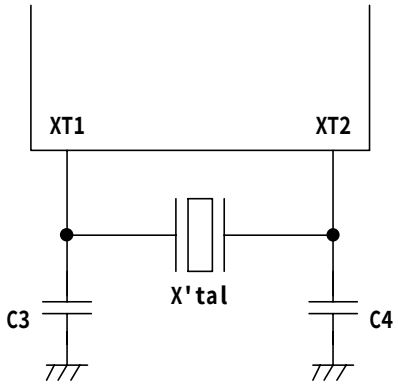


Figure 2 Crystal oscillation circuit

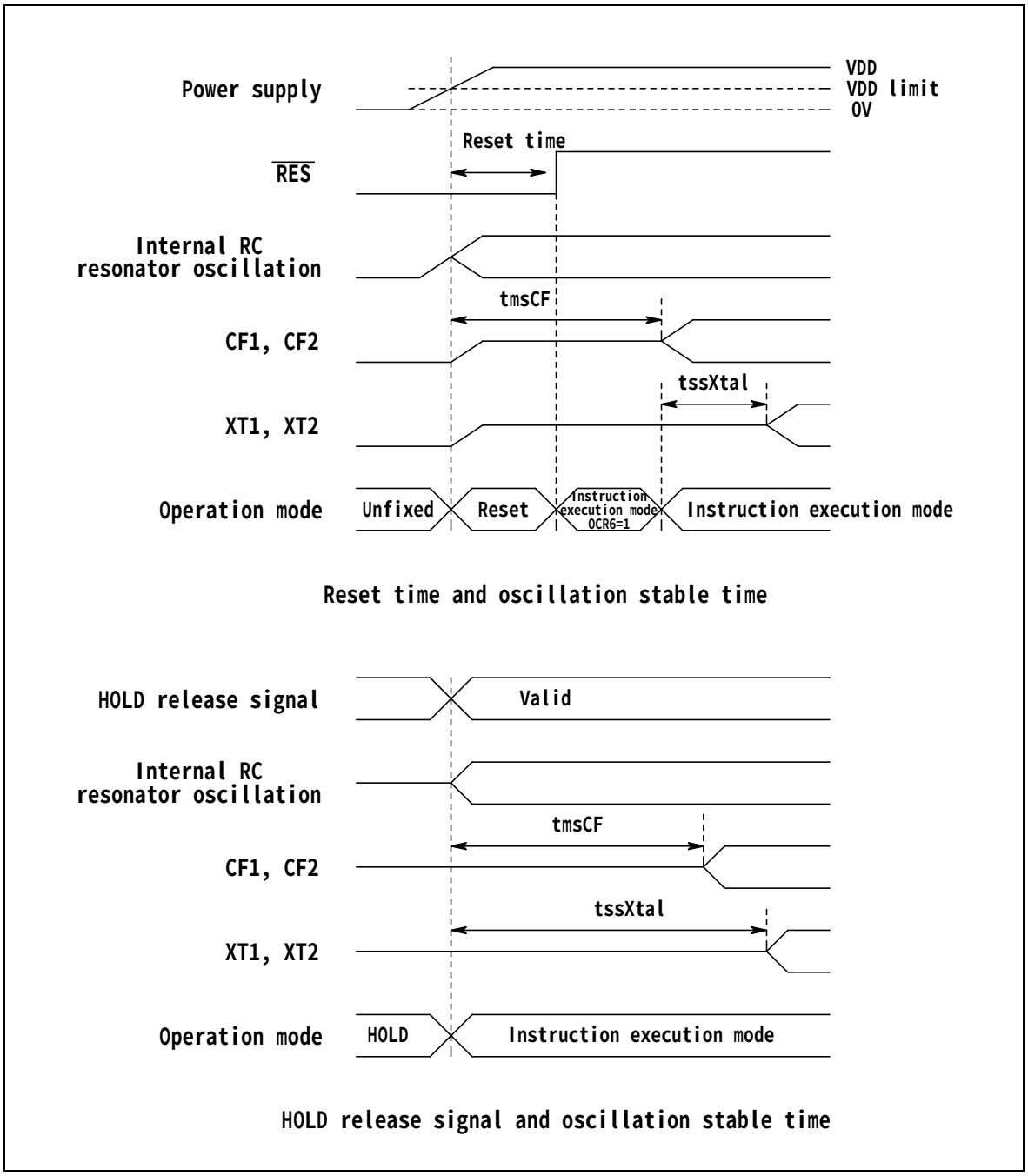
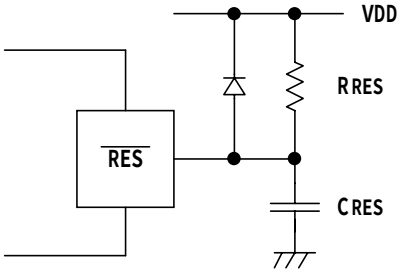


Figure 3 Oscillation stable time



(Note) Fix the value of CRES, RRES that is sure to reset until 200µs, after Power supply has been over inferior limit of supply voltage.

Figure 4 Reset circuit

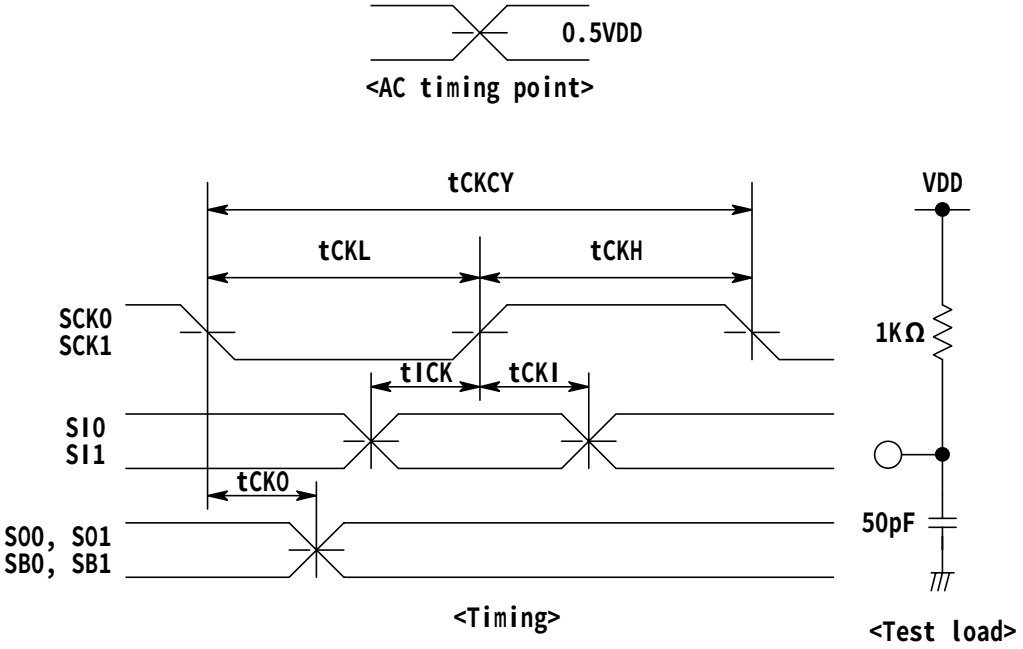


Figure 5 Serial input / output test condition

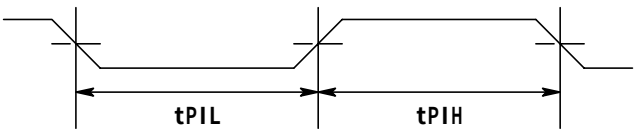


Figure 6 Pulse input timing condition

memo:

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