LC876132A/24A/16A

8-BIT SINGLE CHIP MICROCONTROLLER

UnderDevelopment

LC876132A

8 bit Single Chip Microcontroller incorporating 32 KB ROM and 768 byte RAM on chip

LC876124A

8 bit Single Chip Microcontroller incorporating 24 KB ROM and 768 byte RAM on chip

LC876116A

8 bit Single Chip Microcontroller incorporating 16 KB ROM and 768 byte RAM on chip

Overview

The LC876132A/24A/16A are 8 bit single chip microcontrollers with the following on-chip functional blocks :

- CPU: operable at a minimum bus cycle time of 100ns
- On-chip ROM Maximum Capacity : LC876132A 32K bytes
  LC876124A 24K bytes
  LC876116A 16K bytes
- On-chip RAM: 768 bytes
- VFD automatic display controller / driver
- 16 bit timer / counter (can be divided into two 8 bit timers)
- 16 bit timer / PWM (can be divided into two 8 bit timers)
- System clock divider function
- Synchronous serial I/O port (with automatic block transmit / receive function)
- Asynchronous / synchronous serial I/O port
- 10-channel × 8-bit AD converter
- 13-source 10-vectored interrupt system

All of the above functions are fabricated on a single chip.

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Features

(1) Read-Only Memory (ROM):
- LC876132A 32768 × 8 bits
- LC876124A 24576 × 8 bits
- LC876116A 16384 × 8 bits

(2) Random Access Memory (RAM): LC876132A/24A/16A 768 × 9 bits

(3) Minimum Bus Cycle Time: 100 ns (10MHz)

Note: The bus cycle time indicates ROM read time.

(4) Minimum Instruction Cycle Time: 300 ns (10MHz)

(5) Ports

- Input/output ports
  - Data direction programmable for each bit individually : 12 (P1n, P70 to P73)
  - Data direction programmable in nibble unit : 8 (P0n)
  - (When N-channel open drain output is selected, data can be input in bit unit.)
- VFD output ports
  - Large current outputs for digits : 9 (S0 / T0 to S8 / T8)
  - Large current outputs for digits / segments : 7 (S9 / T9 to S15 / T15)
  - Digit / segment outputs : 8 (S16 to S23)
  - Segment outputs : 28 (S24 to S51)
  - Other functions
  - Input ports : 16 (PCn, PDn)
  - Output ports : 8 (PFn)
  - Input/output ports : 4 (PGn)
- Oscillator pins : 2 (CF1,CF2)
- Reset pin : 1 ($\overline{\text{RES}}$)
- Power supply : 4 (VSS1, VDD1 to 3)
- VFD power supply : 1 (VP)

(6) VFD automatic display controller

- Programmable segment/digit output pattern
  - Output can be switched between digit/segment waveform output (pins 9 to 24 can be used for output of digit waveforms).
  - parallel-drive available for large current VFD.
- 16-step dimmer function available

(7) Timers

- Timer 0: 16 bit timer / counter with capture register
  - Mode 0: 2 channel 8-bit timer with programmable 8 bit prescaler and 8 bit capture register
  - Mode 1: 8 bit timer with 8 bit programmable prescaler and 8 bit capture register + 8 bit Counter with 8-bit capture register
  - Mode 2: 16 bit timer with 8 bit programmable prescaler and 16 bit capture register
  - Mode 3: 16 bit counter with 16 bit capture register
- Timer 1: PWM / 16 bit timer toggle output
  - Mode 0: 2 channel 8 bit timer (with toggle output)
  - Mode 1: 2 channel 8 bit PWM
  - Mode 2: 16 bit timer (with toggle output) Toggle output also possible using lower 8 bits.
  - Mode 3: 16 bit timer (with toggle output) Lower 8 bits can be used as PWM output.

(8) Serial-interface

- SIO 0: 8 bit synchronous serial interface
  1) LSB first / MSB first is selectable
  2) Internal 8 bit baud-rate generator (maximum transmit clock period 4 / 3 Tcyc)
  3) Continuous automatic data communication (1-256 bits)
- SIO 1: 8 bit asynchronous / synchronous serial interface
  Mode 0: Synchronous 8 bit serial IO (2-wire or 3-wire, transmit clock 2–512 Tcyc)
  Mode 1: Asynchronous serial IO (half duplex, 8 data bits, 1 stop bit, baud rate 8–2048Tcyc)
  Mode 2: Bus mode 1 (start bit, 8 data bits, transmit clock 2–512 Tcyc)
  Mode 3: Bus mode 2 (start detection, 8 data bits, stop detection)

(9) AD converter

-8 bits × 10 channels

(10) Remote control receiver circuit (connected to P73 / INT3 / T0IN terminal)

-Noise rejection function (noise rejection filter time constant can selected from 1 / 32 / 128 Tcyc)

(11) Watchdog timer

- The watching timer period is determined by an external RC.
- Watchdog timer can produce interrupt, system reset

(12) Interrupts: 13-source, 10-vectored interrupts

1) Three priority, low (L), high (H) and highest (X), multiple interrupts are supported. During interrupt handling, an equal or lower priority interrupt request is postponed.
2) If interrupt requests to two or more vector addresses occur at once, the higher priority interrupt takes precedence. In the case of equal priority levels, the vector with the lowest address takes precedence.

No.	Vector	Selectable Level	Interrupt signal
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L
4	0001BH	H or L	INT3
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0
8	0003BH	H or L	SIO1
9	00043H	H or L	ADC
10	0004BH	H or L	VFD automatic display controller / Port0

- Priority Level : X > H > L
- For equal priority levels, vector with lowest address takes precedence.

(13) Subroutine stack levels: 384 levels max. Stack is located in RAM.

(14) Multiplication and division

- 16 bits × 8 bits (executed in 5 cycles)
- 24 bits × 16 bits (executed in 12 cycles)
- 16 bits ÷ 8 bits (executed in 8 cycles)
- 24 bits ÷ 16 bits (executed in 12 cycles)

(15) Oscillation circuits

- On-chip RC oscillation circuit for system clock use.
- On-chip CF oscillation circuit for system clock use. (R_f built in)
- Frequency variable RC oscillation Circuit (imbedded) for system clock use.

(16) System clock divider function

- Able to reduce current consumption

Available minimum instruction cycle time: 300ns, 600ns, 1.2µs, 2.4µs, 4.8µs, 9.6µs, 19.2µs, 38.4µs, 76.8µs. (Using 10MHz main clock)

(17) Standby function

- HALT mode

HALT mode is used to reduce power consumption. Program execution is stopped. Peripheral circuits still operate but VFD display and some serial transfer operations stop.

1) Oscillation circuits are not stopped automatically.

2) Release occurs on system reset or by interrupt.

-HOLD mode

HOLD mode is used to reduce power consumption. Both program execution and peripheral circuits are stopped.

1)CF, RCand crystal oscillation circuits stop automatically.

2) Release occurs on any of the following conditions.

(1) Input to the reset pin goes low

(2) A specified level is input at least one of INT0, INT1, INT2

(3) An interrupt condition arises at port 0

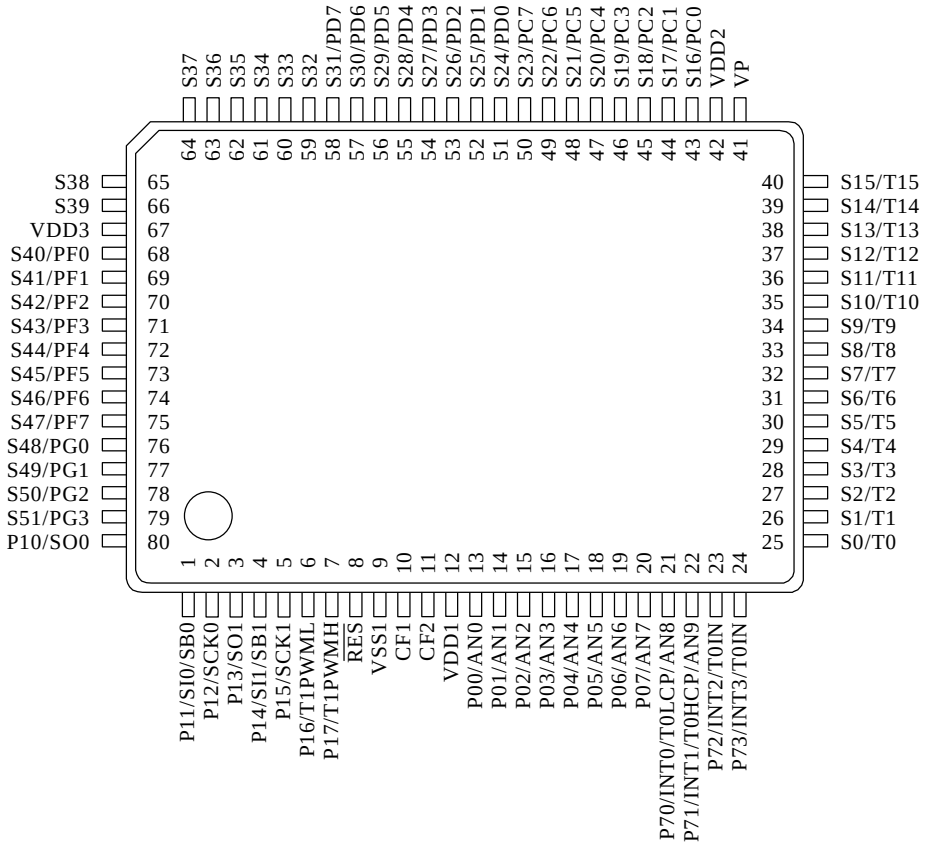
(18) Factory shipment

- QIP80E

(19) Development tools

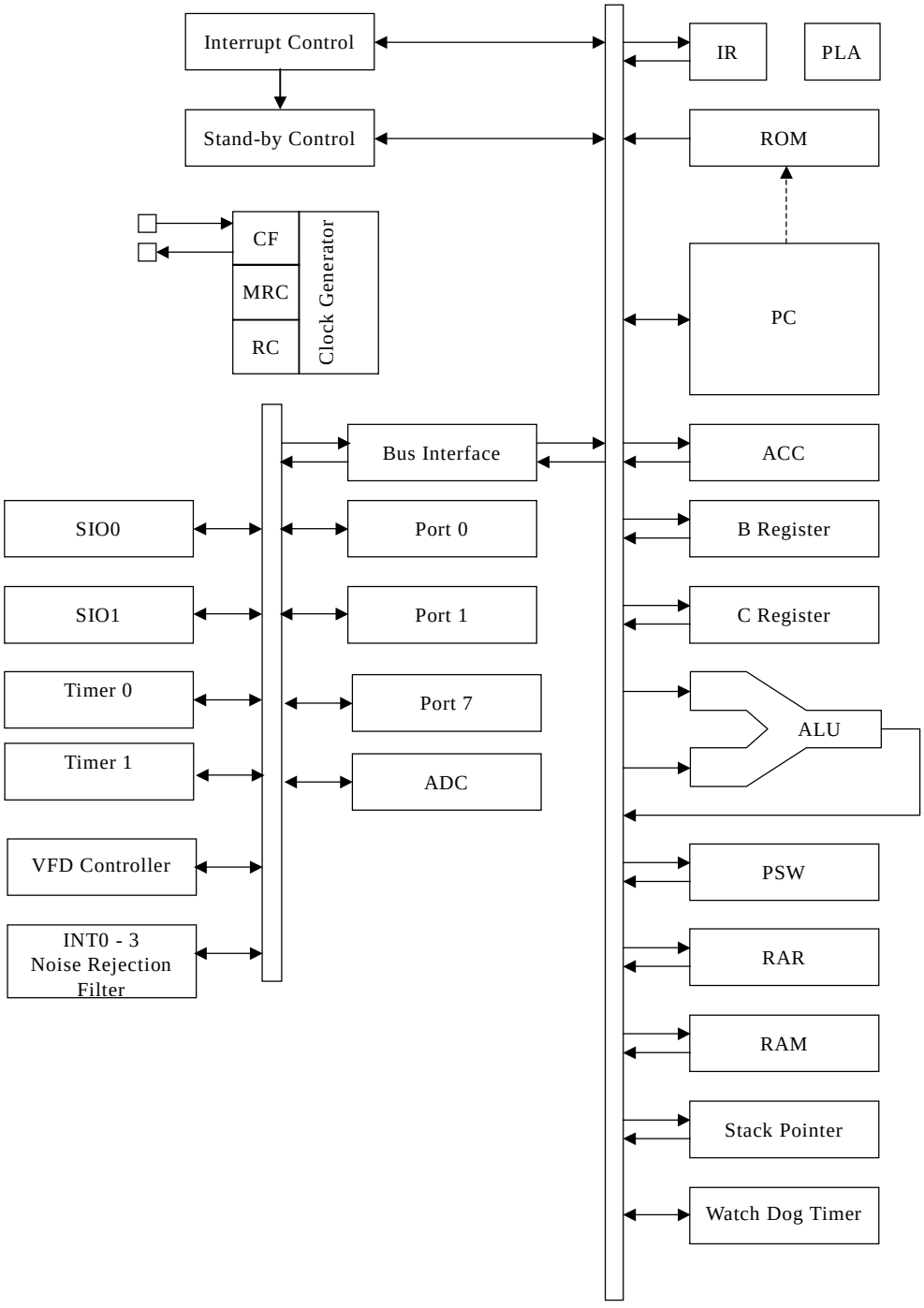
- Evaluation chip: LC876093
- Emulator: EVA62S + ECB876600 (Evaluation chip board) + SUB876100 + POD80QFP
  : ICE-B877300 + SUB876100 + POD80QFP
  : Flash ROM Version : LC87F6164A

Pin Assignment



SANYO: QIP80E

System Block Diagram



Pin Assignment

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function</th><th>Option</th></tr>
<tr><td>VSS1</td><td>-</td><td>• Power supply (-)</td><td>No</td></tr>
<tr><td>VDD1
VDD2
VDD3</td><td>-</td><td>• Power supply (+)</td><td>No</td></tr>
<tr><td>VP</td><td>-</td><td>• Power supply (-)</td><td>No</td></tr>
<tr><td>PORT0
P00 to P07</td><td>I/O</td><td>• 8bit input/output port
• data direction programmable in nibble units
• Use of pull-up resistors for P1 to P3 and P4 to P7 can be specified in three bit unit and nibble unit respectively.
• Input for HOLD release
• Input for port 0 interrupt
• Other function
A/D conversion input port: AN0 to AN7</td><td>Yes
(P00 has no option)</td></tr>
<tr><td>PORT1
P10 to P17</td><td>I/O</td><td>• 8-bit input/output port
• Data direction programmable for each bit
• Use of pull-up resistor can be specified for each bit
• Other pin functions
P10 SIO0 data output
P11 SIO0 data input/bus input/output
P12 SIO0 clock input/output
P13 SIO1 data output
P14 SIO1 data input/bus input/output
P15 SIO1 clock input/output
P16: Timer 1 PWML output
P17: Timer 1 PWMH output/Buzzer output</td><td>Yes</td></tr>
<tr><td>PORT7
P70 to P73</td><td>I/O</td><td>• 4-bit Input/output port
• Data direction can be specified for each bit
• Use of pull-up resistor can be specified
• Other functions
P70: INT0 input/HOLD release input/Timer0L capture Input/output for watchdog timer
P71: INT1 input/HOLD release input/Timer0H capture input
P72: INT2 input/HOLD release input/timer 0 event input/Timer0L capture input/High speed clock counter input
P73: INT3 input(noise rejection filter attached input)/timer 0 event input/Timer 0H capture input
AD input port: AN8(P70), AN9(P71)
The following types of interrupt detection are possible:
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/ falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>Yes</td><td>Yes</td><td>No</td><td>Yes</td><td>Yes</td></tr>
<tr><td>INT1</td><td>Yes</td><td>Yes</td><td>No</td><td>Yes</td><td>Yes</td></tr>
<tr><td>INT2</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
<tr><td>INT3</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
</table></td><td>No</td></tr>
</table>

Pin name	I/O	Function description	Option
S0/T0 to S8/T8	O	• Large current output for VFD display controller digit (can be used for segment)	No
S9/T9 to S15/T15	O	• Large current output for VFD display controller segment/digit	No
S16 to S23	I/O	• Output for VFD display controller segment/digit • Other functions: High voltage input port: PC0 to PC7	No
S24 to S31	I/O	• Output for VFD display controller segment • Other functions: High voltage input port: PD0 to PD7	No
S32 to S39	O	• Output for VFD display controller segment	No
S40 to S47	O	• Output for VFD display controller segment • Other functions: High voltage output port: PF0 to PF7	No
S48 to S51	I/O	• Output for VFD display controller segment • Other functions: High voltage input/output port: PG0 to PG3	No
$\overline{\text{RES}}$	I	Reset terminal	No
CF1	I	Input terminal for ceramic oscillator	No
CF2	O	Output terminal for ceramic oscillator	No

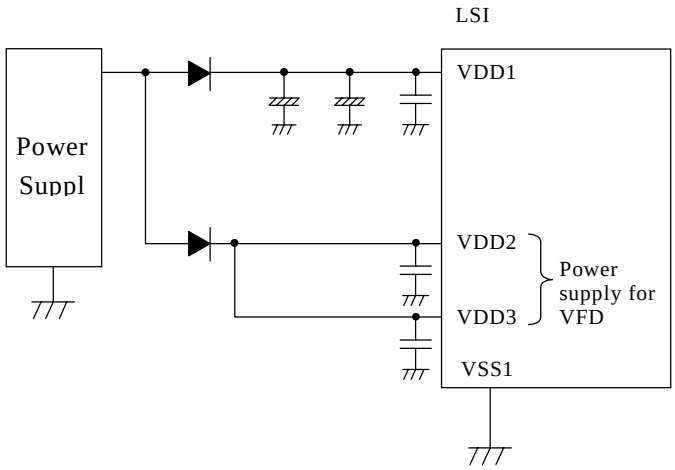
Port Output Configuration

Output configuration and pull-up/pull-down resistor options are shown in the following table.
Input /output is possible even when port is set to output mode.

Terminal	Option applies to:	Options	Output Format	Pull-up resistor	Pull-down resistor
P00	-	None	N-ch open drain	None	-
P01 to P07	1 bit unit	1	CMOS	Programmable (Note 1)	-
		2	Nch-open drain	None	-
P10 to P17	1 bit unit	1	CMOS	Programmable	-
		2	Nch-open drain	Programmable	-
P70	-	None	Nch-open drain	Programmable	-
P71 to P73	-	None	CMOS	Programmable	-
S0/T0 to S6/T6	-	None	High voltage Pch-open drain	-	None
S7/T7 to S15/T15	-	None	High voltage Pch-open drain	-	Fixed
S16 to S31	-	None	High voltage Pch-open drain	-	None
S32 to S47	-	None	High voltage Pch-open drain	-	Fixed
S48 to S51	-	None	High voltage Pch-open drain	-	None

Note 1 Pull-up resisters for Port 0 can be attached in three-bit unit (P01-03) and nibble unit (P04-07) by the program.

* Note 1: Connect as follows to reduce noise on VDD and increase the back-up time.



1. Absolute maximum ratings / Ta=25°C and VSS1=0V

Parameter		Symbol	Pins	Conditions	VDD[V]	Limits min.	typ.	max.	unit
Supply voltage		VDDMAX	VDD1,VDD2,VDD3	VDD1=VDD2 =VDD3		-0.3		+6.5	V
Input voltage		VI(1)	CF1, $\overline{RES}$			-0.3		VDD+0.3	
		VI(2)	VP			VDD-45		VDD+0.3	
Output voltage		VO(1)	S0/T0 to S15/T15 S32 to S47			VDD-45		VDD+0.3	
Input/Output voltage		VIO(1)	•Port 0 •Port 1 •Port 7			-0.3		VDD+0.3	
		VIO(2)	S16 to S31, S48 to S51			VDD-45		VDD+0.3	
High level output current	Peak output current	IOPH(1)	Port 0, 1	•CMOS output selected •Current at each pin		-10			mA
		IOPH(2)	Port71,72,73	Current at each pin		-3			
		IOPH(3)	S0/T0 to S15/T15	Current at each pin		-30			
		IOPH(4)	S16 to S51	Current at each pin		-15			
	Total output current	ΣIOAH(1)	Port 0	Total of all pins		-30			
		ΣIOAH(2)	Port 1	Total of all pins		-30			
		ΣIOAH(3)	Port 7	Total of all pins		-5			
		ΣIOAH(4)	S0/T0 to S15/T15	Total of all pins		-65			
		ΣIOAH(5)	S16 to S27	Total of all pins		-60			
		ΣIOAH(6)	S28 to S39	Total of all pins		-60			
		ΣIOAH(7)	S40 to S51	Total of all pins		-60			
Low level output current	Peak output current	IOPL(1)	Port 0, 1	For each pin				20	
		IOPL(2)	Port 7	For each pin				5	
	Total output current	ΣIOAL(1)	Port 0	Total of all pins				60	
		ΣIOAL(2)	Ports 1, 7	Total of all pins				60	
Maximum power consumption		Pdmax	QIP80E	Ta = -30 to +70°C				478	mW
Operating temperature range		Topr				-30		+70	°C
Storage temperature range		Tstg				-55		+125	

2. Recommended operating range / Ta=-30°C to +70°C, VSS1=0V

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[V]	min.	typ.	max.	unit
Operating supply voltage range	VDD(1)	VDD1=VDD2 =VDD3	0.294µs ≤ Tcyc ≤ 200µs		4.5		5.5	V
Hold voltage	VHD	VDD1	RAM and the register data are kept in HOLD mode.		2.0		5.5	
Pull-down voltage	VP	VP		4.5–5.5	-35		VDD	
Input high voltage	VIH(1)	•Port 0	Output disable	4.5–5.5	0.3VDD +0.7		VDD	
	VIH(2)	•Port 1 •Port 71, 72, 73 •P70 port input/interrupt	Output disable	4.5–5.5	0.3VDD +0.7		VDD	
	VIH(3)	S16 to S31 S48 to S51	Output P-channel Tr. OFF	4.5–5.5	0.33VDD +1.0		VDD	
	VIH(4)	Port 70 Watchdog timer	Output disable	4.5–5.5	0.9VDD		VDD	
	VIH(5)	CF1, $\overline{RES}$		4.5–5.5	0.75VDD		VDD	
Input low voltage	VIL(1)	•Port 0	Output disable	4.5–5.5	VSS		0.15VDD +0.4	
	VIL(2)	•Port 1 •Port 71, 72, 73 •P70 port input/interrupt	Output disable	4.5–5.5	VSS		0.1VDD +0.4	
	VIL(3)	S16 to S31 S48 to S51	Output P-channel Tr. OFF	4.5–5.5	VSS		0.2VDD	
	VIL(4)	Port 70 Watchdog timer	Output disabled	4.5–5.5	VSS		0.8VDD -1.0	
	VIL(5)	CF1, $\overline{RES}$		4.5–5.5	VSS		0.25VDD	
Operation cycle time	tCYC			4.5–5.5	0.294		200	µs
External system clock frequency	FEXCF(1)	CF1	•CF2 open circuit •system clock divider set to 1/1 •external clock DUTY = 50±5%	4.5–5.5	0.1		10	MHz
			•CF2 open circuit •system clock divider set to 1/2	4.5–5.5	0.2		20	
Oscillation stabilizing time period (Note 1)	FmCF(1)	CF1, CF2	10MHz ceramic resonator oscillation Refer to figure 1	4.5–5.5		10		
	FmCF(2)	CF1, CF2	4MHz ceramic resonator oscillation Refer to figure 1	4.5–5.5		4		
	FmMRC		Frequency Variable RC oscillation	4.5–5.5		50		
	FmRC		RC oscillation	4.5–5.5	0.3	1.0	2.0	

(Note 1) The oscillation constant is shown in table 1 and table 2.

3. Electrical characteristics / Ta=-30°C to +70°C, VSS1=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
Input high current	IIH(1)	Port 0,1,7	•Output disabled •Pull-up resister OFF. •VIN=VDD (including OFF state leak current of the output Tr.)	4.5–5.5			1	µA
	IIH(2)	S16 to S31 S48 to S51 (Port C, D,G)	When configured as an input port VIN=VDD				60	
	IIH(3)	$\overline{RES}$	VIN=VDD	4.5–5.5			1	
	IIH(4)	CF1	VIN=VDD	4.5–5.5			15	
Input low current	IIL(1)	Port 0,1,7	•Output disabled •Pull-up resister OFF •VIN=VSS (including OFF state leak current of the output Tr.)	4.5–5.5	-1			
	IIL(2)	$\overline{RES}$	VIN=VSS	4.5–5.5	-1			
	IIL(3)	CF1	VIN=VSS	4.5–5.5	-15			
Output high voltage	VOH(1)	Port 0,1	IOH=-1.0mA	4.5–5.5	VDD-1			V
	VOH(2)		IOH=-0.1mA	4.5–5.5	VDD-0.5			
	VOH(3)	Port 7	IOH=-0.4mA	4.5–5.5	VDD-1			
	VOH(4)	S0/T0–S15/T15	IOH=-20.0mA	4.5–5.5	VDD-1.8			
	VOH(5)		IOH=-1.0mA IOH at any single pin is not over 1mA.	4.5–5.5	VDD-1			
	VOH(6)	S16 to S51	IOH=-5.0mA	4.5–5.5	VDD-1.8			
	VOH(7)		IOH=-1.0mA IOH at any single pin is not over 1mA.	4.5–5.5	VDD-1			
Output low voltage	VOL(1)	Port 0,1	IOL=9mA	4.5–5.5			1.5	
	VOL(2)		IOL=1.5mA	4.5–5.5			0.4	
	VOL(3)	Port 7	IOL=1mA	4.5–5.5			0.4	
Pull-up resistor	Rpu	Port 0,1,7	VOH=0.9VDD	4.5–5.5	15	40	70	kΩ
Output off-leak current	IOFF(1)	S0/T0 to S6/S6, S16 to S31 S48 to S51	•Output P-ch Tr. OFF •VOUT=VSS	4.5–5.5	-1			µA
	IOFF(2)		•Output P-ch Tr. OFF •VOUT=VDD-40V	4.5–5.5	-30			
Resistance of the low level hold Tr.	Rinpd	S16 to S31 S48 to S51	•Output P-ch Tr. OFF	4.5–5.5		200		kΩ
High voltage pull-down resistor	Rpd	S7/S7 to S15/T15, S32 to S47	•Output P-ch Tr. OFF •VOUT=3V •Vp=-30V	5.0	60	100	200	
Hysteresis voltage	VHIS(1)	•Port 1,7 • $\overline{RES}$		4.5–5.5		0.1VDD		V
Pin capacitance	CP	All pins	•All other terminals connected to VSS. •f=1MHz •T_a=25°C	4.5–5.5		10		pF

4. Serial input/output characteristics / Ta=-30°C to +70°C, VSS1=0V

Parameter			Symbol	Pins	Conditions	Limits				
						VDD[V]	min.	typ.	max.	unit
Serial clock	Input clock	Cycle Time	tSCK(1)	SCK0(P12)	Refer to figure 5	4.5–5.5	4/3			tCYC
		Low Level pulse width	tSCKL(1)				2/3			
			tSCKLA(1)				2/3			
		High Level pulse width	tSCKH(1)				2/3			
			tSCKHA(1)				3			
		Cycle Time	tSCK(2)	SCK1(P15)	Refer to figure 5	4.5–5.5	2			
		Low Level pulse width	tSCKL(2)				1			
		High Level pulse width	tSCKH(2)				1			
	Output clock	Cycle Time	tSCK(3)	SCK0(P12)	•CMOS output option •Refer to figure 5	4.5–5.5	4/3			
		Low Level pulse width	tSCKL(3)					1/2		tSCK
			tSCKLA(2)					3/4		
		High Level pulse width	tSCKH(3)					1/2		
			tSCKHA(2)					2		
		Cycle Time	tSCK(4)	SCK1(P15)	•CMOS output option •Refer to figure 5	4.5–5.5	2			tCYC
		Low Level pulse width	tSCKL(4)					1/2		tSCK
		High Level pulse width	tSCKH(4)					1/2		
Serial input	Data set-up time		tsDI	SI0(P11), SI1(P14), SB0(P11), SB1(P14)	•Measured with respect to SI0CLK leading edge. •Refer to figure 5	4.5–5.5	0.03			µs
	Data hold time		thDI				0.03			
Serial output	Output delay time		tdDO	SO0(P10), SO1(P13), SB0(P11), SB1(P14)	•Measured with respect to SI0CLK trailing edge. •When port is open drain: Time delay from SI0CLK trailing edge to the SO data change. •Refer to figure 5	4.5–5.5			1/3 tCYC +0.05	

5. Pulse input conditions / Ta=-30°C to +70°C, VSS1=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72)	•Interrupt acceptable •Events to timer 0 can be input.	4.5–5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) (Noise rejection ratio set to 1/1.)	•Interrupt acceptable •Events to timer 0 can be input.	4.5–5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) (Noise rejection ratio set to 1/32.)	•Interrupt acceptable •Events to timer 0 can be input.	4.5–5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) (Noise rejection ratio set to 1/128.)	•Interrupt acceptable •Events to timer 0 can be input.	4.5–5.5	256			
	tPIL(5)	$\overline{\text{RES}}$	•Reset possible	4.5–5.5	200			µs

6. AD converter characteristics / Ta=-30°C to + 70°C, VSS1=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
Resolution	N	AN0(P00) to AN7(P07) AN8(P70), AN9(P71)		4.5–5.5		8		bit
Absolute precision	ET		(Note2)	4.5–5.5			±1.5	LSB
Conversion time	TCAD		AD conversion time = 32 × tCYC (ADCR2=0) (Note 3)	4.5–5.5	15.62 (tCYC= 0.488µs)		97.92 (tCYC= 3.06µs)	µs
			AD conversion time = 64 × tCYC (ADCR2=1) (Note 3)		18.82 (tCYC= 0.294µs)		97.92 (tCYC= 1.53µs)	
Analog input voltage range	VAIN			4.5–5.5	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5–5.5			1	µA
	IAINL		VAIN=VSS	4.5–5.5	-1			

(Note 2) Absolute precision not including quantizing error (±1/2 LSB).

(Note 3) Conversion time means time from executing AD conversion instruction to loading complete digital value to register.

7. Current consumption characteristics / Ta=-30°C to +70°C, VSS1= 0V

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[V]	min.	typ.	max	unit
Current consumption during basic operation (Note 4)	IDDOP(1)	VDD1= VDD2= VDD3	•FmCF=10MHz for Ceramic resonator oscillation •System clock: CF oscillation •Internal RC oscillation stopped. •Frequency variable RC oscillation stopped. •Divider set to 1/1	4.5–5.5		8	27	mA
	IDDOP(2)		•CF1=20MHz for external clock •System clock: CF oscillation •Internal RC oscillation stopped. •Frequency variable RC oscillation stopped. •Divider set to 1/2	4.5–5.5		8.5	28	
	IDDOP(3)		•FmCF=4MHz Ceramic resonator oscillation •System clock: CF oscillation •Internal RC oscillation stopped. •Frequency variable RC oscillation stopped. •Divider set to 1/1	4.5–5.5		3.5	15	
	IDDOP(4)		•FmCF=0Hz (No oscillation) •System clock: RC oscillation •Frequency variable RC oscillation stopped. •Divider set to 1/2	4.5–5.5		1	8.5	
	IDDOP(5)		•FmCF=0Hz (No oscillation) •Internal RC oscillation stopped. •System clock: Frequency Variable RC oscillation •Divider set to 1/2	4.5–5.5		2.0	10.5	

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[V]	Min	Typ	Max	Unit
Current consumption HALT mode (Note 4)	IDDHALT(1)	VDD1= VDD2= VDD3	HALT mode •FmCF=10MHz for Ceramic resonator oscillation •System clock : CF oscillation •Internal RC oscillation stopped. •Divider: 1/1	4.5 to 5.5		3	11	Ma
	IDDHALT(2)		HALT mode •CF1=20MHz for external clock •System clock : CF oscillation •Internal RC oscillation stopped. •Frequency variable RC oscillation stopped. •Divider 1/2	4.5 to 5.5		3.5	12	
	IDDHALT(3)	VDD1= VDD2= VDD3	HALT mode •FmCF=4MHz for Ceramic resonator oscillation •System clock : CF oscillation •Internal RC oscillation stopped. •Divider: 1/1	4.5 to 5.5		1.5	6	mA
	IDDHALT(4)		HALT mode •FmCF=0Hz (When oscillation stops.) •System clock : RC oscillation •Divider: 1/2	4.5 to 5.5		400	1600	µA
	IDDHALT(5)		HALT mode •FmCF=0Hz (When oscillation stops.) •Internal RC oscillation stopped. •System clock : Frequency variable RC oscillation 1MHz •Divider: 1/2	4.5 to 5.5		1400	3600	
Current consumption HOLD mode	IDDHOLD(1)	VDD1	HOLD mode •CF1=VDD or open circuit (when using external clock)	4.5 to 5.5		0.025	25	µA

(Note 4) The currents of the output transistors and the pull-up MOS transistors are ignored.

Main system clock oscillation circuit characteristics

The characteristics in the table bellow is based on the following conditions:

1. Use the standard evaluation board SANYO has provided.
2. Use the peripheral parts with indicated value externally.
3. The peripheral parts value is a recommended value of oscillator manufacturer

Table 1. Main system clock oscillation circuit characteristics using ceramic resonator

Frequency	Manufacturer	Oscillator	Circuit parameters			Operating supply voltage range	Oscillation stabilizing time		Notes
			C1	C2	Rd1		typ	max	
10MHz	Murata	CSTLS10M0G53-B0	(15pF)	(15pF)	0Ω	4.5 - 5.5V	0.03mS	0.25mS	With C1, C2
		CSTCC10M0G53-R0	(15pF)	(15pF)	100Ω	4.5 - 5.5V	0.03mS	0.25mS	With C1, C2
4MHz	Murata	CSTLS4M00G53-R0	(15pF)	(15pF)	330Ω	4.5 - 5.5V	0.03mS	0.25mS	With C1, C2
		CSTCR4M00G53-R0	(15pF)	(15pF)	330Ω	4.5 - 5.5V	0.05mS	0.3mS	With C1, C2
	Kyosera	PBRC4.00HR	(33pF)	(33pF)	0Ω	4.5 - 5.5V	0.15mS	1.0mS	With C1, C2
		KBR-4.0MKC	(33pF)	(33pF)	0Ω	4.5 - 5.5V	0.15ms	1.0mS	With C1, C2

The oscillation stabilizing time is a period until the oscillation becomes stable after VDD becomes higher than minimum operating voltage. (Refer to Figure 3)

(Notes) • Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close tothe oscillation pins as possible with the shortest possible pattern length.

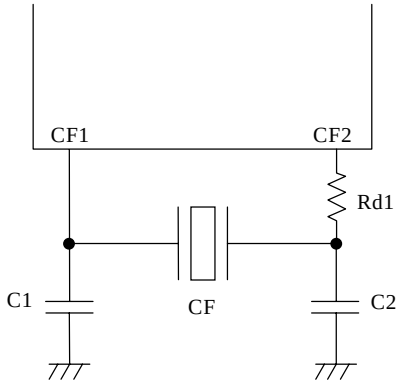


Figure 1 Ceramic oscillation circuit

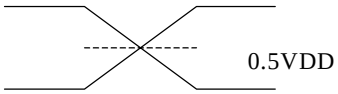


Figure 2 AC timing measurement point

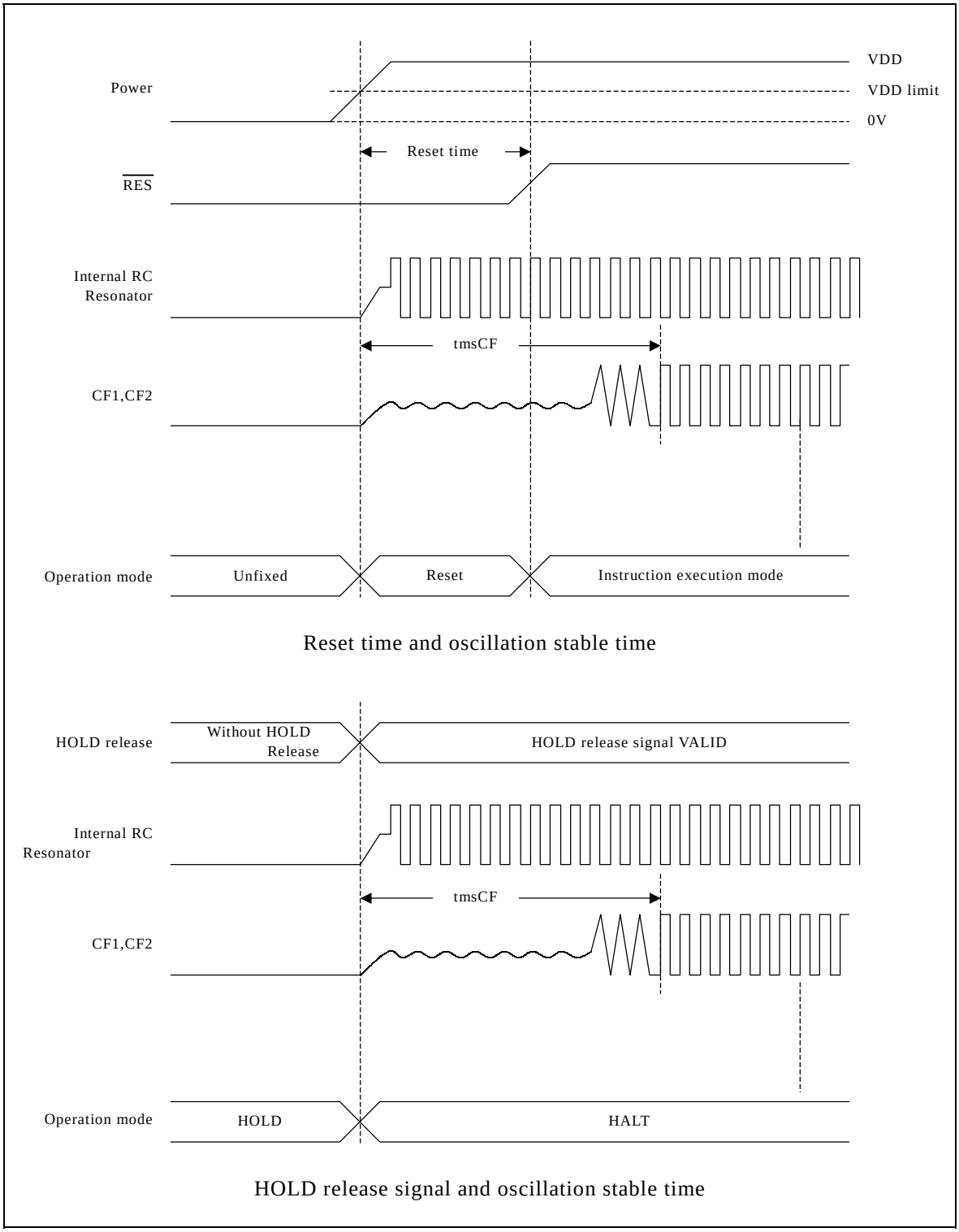
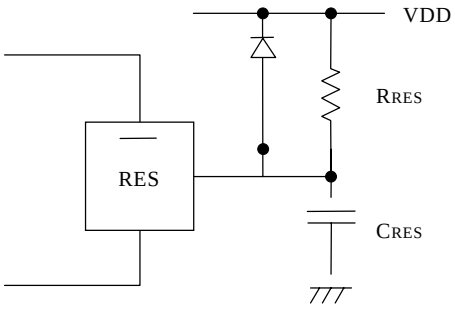


Figure 3 Oscillation stabilization time



(Note) Set CRES, RRES values such that reset time exceeds 200µs.

Figure 4 Reset circuit

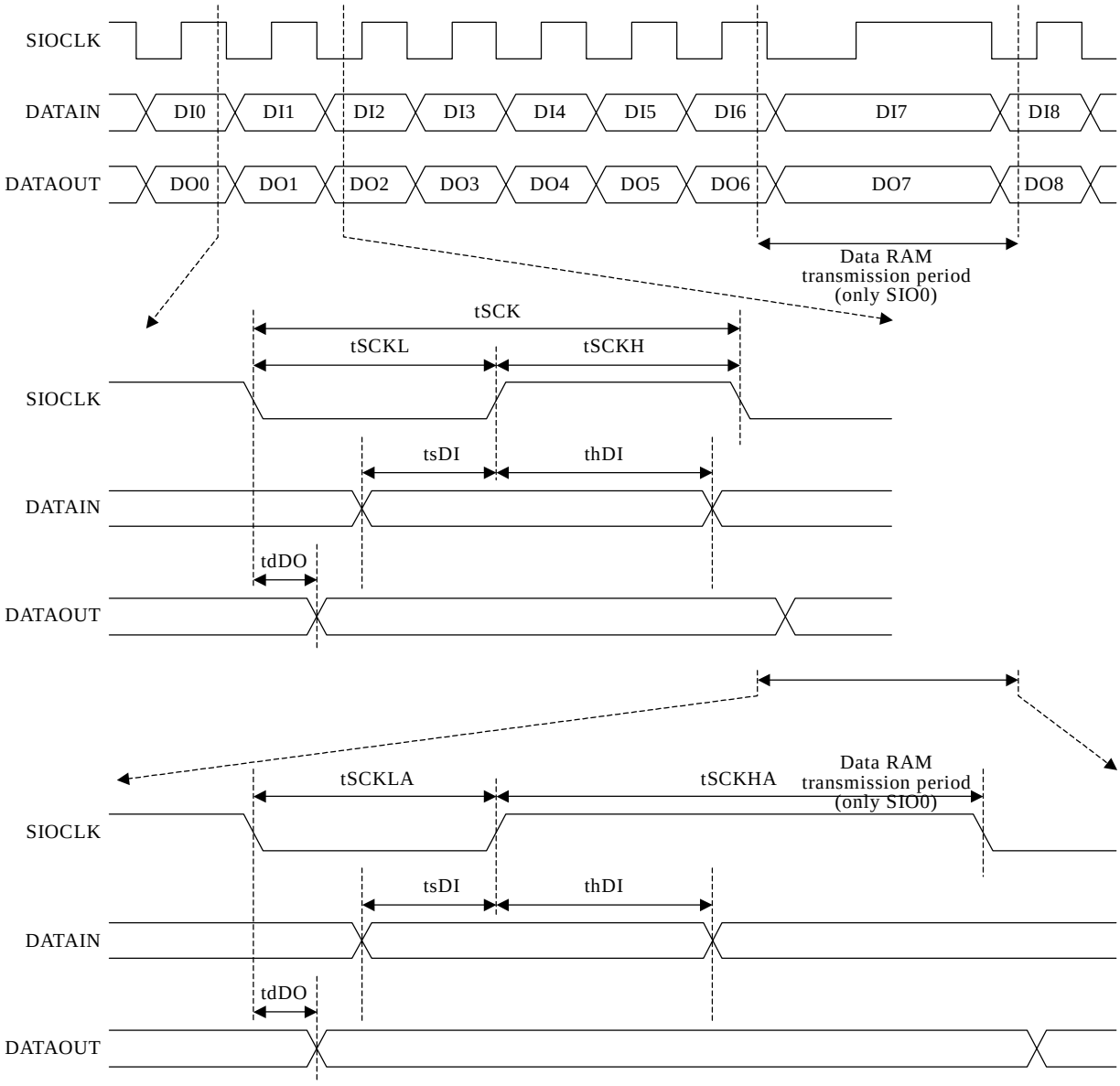


Figure 5 Serial input / output test condition

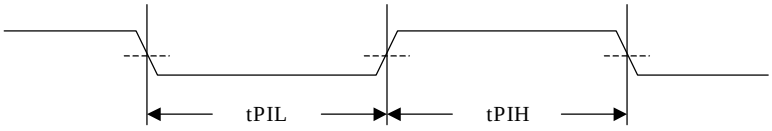


Figure 6 Pulse input timing condition

This catalog provides information as of June, 2001. Specifications and information herein are subject to change without notice