LC87F6164A

8 bit Single Chip Microcontroller With 64K-byte FROM and 1024 byte RAM

UnderDevelopment

LC87F6164A

8 bit Single Chip Microcontroller incorporating 64K-byte FROM and 1024 byte RAM on chip

Overview

The LC87F6164A is an 8-bit single chip microcontroller with the following one-chip features:

- CPU: Operable at a minimum bus cycle time of 100 ns
- on-chip Flash ROM Capacity : 64K bytes (on-board rewritable)
- on-chip RAM Capacity : 1024 bytes
- VFD automatic display controller / driver
- 16-bit timer / counter (can be divided into two 8 bit timers)
- 16-bit timer / PWM (can be divided into two 8 bit timers)
- system clock divider
- synchronous serial I/O port (with automatic block transmit / receive function)
- asynchronous / synchronous serial I/O port
- 10-channel × 8-bit AD converter
- 13-source 10-vectored interrupt system

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Features

(1) Read Only Memory (Flash ROM)
-single 5V power supply, on-board rewritable
-block erase in 128 byte units
-65536 × 8bits (LC87F6164A)

(2) Random Access Memory (RAM): 1024 × 9 bits (LC87F6164A)

(3) Minimum Bus Cycle Time: 100 ns (10 MHz)
Note: Bus cycle time indicates the speed to read ROM.

(4) Minimum Instruction Cycle Time: 300 ns (10MHz)

(5) Ports
- Input/output ports
  - Input/output programmable for each bit individually : 12 (P1n, P70 to P73)
  - Data direction programmable in nibble units : 8 (P0n)
  - (When N-channel open drain output is selected, data can be input by bit.)
- VFD output ports
  - Large current outputs for digits : 9 (S0 / T0 to S8 / T8)
  - Large current outputs for digits / segments : 7 (S9 / T9 to S15 / T15)
  - digit / segment outputs : 8 (S16 to S23)
  - segment outputs : 28 (S24 to S51)
  - Other functions
  - Input ports : 16 (PCn, PDn,)
  - Output ports : 8 (PFn)
  - Input/output ports : 4 (PGn)
- Oscillator pins : 2 (CF1,CF2)
- Reset pin : 1 (RES#)
- Power supply : 4 (VSS1, VDD1 to VDD3)
- VFD power supply : 1 (VP)

(6) VFD automatic display controller
- Programmable segment/digit output pattern
  - Output can be toggled between digit/segment waveform output.
  - (pins 9 - 24 can be used for the digit output)
  - parallel-drive available for large current VFD
- 16-step dimmer function available

(7) Timers
- Timer 0: 16 bit timer / counter with capture register
  - Mode 0: Two 8-bit timers with 8-bit programmable prescaler and 8-bit capture register
  - Mode 1: 8-bit timer with 8-bit programmable prescaler and 8-bit capture register + 8-bit counter with 8-bit capture register
  - Mode 2: 16-bit timer with 8-bit programmable prescaler and 16-bit capture register
  - Mode 3: 16-bit counter with 16-bit capture register

- Timer 1: PWM/16-bit timer with toggle output
  - Mode 0: Two 8-bit timers with toggle output
  - Mode 1: Two 8-bit PWM
  - Mode 2: 16-bit timer with toggle output (Toggle output is also possible by using the lower order 8 bits)
  - Mode 3: 16-bit timer with toggle output (The lower order 8 bits can be used as PWM output)

(8) Serial interface

- SIO 0: 8 bit synchronous serial interface
  1) LSB first / MSB first function available
  2) An internal 8-bit baud-rate generator (maximum transmit clock period 4 / 3 Tcyc)
  3) Consecutive automatic data communication (1 - 256 bits)
- SIO 1: 8 bit asynchronous / synchronous serial interface
  - Mode 0: Synchronous 8 bit serial IO (2-wire or 3-wire, transmit clock 2 - 512 Tcyc)
  - Mode 1: Asynchronous serial IO (half duplex, 8 data bits, 1 stop bit, baud rate 8 - 2048Tcyc)
  - Mode 2: Bus mode 1 (start bit, 8 data bits, transmit clock 2 - 512 Tcyc)
  - Mode 3: Bus mode 2 (start detection, 8 data bits, stop detection)

(9) AD converter

-10 channels × 8-bit AD converter

(10) Remote receiver circuit (share with P73 / INT3 / T0IN terminal)

-Noise rejection function (The filtering time of the noise rejection filter (1 / 32 / 128 Tcyc) can be switched by program)

(11) Watchdog timer

- External RC circuit is required.
- Interrupt or system reset is activated when the timer overflows.

(12) Interrupts: 13-source and 10-vectored interrupt function

1) Three interrupt priorities, low (L), high (H) and highest (X) are supported with multi-level nesting. During interrupt handling, an equal or lower level interrupt request is refused.
2) If interrupt requests for two or more vector addresses occur at once, the higher level interrupt takes precedence. In the case of equal priority levels, the vector with the lowest address takes precedence.

No.	Vector	Selectable Level	Interrupt signal
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L
4	0001BH	H or L	INT3
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0
8	0003BH	H or L	SIO1
9	00043H	H or L	ADC
10	0004BH	H or L	VFD automatic display controller/Port 0

• Priority Level : X > H > L

• For equal priority levels, vector with lowest address takes precedence.

(13) Subroutine stack levels
- A maximum of 512 levels (set stack inside RAM)

(14) Multiplication and division
- 16 bits × 8 bits (5 instruction-cycle times)
- 24 bits × 16 bits (12 instruction-cycle times)
- 16 bits ÷ 8 bits (8 instruction-cycle times)
- 24 bits ÷ 16 bits (12 instruction-cycle times)

(15) Oscillation circuits
- Built-in RC oscillation circuit used for the system clock
- CF oscillation circuit used for the system clock. (R_f built in)
- Frequency-variable RC oscillation circuits for system clock use.

(16) System clock divider
- operable on the lowest power consumption
- Minimum instruction cycle time (300ns, 600ns, 1.2µs, 2.4µs, 4.8µs, 9.6µs, 19.2µs, 38.4µs, 76.8µs can be switched by program (when using 10MHz main clock)

(17) Standby function
- HALT mode

  The HALT mode stops program execution while the peripheral circuits keep operating and minimizes power consumption. (VFD display and some serial transfer operations stop). This operation mode can be released by a system reset or an interrupt request.

-HOLD mode

  The HOLD mode stops program execution and CF and RC oscillation circuits. This mode can be released by the following conditions.

  (1) Supply "L" level to the reset terminal
  (2) Supply the selected level to at least one of INT0, INT1, INT2
  (3) Supply an interrupt condition to Port 0

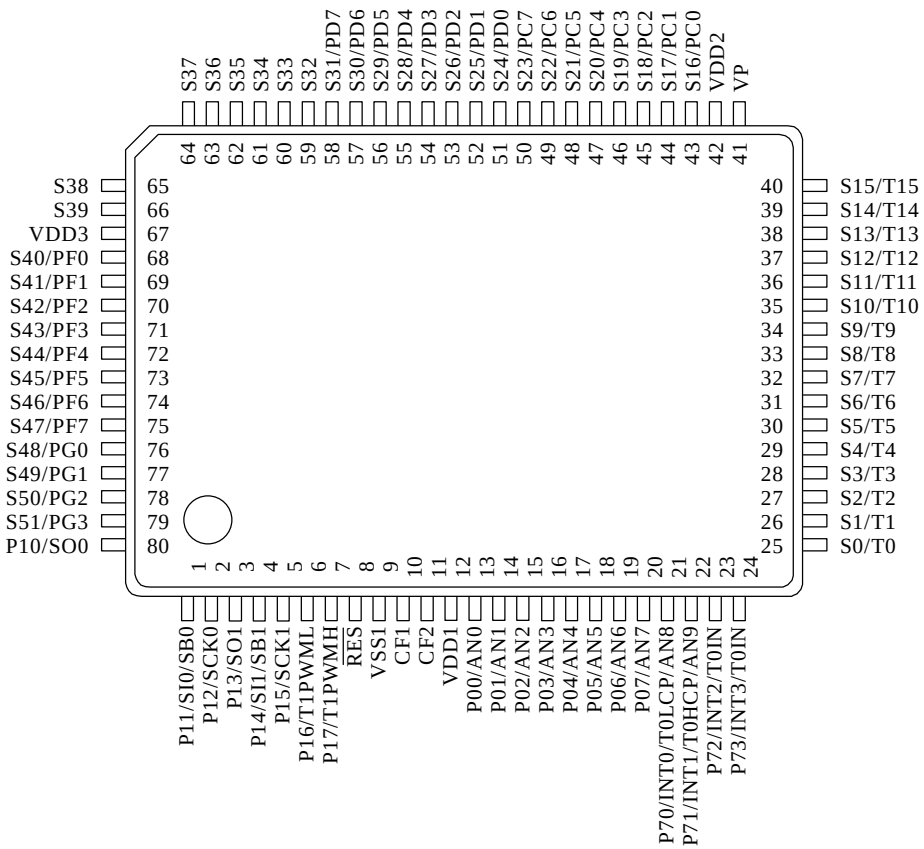
(18) Shipping form
- QIP80E

(19) Development tools
- Evaluation (EVA) chip: LC876093
- Emulator : EVA62S + ECB876600 (Evaluation chip board) + SUB876100 + POD80QFP
  : ICE-B877300+SUB876100+POD80QFP

(20) Same package and pin assignment as mask ROM version.

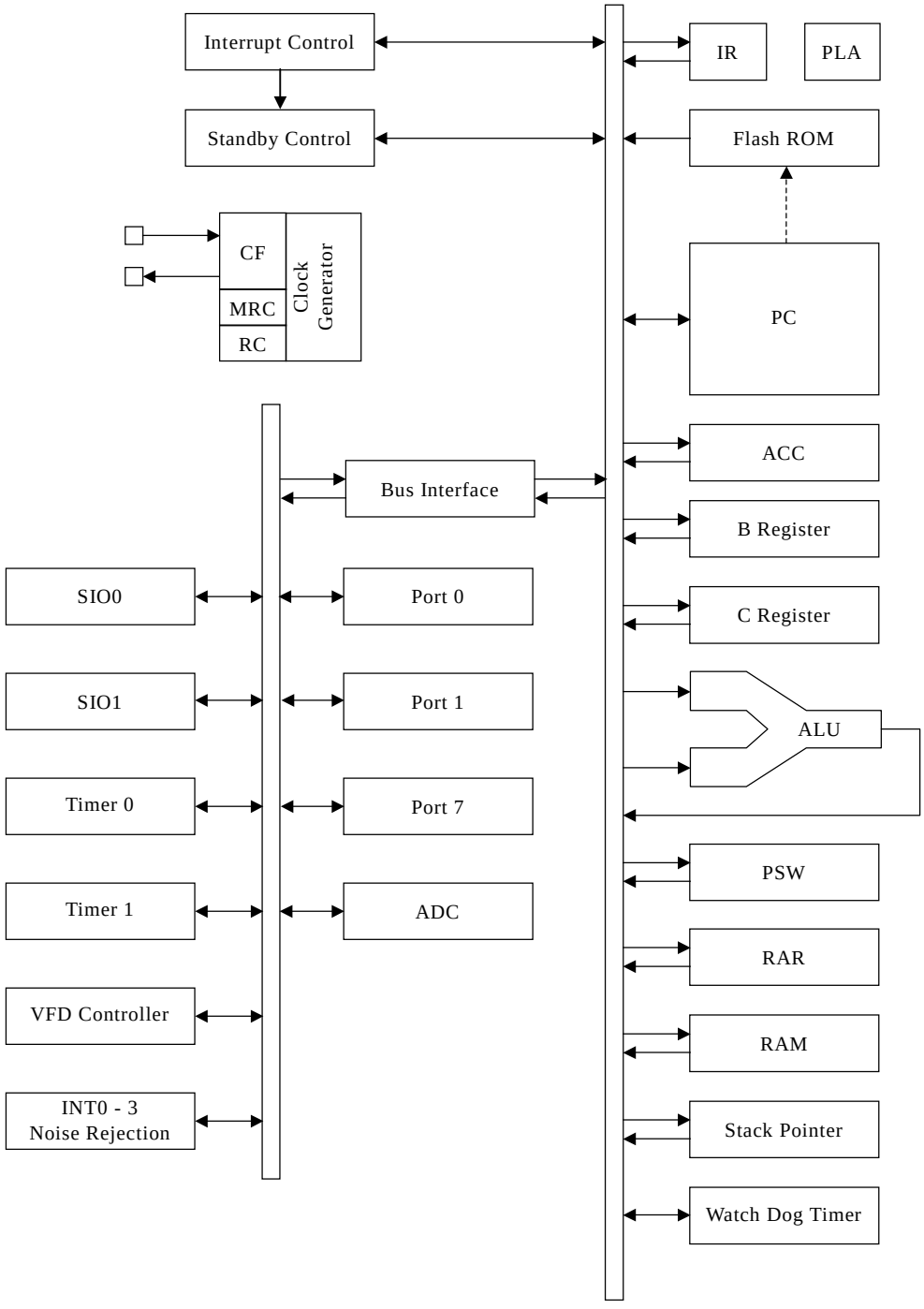
1) LC876100 series options can be set using flash ROM data. Thus testing and evaluation of mass production boards is possible.
2) The flash version has the ability to emulate the RAM and ROM capacity of the mask ROM version.

Pin Assignment



SANYO: QIP80E

System Block Diagram



Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Function description</th><th>Option</th></tr>
<tr><td>VSS1</td><td>-</td><td>Power terminal (-)</td><td>No</td></tr>
<tr><td>VDD1, VDD2, VDD3</td><td>-</td><td>Power terminal (+)</td><td>No</td></tr>
<tr><td>VP</td><td>-</td><td>Power terminal (-)</td><td>No</td></tr>
<tr><td>PORT0
P00 to P07</td><td>I/O</td><td>• 8-bit input/output port
• Data direction programmable in nibble units
• Pull-up resistor provided/not provided (specified in three bits for P01 to P03 and specified in nibble units for P04 to P07)
• HOLD release input
• Port 0 interrupt input
• Other function
AD converter input port : AN0 to AN7</td><td>Yes
(P00 has no option)</td></tr>
<tr><td>PORT1
P10 to P17</td><td>I/O</td><td>• 8-bit input/output port
• Data direction programmable for each bit individually
• Pull-up resistor provided/not provided (specified by bit)
• Other functions
P10 : SIO0 data output
P11 : SIO0 data input, bus input/output
P12 : SIO0 clock input/output
P13 : SIO1 data output
P14 : SIO1 data input, bus input/output
P15 : SIO1 clock input/output
P16 : Timer 1 PWML output
P17 : Timer 1 PWMH output/buzzer output</td><td>Yes</td></tr>
<tr><td>PORT7
P70 to P73</td><td>I/O</td><td>• 4-bit input/output port
• Data direction programmable for each bit individually
• Pull-up resistor provided/not provided (specified by bit)
• Other functions
P70: INT0 input/HOLD release input/Timer 0L capture input/Output for watchdog timer
P71: INT1 input/HOLD release input/Timer 0H capture input
P72: INT2 input/HOLD release input/Timer 0 event input/Timer 0L capture input
P73: INT3 input with noise filter/Timer 0 event input/Timer 0H capture input
AD converter input port : AN8 (P70), AN9 (P71)
• Interrupt detection style
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/ Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>No</td></tr>
<tr><td>S0/T0 to S8/T8</td><td>O</td><td>• Large current output for VFD display controller digit (can be used for segment)</td><td>No</td></tr>
<tr><td>S9/T9 to S15/T15</td><td>O</td><td>• Large current output for VFD display controller segment/digit</td><td>No</td></tr>
<tr><td>S16 to S23</td><td>I/O</td><td>• Output for VFD display controller segment/digit
• Other function
High voltage input port : PC0 to PC7</td><td>No</td></tr>
</table>

Name	I/O	Function description	Option
S24 to S31	I/O	• Output for VFD display controller segment • Other function High voltage input port: PD0 to PD7	No
S32 to S39	O	Output for VFD display controller segment	No
S40 to S47	O	• Output for VFD display controller segment • Other function High voltage output port : PF0 to PF7	No
S48 to S51	I/O	• Output for VFD display controller segment • Other function High voltage input/output port : PG0 to PG3	No
$\overline{\text{RES}}$	I	Reset terminal	No
CF1	I	Input terminal for ceramic resonator	No
CF2	O	Output terminal for ceramic resonator	No

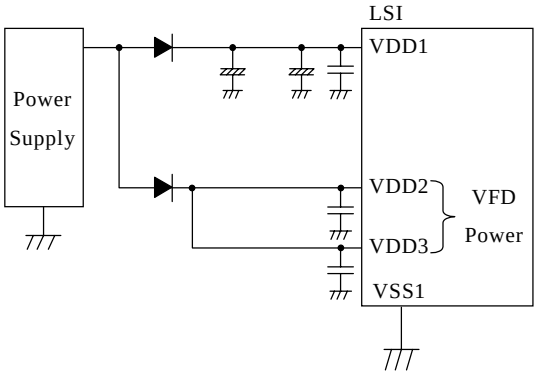
Port Output Configuration

Output configuration and pull-up/pull-down resistor options are shown in the following table.
Input /output is possible even when port is in output mode.

Terminal	Option applies to:	Options	Output Format	Pull-up resistor	Pull-down resistor
P00	–	None	Nch-open drain	None	–
P01 to P07	each bit	1	CMOS	Programmable (Note 1)	–
		2	Nch-open drain	None	–
P10 to P17	each bit	1	CMOS	Programmable	–
		2	Nch-open drain	Programmable	–
P70	–	None	Nch-open drain	Programmable	–
P71 to P73	–	None	CMOS	Programmable	–
S0/T0 to S6/T6	–	None	High voltage Pch-open drain	–	None
S7/T7 to S15/T15	–	None	High voltage Pch-open drain	–	fixed
S16 to S31	–	None	High voltage Pch-open drain	–	None
S32 to S39	–	None	High voltage Pch-open drain	–	fixed
S40 to S51	–	None	High voltage Pch-open drain	–	None

Note 1 Programmable pull-up resisters of Port 0 is specified in three bits (P01 - P03) and specified in nibble units (P04 - P07).

* Note 1: Connect as follows to reduce VDD signal noise and to increase the duration of the backup battery supply.



1. Absolute maximum ratings / Ta=25°C, VSS1=0V

Parameter		Symbol	Pins	Conditions	VDD[V]	Limits min.	typ.	max.	unit
Supply voltage		VDDMAX	VDD1,VDD2, VDD3	VDD1=VDD2=VDD3		-0.3		+6.5	V
Input voltage		VI(1)	• CF1 • $\overline{RES}$			-0.3		VDD+0.3	
		VI(2)	VP			VDD-45		VDD+0.3	
Output voltage		VO(1)	• S0/T0 to S15/T15 • S32 to S47			VDD-45		VDD+0.3	
Input/Output voltage		VIO(1)	• Port 0 • Port 1 • Port 7			-0.3		VDD+0.3	
		VIO(2)	S16 to S31, S48 to S51			VDD-45		VDD+0.3	
High level output current	Peak output current	IOPH(1)	Port 0, 1	• CMOS output • For each pin		-10			mA
		IOPH(2)	Port 71, 72, 73	For each pin		-3			
		IOPH(3)	S0/T0 to S15/T15	For each pin		-30			
		IOPH(4)	S16 to S51	For each pin		-15			
	Total output current	ΣIOAH(1)	Port 0	Total of all pins		-30			
		ΣIOAH(2)	Port 1	Total of all pins		-30			
		ΣIOAH(3)	Port 7	Total of all pins		-5			
		ΣIOAH(4)	S0/T0 to S15/T15	Total of all pins		-65			
		ΣIOAH(5)	S16 to S27	Total of all pins		-60			
		ΣIOAH(6)	S28 to S39	Total of all pins		-60			
		ΣIOAH(7)	S40 to S51	Total of all pins		-60			
Low level output current	Peak output current	IOPL(1)	Port 0, 1	For each pin				20	
		IOPL(2)	Port 7	For each pin				5	
	Total output current	ΣIOAL(1)	Port 0	Total of all pins				60	
		ΣIOAL(2)	Port 1, 7	Total of all pins				60	
Maximum power consumption		Pdmax	QIP80E	Ta = -20 to+70°C				438	mW
Operating temperature range		Topr				-20		+70	°C
Storage temperature range		Tstg				-55		+125	

2. Recommended operating range / Ta=-20°C to +70°C, VSS1=0V

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[V]	min.	typ.	max.	unit
Operating supply voltage range	VDD(1)	VDD1=VDD2 =VDD3	0.294µs ≤ tCYC ≤ 200µs		4.5		5.5	V
Hold voltage	VHD	VDD1	RAM and register data are kept in HOLD mode.		2.0		5.5	
Pull-down voltage	VP	VP		4.5 - 5.5	-35		VDD	
Input high voltage	VIH(1)	Port 0	Output disable	4.5 - 5.5	0.3VDD +0.7		VDD	
	VIH(2)	• Port 1 • Port 71, 72, 73 • P70 port input/interrupt	Output disable	4.5 - 5.5	0.3VDD +0.7		VDD	
	VIH(3)	• S16 to S31 • S48 to S51	Output P-channel Tr. OFF	4.5 - 5.5	0.33VDD +1.0		VDD	
	VIH(4)	Port 70 Watchdog timer	Output disable	4.5 - 5.5	0.9VDD		VDD	
	VIH(5)	• CF1 • $\overline{RES}$		4.5 - 5.5	0.75VDD		VDD	
Input low voltage	VIL(1)	Port 0	Output disable	4.5 - 5.5	VSS		0.15VDD +0.4	
	VIL(2)	• Port 1 • Port 71, 72, 73 • P70 port input/interrupt	Output disable	4.5–5.5	VSS		0.1VDD +0.4	
	VIL(3)	• S16 to S31 • S48 to S51	Output P-channel Tr. OFF	4.5 - 5.5	VSS		0.2VDD	
	VIL(4)	Port 70 Watchdog timer	Output disable	4.5 - 5.5	VSS		0.8VDD -1.0	
	VIL(5)	• CF1 • $\overline{RES}$		4.5 - 5.5	VSS		0.25VDD	
Operation cycle time	tCYC			4.5 - 5.5	0.294		200	µs
External system clock frequency	FEXCF(1)	CF1	• Leave CF2 pin open • System clock divider set to 1/1 • External clock DUTY= 50±5%	4.5 - 5.5	0.1		10	MHz
			• Leave CF2 pin open • System clock divider set to 1/2	4.5 - 5.5	0.2		20	
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	• 10MHz (ceramic resonator) • Refer to figure 1	4.5 - 5.5		10		
	FmCF(2)	CF1, CF2	• 4MHz (ceramic resonator) • Refer to figure 1	4.5 - 5.5		4		
	FmRC		Internal RC oscillation	4.5 - 5.5	0.3	1.0	2.0	

(Note 1) The oscillation parameters are shown on table 1 and 2.

3. Electrical characteristics / Ta=-20°C to +70°C, VSS1=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
Input high current	IIH(1)	Ports 0: N-ch open drain output	• Output disable • VIN=VDD (including the off-leak current of the output Tr.)	4.5 - 5.5			5	µA
	IIH(2)	Port 0, 1, 7	• Output disable • Pull-up resistor OFF • VIN=VDD (including the off-leak current of the output Tr.)	4.5 - 5.5			1	
	IIH(3)	• S16 to S31 • S48 to S51 (Port C, D, G)	• Using as an input port • VIN=VDD	4.5 - 5.5			60	
	IIH(4)	$\overline{RES}$	VIN=VDD	4.5 - 5.5			1	
	IIH(5)	CF1	VIN=VDD	4.5 - 5.5			15	
Input low current	IIL(1)	Port 0, 1 ,7	• Output disable • Pull-up resistor OFF • VIN=VSS (including the off-leak current of the output Tr.)	4.5 - 5.5	-1			
	IIL(2)	$\overline{RES}$	VIN=VSS	4.5 - 5.5	-1			
	IIL(3)	CF1	VIN=VSS	4.5 - 5.5	-15			
Output high voltage	VOH(1)	Port 0, 1	IOH= -1.0mA	4.5 - 5.5	VDD-1			V
	VOH(2)		IOH= -0.1mA	4.5 - 5.5	VDD-0.5			
	VOH(3)	Port 7	IOH= -0.4mA	4.5 - 5.5	VDD-1			
	VOH(4)	S0/T0 to S15/T15	IOH= -20mA	4.5 - 5.5	VDD-1.8			
	VOH(5)		IOH= -1.0mA IOH at any single pin is not over 1mA.	4.5 - 5.5	VDD-1			
	VOH(6)	S16 to S51	IOH=-5.0mA	4.5 - 5.5	VDD-1.8			
	VOH(7)		IOH=-1.0mA IOH at any single pin is not over 1mA.	4.5 - 5.5	VDD-1			
Output low voltage	VOL(1)	Port 0, 1	IOL=9mA	4.5 - 5.5			1.5	
	VOL(2)		IOL=1.5mA	4.5 - 5.5			0.4	
	VOL(3)	Port 7	IOL=1mA	4.5 - 5.5			0.4	
Pull-up MOS Tr. resistor	Rpu	Port 0, 1, 7	VOH=0.9VDD	4.5 - 5.5	15	40	70	kΩ
Off-leak current of the output Tr.	IOFF(1)	• S0/T0 to S6/T6 • S16 to S31 • S48 to S51	• Output P-ch Tr. OFF • VOUT=VSS	4.5 - 5.5	-1			µA
	IOFF (2)		• Output P-ch. Tr. OFF • VOUT=VDD - 40V	4.5 - 5.5	-30			

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
Resistance of the low level hold Tr	Rinpd	• S16 to S31 • S48 to S51	Output P-ch Tr. OFF	4.5 - 5.5		200		kΩ
High voltage pull-down resistor	Rpd	• S7/T7 to S15/T15 • S32 to S47	• Output P-ch Tr. OFF • VOUT=3V • Vp= -30V	5.0	60	100	200	
Hysteresis voltage	VHIS(1)	• Port 1, 7 • $\overline{\text{RES}}$		4.5 - 5.5		0.1VDD		V
Pin capacitance	CP	All pins	• All pins except the measured terminal : VIN=VSS • f=1MHz • Ta=25°C	4.5 - 5.5		10		pF

4. Serial input/output characteristics / Ta=-20°C to +70°C, VSS1=0V

Parameter			Symbol	Pins	Conditions	VDD[V]	Limits min.	typ.	max.	unit
Serial clock	Input clock	Cycle	tSCK(1)	SCK0(P12)	Refer to figure 5	4.5 - 5.5	4/3			tCYC
		Low Level pulse width	tSCKL(1)				2/3			
			tSCKLA(1)				2/3			
		High Level pulse width	tSCKH(1)				2/3			
			tSCKHA(1)				5			
		Cycle	tSCK(2)	SCK1(P15)	Refer to figure 5	4.5 - 5.5	2			
		Low Level pulse width	tSCKL(2)				1			
		High Level pulse width	tSCKH(2)				1			
	Output clock	Cycle	tSCK(3)	SCK0(P12)	• CMOS output • Refer to figure 5	4.5 - 5.5	4/3			
		Low Level pulse width	tSCKL(3)					1/2		tSCK
			tSCKLA(2)					3/4		
		High Level pulse width	tSCKH(3)					1/2		
			tSCKHA(2)					2		
		Cycle	tSCK(4)	SCK1(P15)	• CMOS output • Refer to figure 5	4.5 - 5.5	2			tCYC
		Low Level pulse width	tSCKL(4)					1/2		tSCK
		High Level pulse width	tSCKH(4)					1/2		
Serial input	Data set-up time		tsDI	SI0(P11), SI1(P14), SB0(P11), SB1(P14)	• Data set-up to SI0CLK • Data hold from SI0CLK • Refer to figure 5	4.5 - 5.5	0.03			µs
	Data hold time		thDI				0.03			
Serial output	Output delay time		tdDO	SO0(P10), SO1(P13), SB0(P11), SB1(P14)	• Data hold from SI0CLK • Time delay from SI0CLK trailing edge to the SO data change in the open drain • Refer to figure 5	4.5 - 5.5			1/3tCYC +0.05	

5. Pulse input conditions / Ta=-20°C to +70°C, VSS1=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72)	• Interrupt acceptable • Timer 0 event input acceptable	4.5 - 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) (The noise rejection clock is selected to 1/1)	• Interrupt acceptable • Timer 0 event input acceptable	4.5 - 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) (The noise rejection clock is selected to 1/32)	• Interrupt acceptable • Timer 0 event input acceptable	4.5 - 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) (The noise rejection clock is selected to 1/128)	• Interrupt acceptable • Timer 0 event input acceptable	4.5 - 5.5	256			
	tPIL(5)	$\overline{\text{RES}}$	Reset acceptable	4.5 - 5.5	200			µs

6. AD converter characteristics / Ta=-20°C to + 70°C, VSS1=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
Resolution	N	AN0(P00) to AN7(P07) AN8(P70), AN9(P71)		4.5 - 5.5		8		bit
Absolute precision	ET		(Note2)	4.5 - 5.5			±1.5	LSB
Conversion time	tCAD		AD conversion time = 32 × tCYC (ADCR2=0) (Note 3)	4.5 - 5.5	15.62 (tCYC= 0.488µs)		97.92 (tCYC= 3.06µs)	µs
			AD conversion time = 64 × tCYC (ADCR2=1) (Note 3)		18.82 (tCYC= 0.294µs)		97.92 (tCYC= 1.53µs)	
Analog input voltage range	VAIN			4.5 - 5.5	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5 - 5.5			1	µA
	IAINL		VAIN=VSS	4.5 - 5.5	-1			

(Note 2) Absolute precision excludes the quantizing error (±1/2 LSB).

(Note 3) The conversion time is the time from executing the AD conversion instruction to setting the complete digital conversion value in the register.

. 7. Current consumption characteristics / Ta=-20°C to +70°C, VSS1=0V

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[V]	min.	typ.	max	unit
Current dissipation during basic operation (Note 4)	IDDOP(1)	VDD1= VDD2= VDD3	•FmCF=10MHz for Ceramic resonator oscillation •System clock: CF oscillation(10MHz) •Internal RC oscillation stopped. •Frequency Variable RC oscillation halted. •Divider set to 1/1	4.5-5.5		16	35	mA
	IDDOP(2)		•CF1=20MHz for external clock •System clock: CF1 oscillation(20MHz) •Internal RC oscillation stopped. •Frequency Variable RC oscillation halted. •Divider set to 1/2	4.5-5.5		17	36	
	IDDOP(3)		•FmCF=4MHz Ceramic resonator oscillation •System clock: CF oscillation (4MHz) •Internal RC oscillation stopped. •Frequency Variable RC oscillation halted. •Divider set to 1/1	4.5-5.5		7.5	21	
	IDDOP(4)		•FmCF=0Hz (Oscillation stop) •Frequency Variable RC oscillation halted. •System clock: Internal RC oscillation •Divider set to 1/2	4.5-5.5		1.5	11	

Continued

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max	unit
Current dissipation during basic operation (Note 4)	IDDOP(5)	VDD1=VDD2=VDD3	•FmCF=0Hz (Oscillation stop) •Internal RC oscillation stopped. •System clock=1MHz with the frequency variable RC oscillation •Divider set to 1/2	4.5-5.5		2.7	13	mA
Current dissipation HALT mode (Note 4)	IDDHALT(1)	VDD1=VDD2=VDD3	HALT mode •FmCF=10MHz for Ceramic resonator oscillation •System clock : CF oscillation(10MHz) •Internal RC oscillation stopped. •Frequency Variable RC oscillation halted. •Divider: 1/1	4.5-5.5		3.5	12	mA
	IDDHALT(2)		HALT mode •CF1=20MHz for external clock •System clock : CF1 oscillation •Internal RC oscillation stopped. •Frequency Variable RC oscillation halted. •Divider 1/2	4.5-5.5		4	13	
	IDDHALT(3)		HALT mode •FmCF=4MHz for Ceramic resonator oscillation •System clock : CF oscillation(4MHz) •Internal RC oscillation •Frequency Variable RC oscillation halted. •Divider: 1/1	4.5-5.5		2	6	mA

Continued

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max	unit
Current dissipation HALT mode (Note 4)	IDDHALT(4)	VDD1= VDD2= VDD3	HALT mode •FmCF=0Hz (Oscillation stop.) •System clock : Internal RC oscillation •Frequency Variable RC oscillation halted. •Divider: 1/2	4.5-5.5		500	1600	µA
	IDDHALT(5)		•HALT mode •FmCF=0Hz (Oscillation stop.) •Internal RC oscillation stopped. •System clock=1MHz with the frequency variable RC oscillation •Divider: 1/2	4.5-5.5		1500	3600	
Current dissipation HOLD mode	IDDHOLD(1)	VDD1	HOLD mode •CF1=VDD or open circuit (when using external clock)	4.5-5.5		0.05	25	µA

(Note 4) The currents of the output transistors and the pull-up MOS transistors are ignored.

8. F-ROM write characteristics / Ta=+10 to +55°C VSS1=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
On-board writing current	IDDFW(1)	VDD1	• 128-byte writing • Including erase time current	4.5 - 5.5		30	65	mA
Writing time	tFW(1)		• 128-byte writing • Including data erase time • Excluding time to fetch 128 byte data	4.5 - 5.5		5	10	mS

Main system clock oscillation circuit characteristics

The characteristics in the table bellow is based on the following conditions:

1. Using the standard oscillation evaluation board SANYO has provided.
2. Using the external peripheral parts with the indicated value.
3. The recommended circuit parameters for the peripheral parts are verified by the oscillator manufacture.

Table 1. Recommended circuit parameters for the main system clock using the ceramic resonator

Frequency	Manufacturer	Oscillator	Recommended circuit parameters			Operating supply voltage range	Oscillation stabilizing time		Notes
			C1	C2	Rd1		typ	max	
10MHz	Murata Factory	CSTLS10M0G53-B0	(15pF)	(15pF)	150Ω	4.5V～5.5V	0.03mS	0.25mS	C1 and C2 are built-in.
		CSTCC10M0G53-R0	(15pF)	(15pF)	150Ω	4.5V～5.5V	0.03mS	0.25mS	
4MHz	Murata Factory	CSTLS4M00G53-B0	(15pF)	(15pF)	330Ω	4.5V～5.5V	0.03mS	0.25mS	C1 and C2 are built-in.
		CSTCR4M00G53-R0	(15pF)	(15pF)	330Ω	4.5V～5.5V	0.03mS	0.25mS	

*The oscillation stabilizing time is a period until the oscillation becomes stable after VDD becomes higher than minimum operating voltage. (Refer to Figure 3)

(Notes) • Since the oscillation frequency precision is affected by the circuit pattern, place the oscillation related parts as close to the oscillation pins as possible, using the shortest possible pattern length.

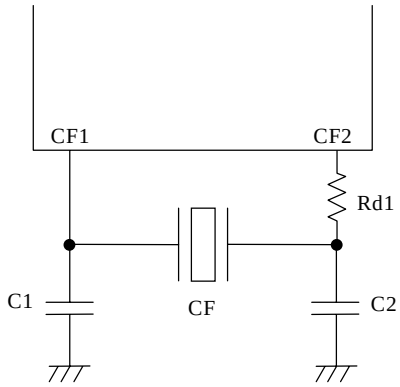


Figure 1 Ceramic oscillation circuit

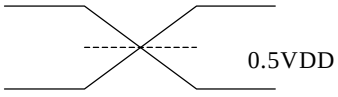
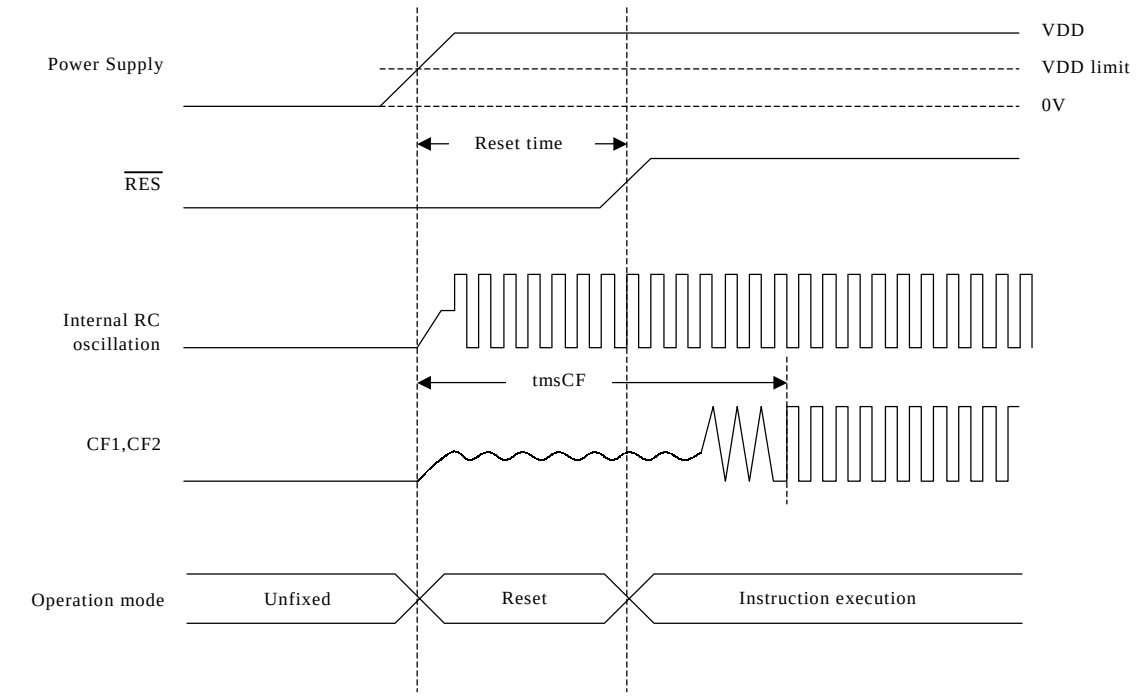
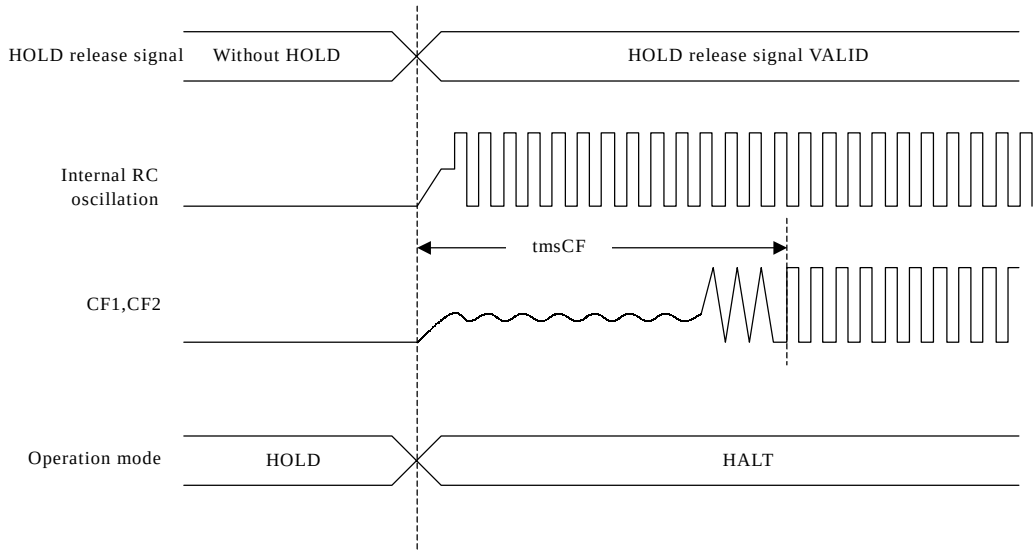


Figure 2 AC timing point

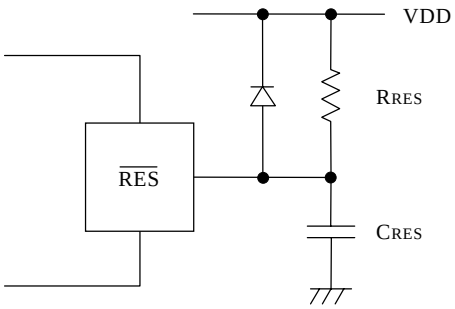


Reset time and oscillation stabilization time



HOLD release signal and oscillation stabilization time

Figure 3 Oscillation stabilization time



(Note) Select CRES and RRES value to assure that at least 200μs reset time is generated after the VDD becomes higher than the minimum operating voltage.

Figure 4 Reset circuit

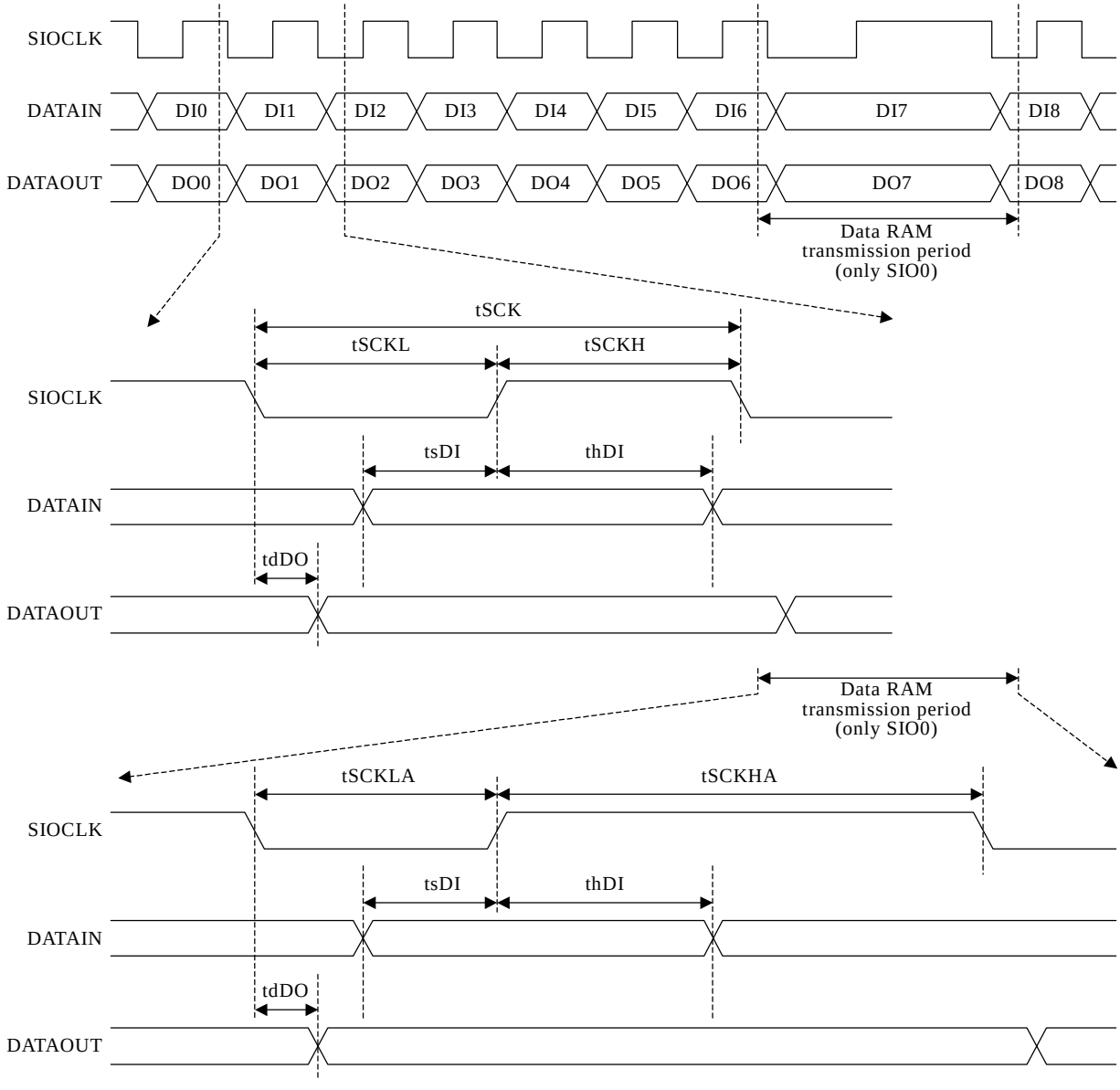


Figure 5 Serial input / output test condition

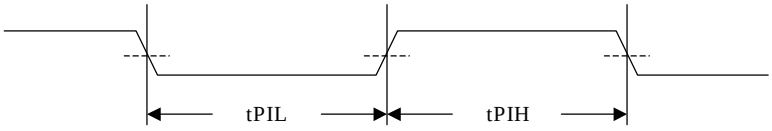


Figure 6 Pulse input timing condition